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P871,874,876



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1.1 INTRODUCTION

The P871 minicomputer system utilizes the CP1BF Central Processor Unit (CPU), which is the successor of the P851M-CPU and CP1A-CPU.
The P874 minicomputer system utilizes the CP7E Central Processor Unit (CPU), which combines the advantages of the P857M-CPU with the smaller physical size of the Eurocard.
The P876 minicomputer system utilizes the CP2B Central Processor Unit which is also called CIP: Central Instruction Processor. The CP2B is about 3 times faster than the CP7E processor.

The CP7E and CP2B employ Microprocessor technology to perform 3 CPU functions:

. Arithmetic Logic Unit, in the format of 4 x 4-bit slices to form the 16-bit word.
. Memory Address Sequensor, in the format of 4 x 4-bit slices to form the 16-bit memory address.
. Micro-Program Sequensor which has control over most CPU functions and their execution (discrete on CP2B).

The processors use the P857 instruction set plus an extra three groups:

. Bit String Handling.
. Address Loading.
. Character String Handling.

The system input/output and control is with the Unified Product Line (UPL) Bus which interconnects all system units. The Central Processing Unit may be connected with other devices in the P800 family via the UPL Bus; these devices are:

. GPBS (P851) Control Units.
. UPL DMA's, IOP's, Control Units and Memories.
. GPB (P856 and P857) Control Units using the Translator Card (TUGP).

The principle facilities available with the P871/4/6 are as follows:

. 16 hardware registers.
. V24 interface for operators peripheral, integrated on CP1BF and CP7E.
. V24 interface for Control Panel.
. Power Failure/ Automatic Restart.
. Battery Back-Up after Power Failure.
. Real Time Clock.
. 2 IOP Channels (16 sub-channels), integrated on CP7E (MIOP).
. 32 parallel interrupts of which 4 are internal to the CPU (CP1BF: 15 parallel inputs).
  Up to 61 serial encoded interrupts.
. Hardware Bootstrap Loading with facility to load from one of 16 external devices.
. One of two serial Control Panels: HHCP - displays a hexadecimal address or data, FRCP - displays hexadecimal address and data simultaneously.
. Logical addressing for up to 32k words, 16 bits (CPU function).
. Physical addressing for up to 8M words, 24 bits (MMU Function) (CP2BF: 512KW, 20 bits).
. Memory Protection on a Page basis (MMU Function).
. Stop On Preset Address for up to 512k words, 20 bits (SOPA Function) (CP7E), up to 8M words, 24 bits (SOPA function CP2B).

The principle components showing their connection to the CPU's are shown in Figure 1.1a, b, c.

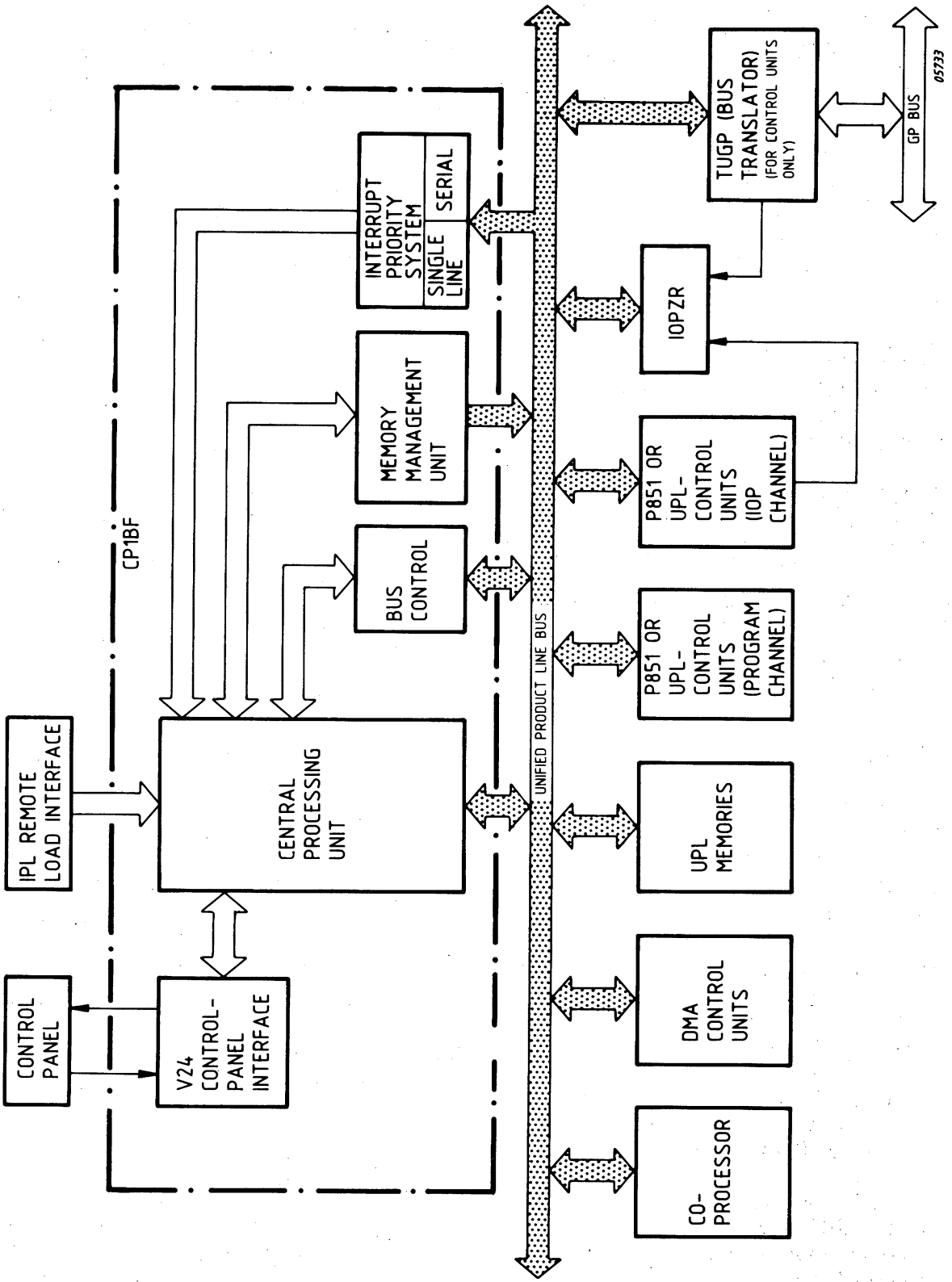


Figure 1.1a P871 MAIN SYSTEM COMPONENTS

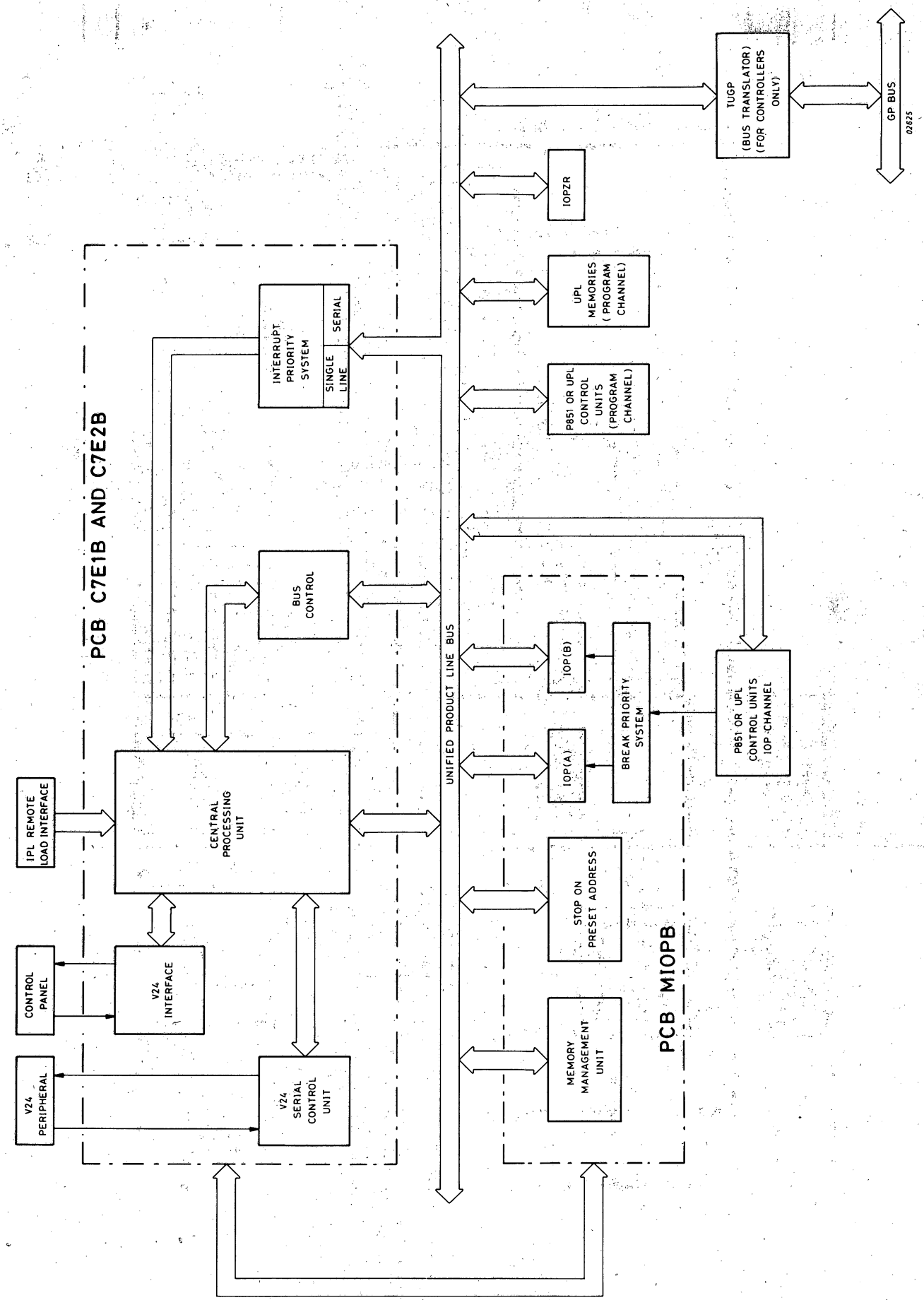


Figure 1.1b P874 MAIN SYSTEM COMPONENTS

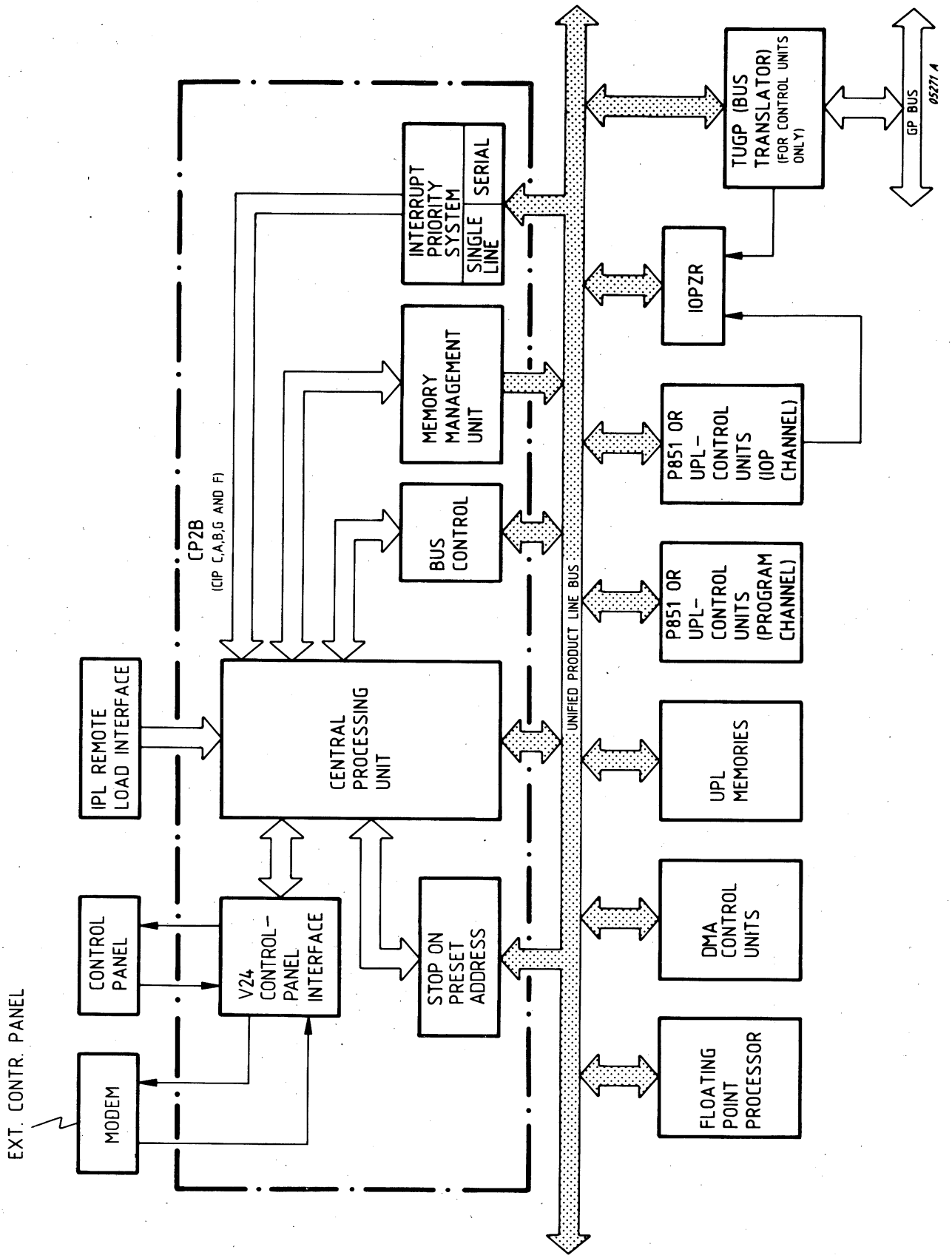


Figure 1.1c P876 MAIN SYSTEM COMPONENTS

1.2 UNIFIED PRODUCT LINE BUS

In the following description N, behind a signal name, stands for "Active Low". The signals and lines, associated with the Bus functions are.

Bus Allocation Signals

BUSRN A signal bus request which is sent to the bus controller in the CPU by a master which requires control of the bus to effect an exchange.

BSYN A signal Bus Busy which is shared by all masters. It is set to "0" by the master which has been given control of the bus so that the exchange can commence without interruption.

MSN A signal Master Selected which is transmitted to all other masters by the master which has become master of the bus to block all activity of the priority selection chain. The signal is released when the master is ready for the next priority transaction.

ERQN Enable Request is sent by the Bus controller and received by masters working with the second level of priority. ERQN is set to 0 when there is no request, no current allocation, no master selected, no current exchange on the bus.

OKO A signal generated by the bus controller. It is sent to the master having the highest priority (determined by hard wiring in the priority selection chain).

OKI A master which receives signal OKO regards the signal as OKI. It then retransmits a further OKO to the next master in the priority chain. The first master to receive OKI (set to "1" and to retransmit OKO reset to "Ø") is next master of the bus.

Bus Address Lines

MADØØ - MAD15, MADEØØ-MADEØ7

These lines carry the memory address, register address, peripheral address or the requested control unit function. They are qualified by a timing signal from a master.

1. Memory Exchange (qualified by TMRN)
   MADØØ through MAD14: these lines carry the 15-bit memory address required to access up to 32k 16-bit words of memory.
   MAD15: this line is only significant in character operations. It carries the least significant bit of the memory address and indicates whether the right hand character (MAD15 = 1) or the left hand character (MAD15 = Ø) of a word is addressed.
   MADEOO-through MADEØ7: these lines extend the memory addressing to 8M 16 bit words.
2. External Register (qualified by TMEN)
   MADØ8 through MAD15: these lines give the 8-bit address of an external register.
   MADØ4: this line is used to indicate a Read (MADØ4 = 1) or Write (MADØ4 = Ø) operation.
3. Peripheral Control Unit Exchange (qualified by TMPN)
   MAD1Ø through MAD15: these lines carry the 6-bit device address required to access up to 64 control units.
   MADØ4 = direction of the exchange of Ø to control unit
   1 to master.
   MADØ8 = indicates whether a data exchange, command or status exchange.
   MADØ9 = this line is a function line reserved for special control units.
   MADØ3 = this line is used to indicate whether the current word or character exchange is the last exchange. If 1: last exchange.

Bus Data Lines

BIOØØN - BIO15N

16 input/output lines used to transfer data between units.

Data and Command Exchange Signals

Timing Signals

TMRN This signal is raised by a master and is used to validate the data and address and to control the timing of the exchange with memory.

TMPN This signal is raised by a master and is used to validate the control data and address and to control the timing of an exchange with peripheral control unit.

TMEN This signal is raised by a master and is used to validate the data and address and to control the timing of an exchange between a master and a unit containing an external register.

TSMN This signal is raised by a slave as answer to TMRN, TMPN or TMEN and validates the data during an input operation or to signal the termination of an exchange.

Miscellaneous Signals

CLEARN This signal is sent from the CPU to all units connected to the Bus and initiates a general reset of these units.

WRITE This signal is raised by a master to indicate that the exchange is "Write to Memory". If not present a "Read from memory" is indicated.

CHA This signal is sent from a master to memory to specify that the requested exchange is to be carried out in character mode. If Ø the change is in word mode.

ACN This signal is sent by a control unit to indicate that it accepts a request from the CPU to carry out a designated function.

BAWOFN This signal is raised to inform that battery power is (was) switched off.

PWFN This signal is raised during the power on or power off or power failure sequence and is used within the system to ensure an orderly run down of operations without loss of data.

RSLN This signal is raised during the power on or power restoration sequence and is used within the system to ensure an orderly commencement or resumption of operation without loss of data.

IRN Ø,1 This signal is raised by the control unit to inform the CPU that a data transfer or status transfer is required.

BRN Ø,1 This signal is raised by the control unit and is sent to the I/O Processor to request a data transfer.

BCI BUS Coded Interrupt (serial)
This interrupt is sent by a control unit with Interrupt Handler Chip
Code: 1 start bit, 6 source bits (interrupt level), 6 destination bits and 2 spare bits.

INCL Interrupt Clock. Sent by CPU to all CU's for synchronisation of BCI.

Time-out

For a normal data transfer TMRN, TMEN and TMPN are sent from the CPU to initiate the transfer.
TSMN is the reply of the slave.
If no TSMN signal is received within 6.4 microsec. the CPU generates an external signal TSMN which frees the bus.

Relation with Power-on/Power-off

After POWER-ON a master is not authorized to request the bus until PWFN is high. When PWFN is going low, the masters must limit their exchanges in order to give to the CPU enough time to execute the power failure routine.

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1C01	+12V	1B01	ERQN	1A01	-12V
1C02	+5VM	1B02	BUSRN	1A02	+5VM
1C03	BCI	1B03	MSN	1A03	INCL
1C04	*	1B04	ØV	1A04	*
1C05	*	1B05	BSYN	1A05	*
1C06	ØV	1B06	OKO	1A06	ØV
1C07	PWFN	1B07	** OKI	1A07	RSLN
1C08	CLEARN	1B08	RTCN	1A08	ACN
1C09	ØV	1B09	* BAWOFN	1A09	ØV
1C10	TMPN	1B10	*** STOPN	1A10	TSMN
1C11	TMEN	1B11	ØV	1A11	TMRN
1C12	ØV	1B12	MADEØ	1A12	ØV
1C13	MADØØ	1B13	MADE1	1A13	MADØ1
1C14	MADØ2	1B14	ØV	1A14	MADØ3
1C15	MADØ4	1B15	MADE2	1A15	MADØ5
1C16	MADØ6	1B16	MADE3	1A16	MADØ7
1C17	MADØ8	1B17	MADE4	1A17	MADØ9
1C18	MAD1Ø	1B18	MADE5	1A18	MAD11
1C19	MAD12	1B19	MADE6	1A19	MAD13
1C20	MAD14	1B20	MADE7	1A20	MAD15
1C21	CHA	1B21	ØV	1A21	WRITE
1C22	ØV	1B22	*	1A22	Ø
1C23	BIOØ8N	1B23	*	1A23	BIOØØN
1C24	BIOØ9N	1B24	*	1A24	BIOØ1N
1C25	BIO1ØN	1B25	*	1A25	BIOØ2N
1C26	BIO11N	1B26	ØV	1A26	BIOØ3N
1C27	BIO12N	1B27	*	1A27	BIOØ4N
1C28	BIO13N	1B28	*	1A28	BIOØ5N
1C29	BIO14N	1B29	*	1A29	BIOØ6N
1C30	BIO15N	1B30	*	1A30	BIOØ7N
1C31	+12VM	1B31	+5VL	1A31	+12VM
1C32	+5VL	1B32	+5VL	1A32	+5VL

* These signals are not bussed on the backpanel.
** This point is not used at the CPU level.
OKO is connected with OKI from the next connector of the backpanel.
*** Not used in P800, however signals may still be connected.

Table 1.1 UPL BUS

1.3 TYPICAL BUS ASPECTS GP - UPL.

Bus timing: difference of memory access (write)

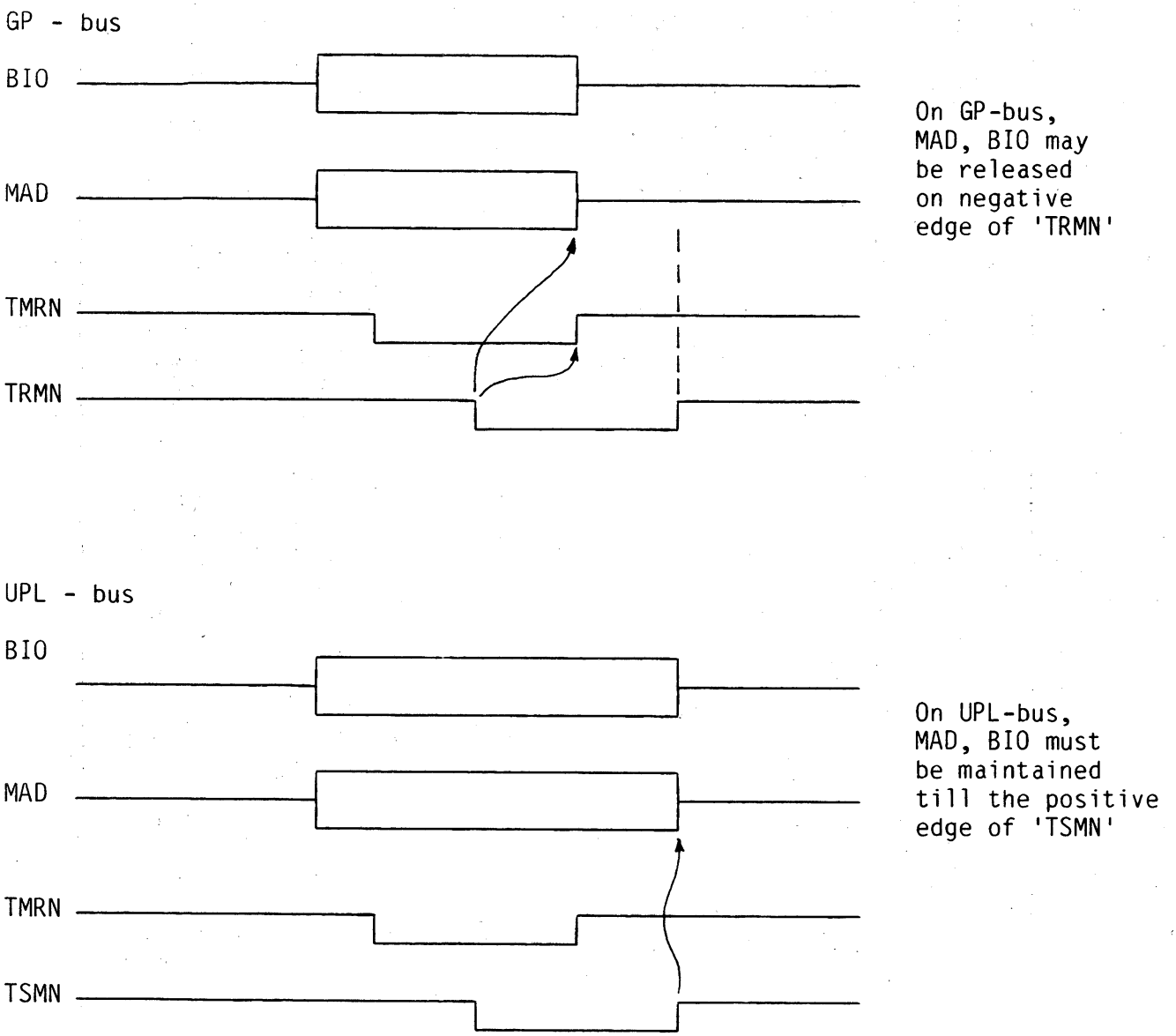


Figure 1.2 GP - UPL BUS TIMING

1.4 UPL BUS ALLOCATION

- Bus priority logic will select the master which requests the bus. In case of more requests, only the master with highest priority will access the bus.
- Master may be switched to second class of priority. In that case bus access can only be done if no requests are available, nor the bus is busy. This is indicated by ERQN.
- The CPU may only use the bus if no other masters do a bus request.

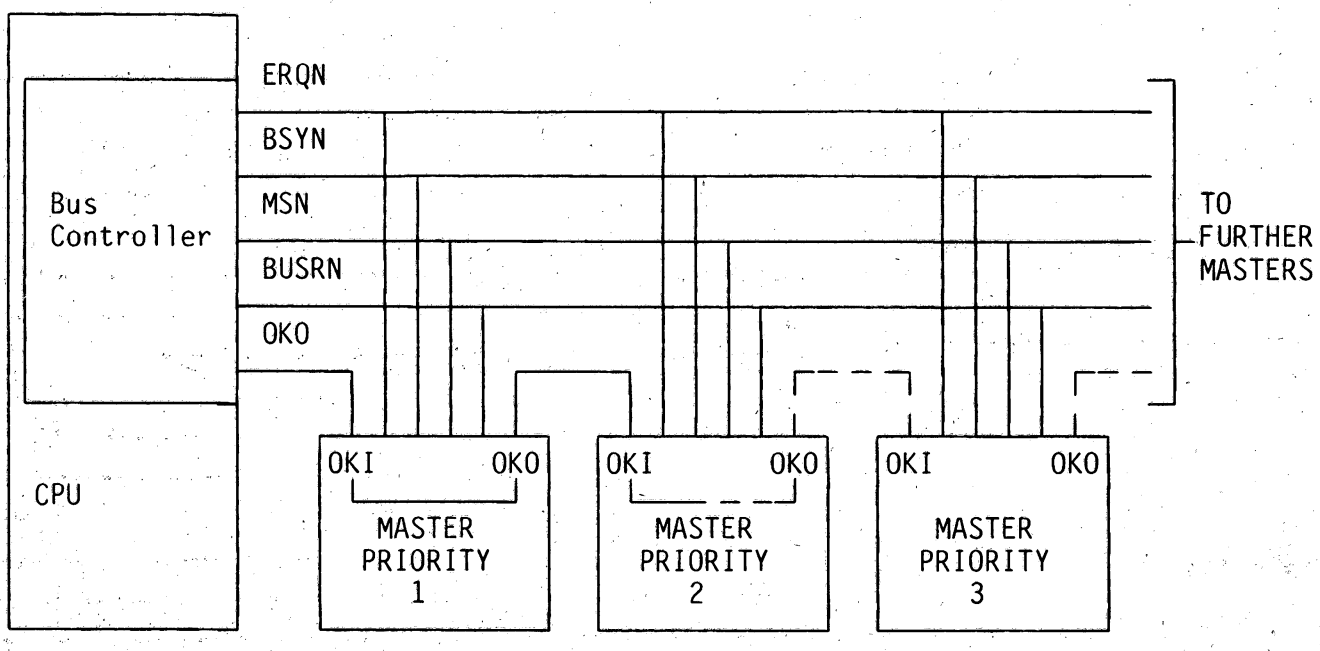


Figure 1.3 UPL BUS PRIORITY CONTROL

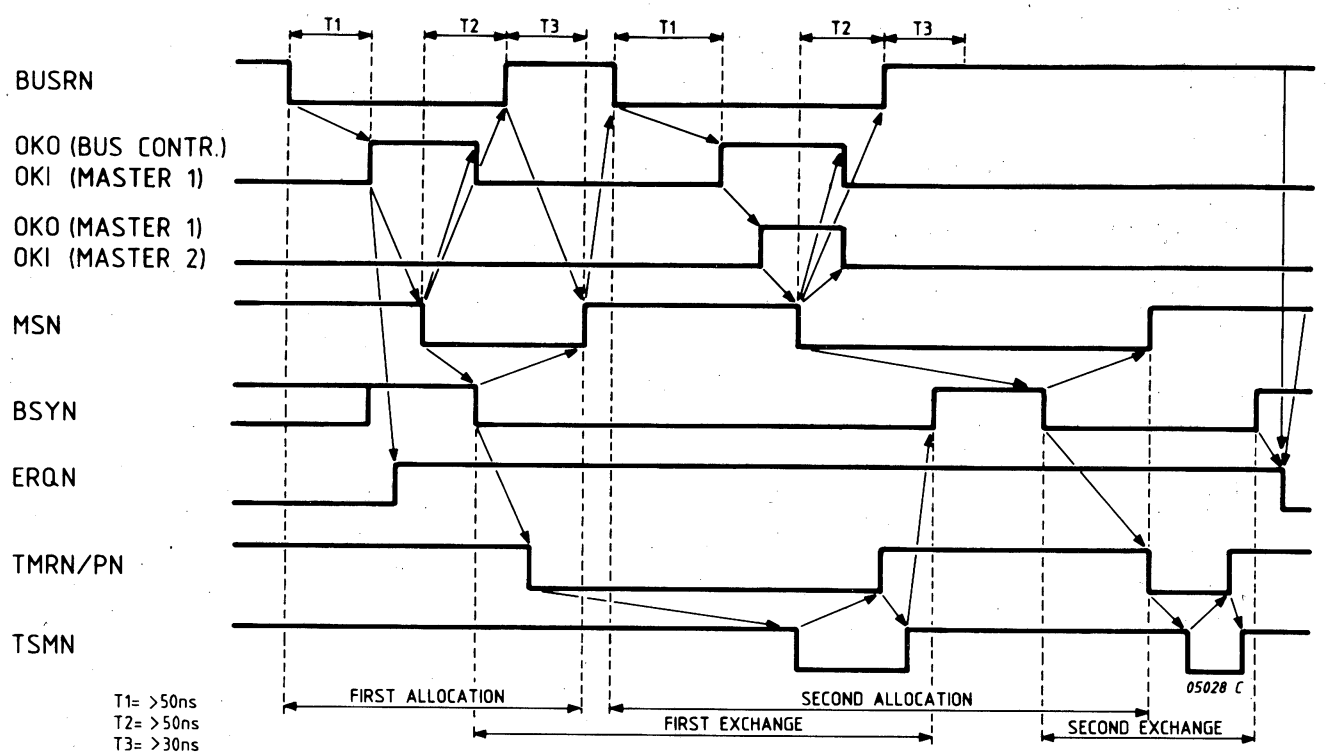
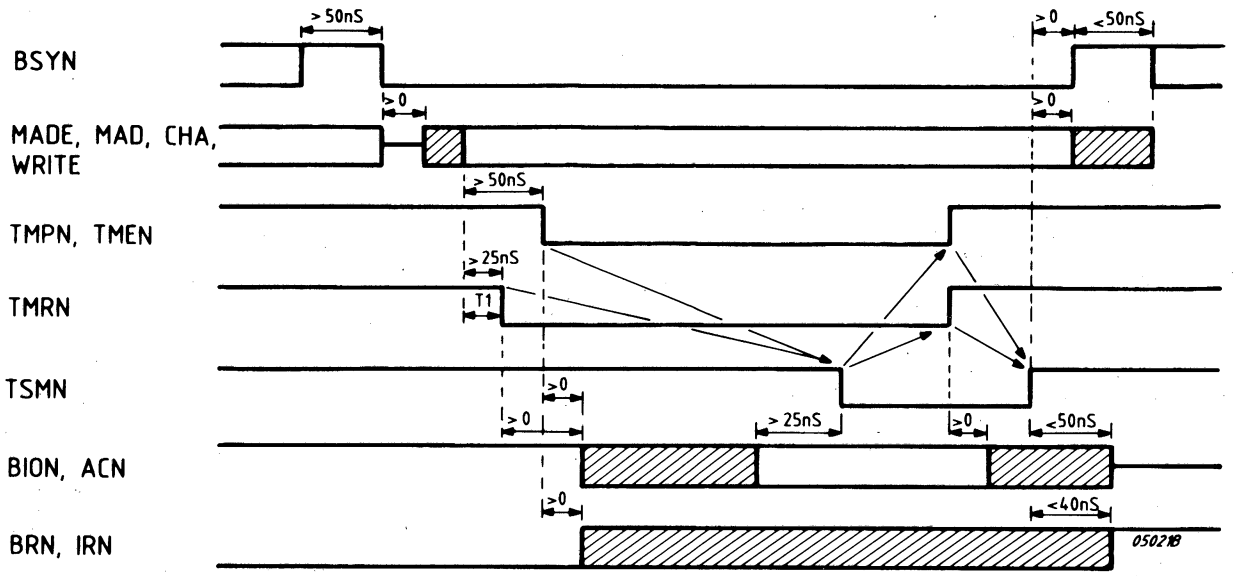


Figure 1.4 EXAMPLE OF 2 BUS ALLOCATIONS



Remarks:
1. New Masters will be able to generate TMRN with t1 = 50ns to be able to work with P851 memories, new memories consider t1 = 25ns.
2. New Masters which work with P851 control units must take into account that ACN signal can be defined 95ns after TSMN = Ø.

Figure 1.5a MASTER TO SLAVE TIMING

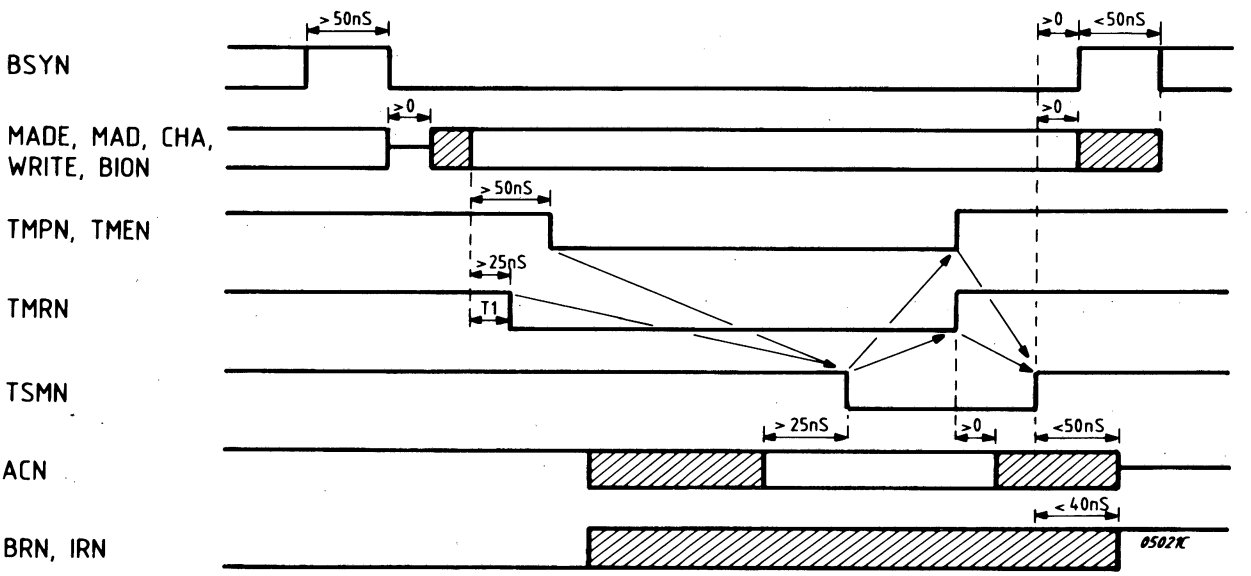


Figure 1.5b SLAVE TO MASTER TIMING

1.6 RECOMMENDED STANDARD INTERRUPTS

	LEVEL HEX	LEVEL DEC	INTERR. CONTROL ADDRESS HEX	SOURCE
INTERNAL (FIXED)	0	0	0	PF/AR
	1	1	2	LKM or Stackoverflow i.e. (A15) less than /100
	2	2	4	RTC
	3	3	6	Control Panel
EXTERN	4	4	8	* Spare (Temporary: memory error)
	5	5	A	* Spare
	6	6	C	
	7	7	E	
	8	8	10	
	9	9	12	
	A	10	14	
	B	11	16	
	C	12	18	
	D	13	1A	
	E	14	1C	
	F	15	1E	
	10	16	20	
	11	17	22	
	12	18	24	
	13	19	26	
	14	20	28	
	15	21	2A	
	16	22	2C	
	17	23	2E	
	18	24	30	
	19	25	32	
	1A	26	34	
	1B	27	36	
	1C	28	38	
	1D	29	3A	
	1E	30	3C	
	1F	31	3E	

Table 1.2 INTERRUPTS

* Note: Not standard on P871/4/6.

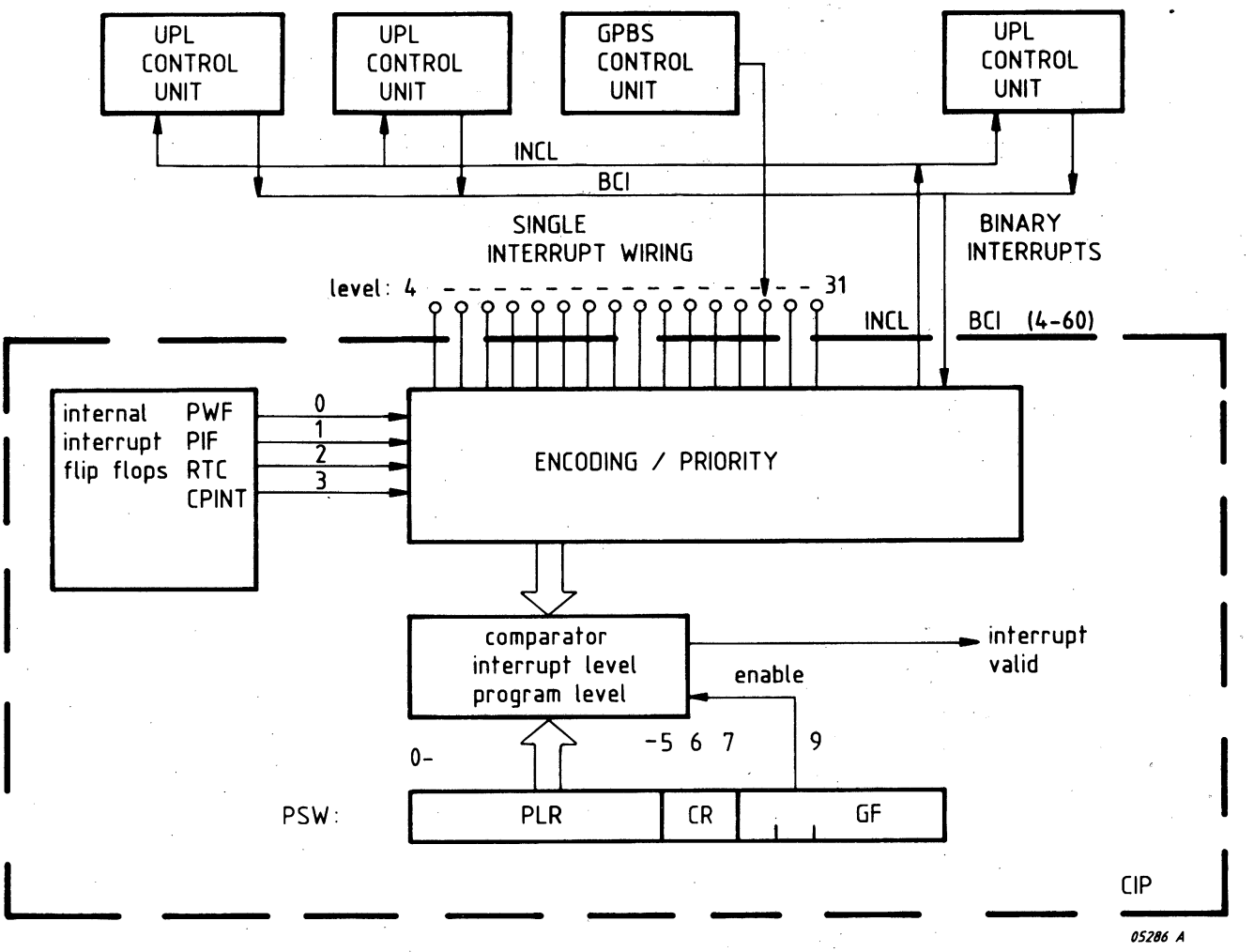
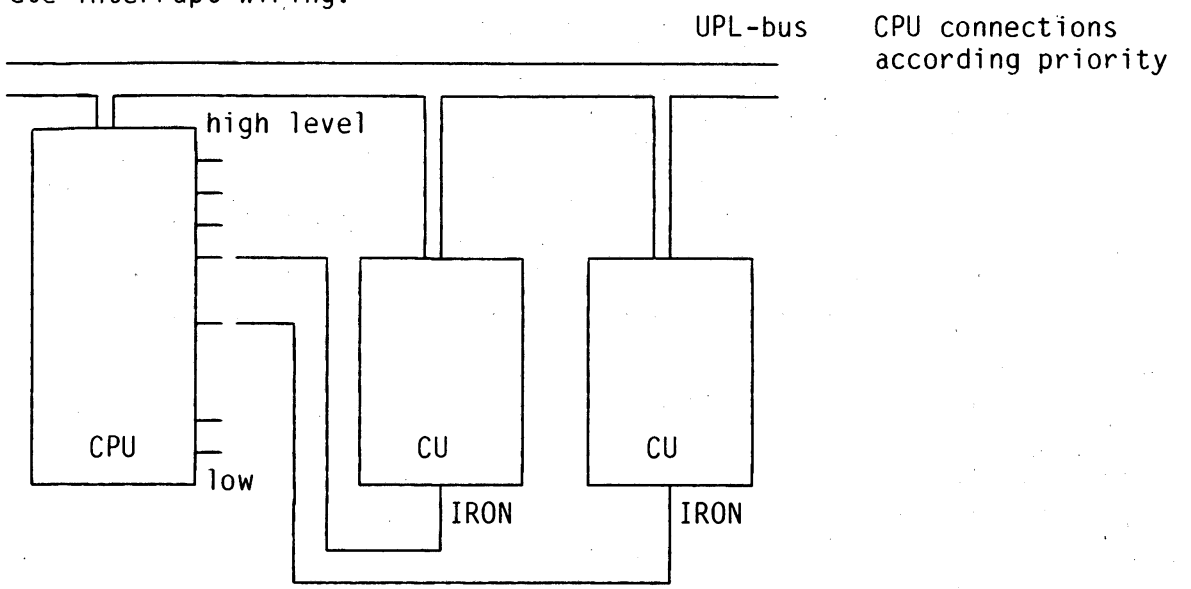


Figure 1.6 INTERRUPT SYSTEM

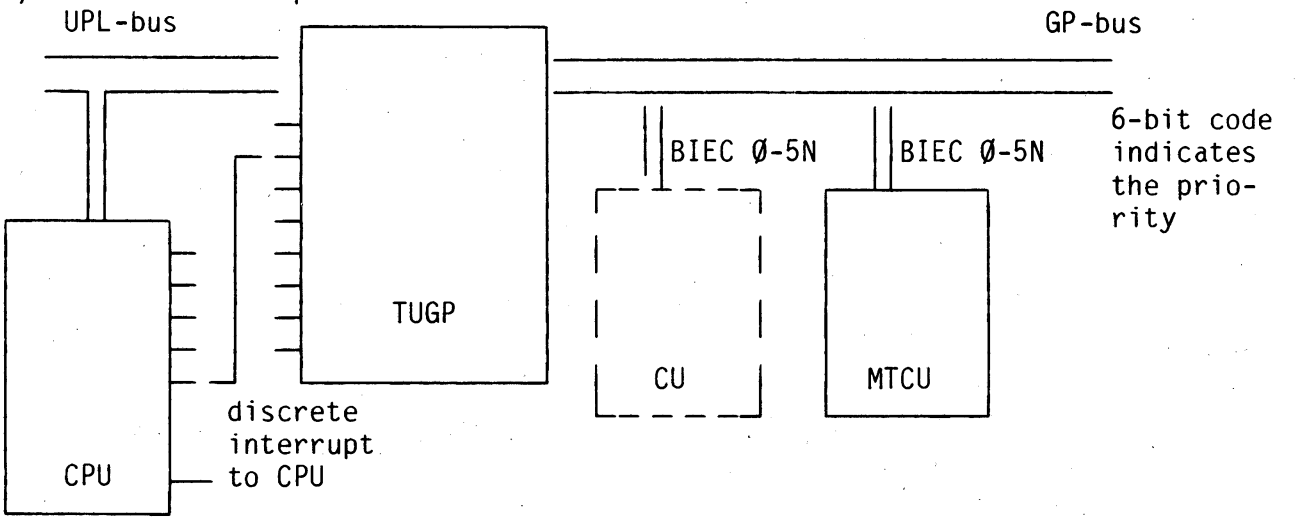
Interrupt Acceptance:
- Store P (return address) ┐
- Store PSW (save condition register) ├ STACK
- Update A15 (for possible next interrupt) ┘
- Inhibit for further interrupts
- PLR updated
- P loaded with the start address of the interrupt routine
- User to system mode

Interrupt Transport Modes

1) Discrete interrupt wiring:



2) Encoded interrupt on bus:



3) Binary coded interrupts on serial line:

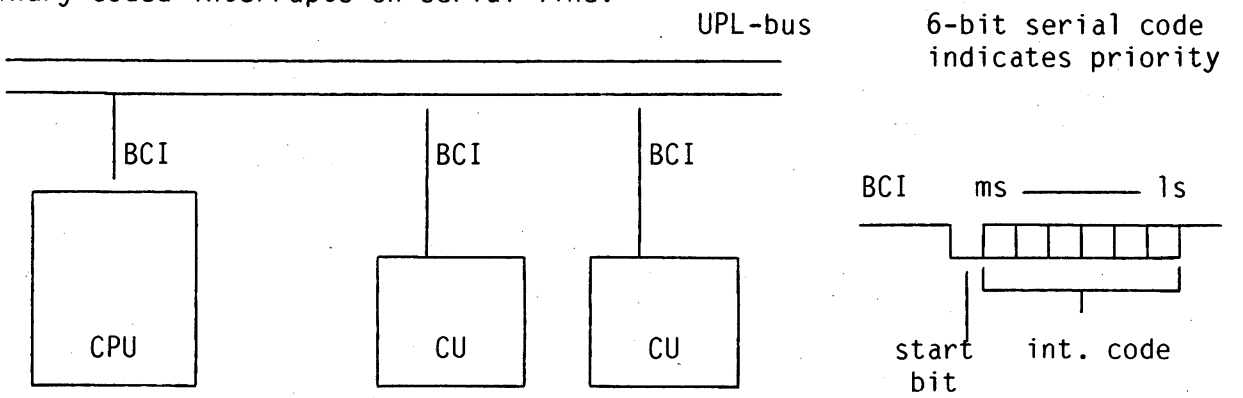


Figure 1.7 INTERRUPT TRANSPORT MODES

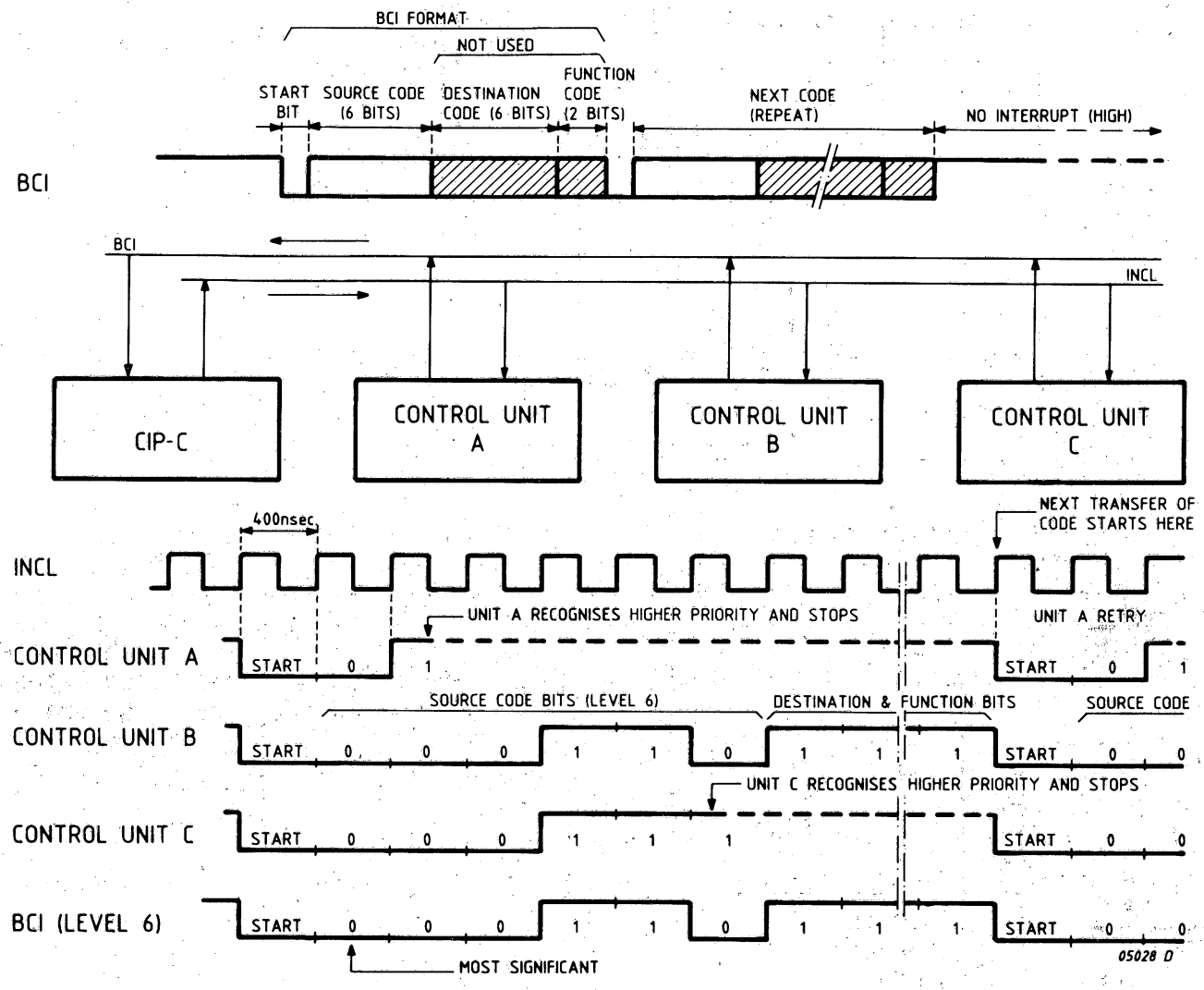


Figure 1.8 SERIAL INTERRUPTS - PRINCIPLE OF OPERATION

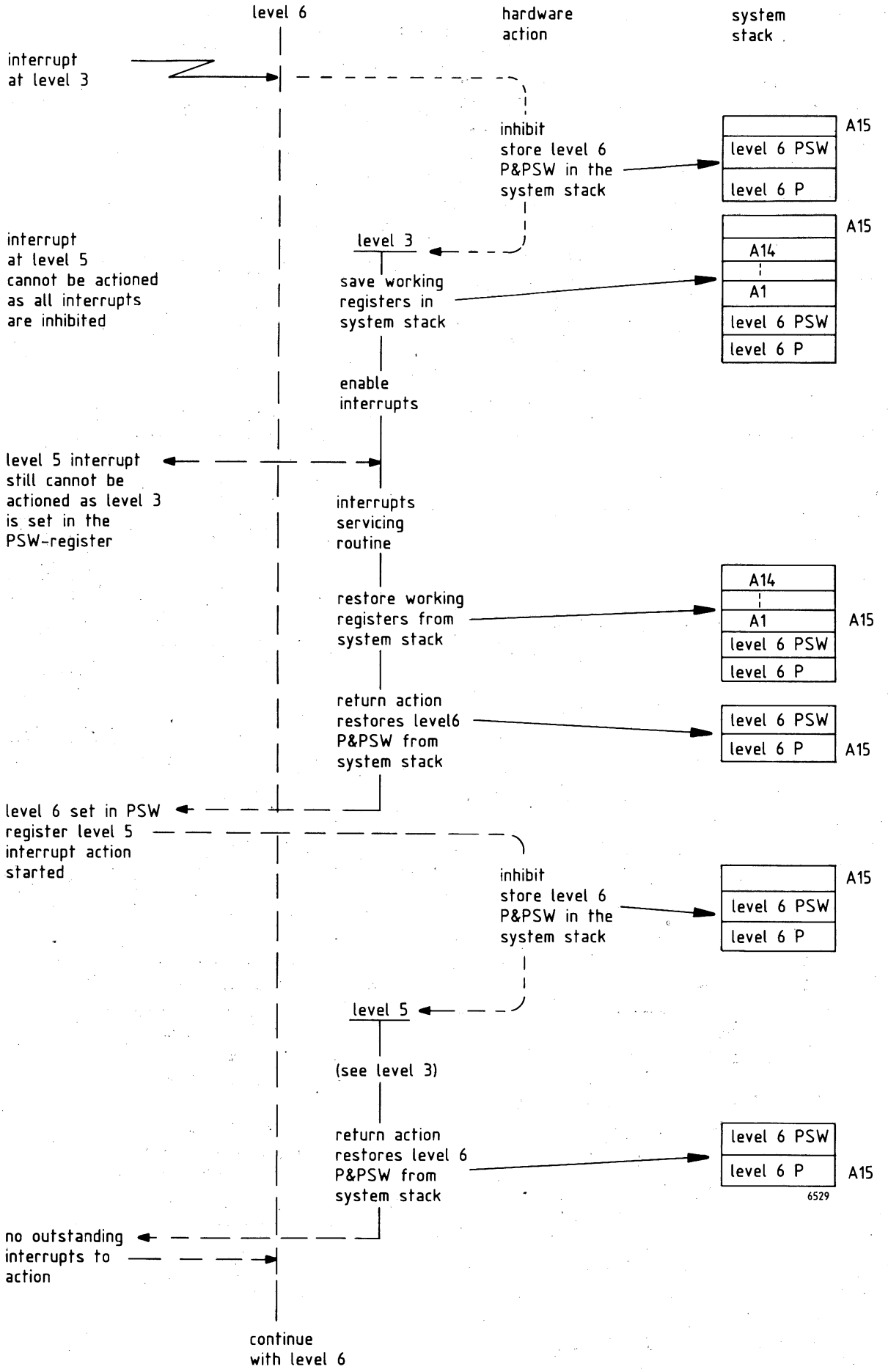


Figure 1.9 INTERRUPT SEQUENCE

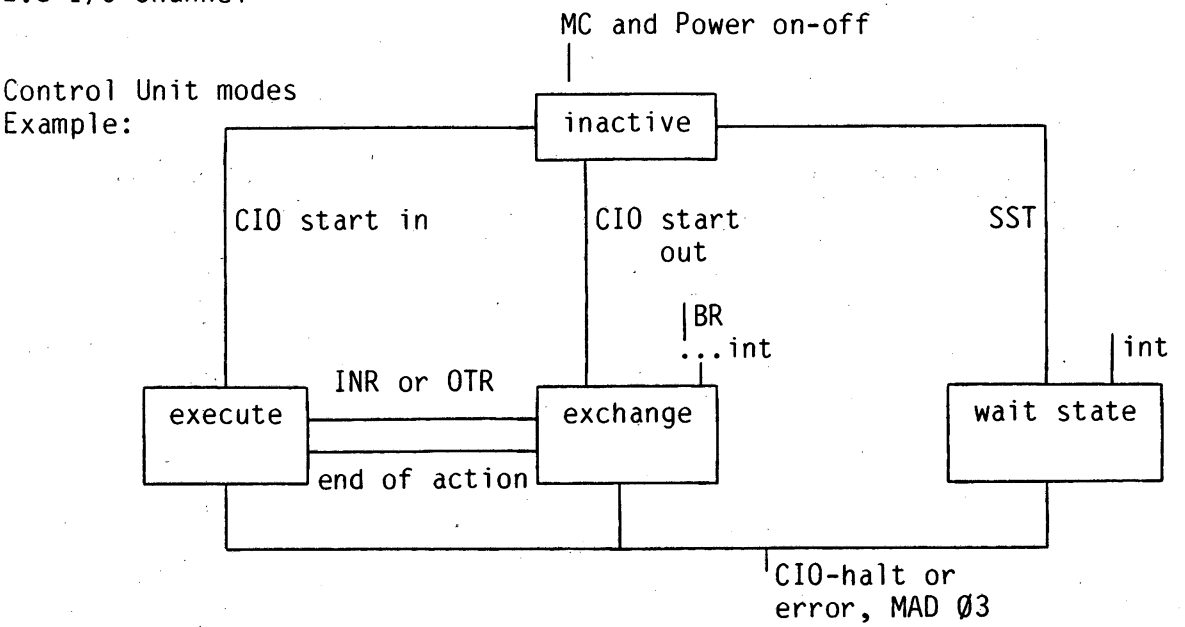
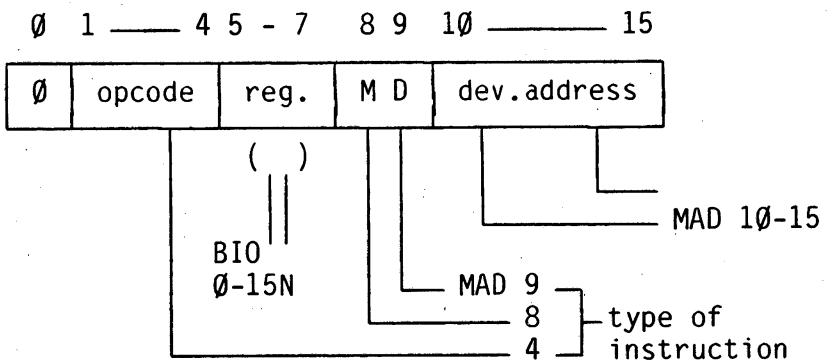


Figure 1.10 CONTROL UNIT MODES

I/O Instruction Format



Instruction		4	8	9	
MAD Lines	Ø3	Ø4	Ø8	Ø9	Accepted in mode
CIO start	Ø	Ø	1	1	Inactive
CIO stop	Ø	Ø	1	Ø	Always
INR (Input Transfer)	Ø	1	Ø	Ø	Exchange
OTR (Output Transfer)	Ø	Ø	Ø	Ø	Exchange
TST (Test Status)	Ø	1	1	Ø	Always
SST (Send Status)	Ø	1	1	1	Wait state
INR (last) IOP	1	1	Ø	Ø	Exchange
OTR (last) IOP	1	Ø	Ø	Ø	Exchange

CR reflects acceptance by TSMN and ACN:
- Ø Ø = accepted
- Ø 1 = not accepted
- 1 1 = Dev. addr. not recognised

Figure 1.11 I/O INSTRUCTIONS

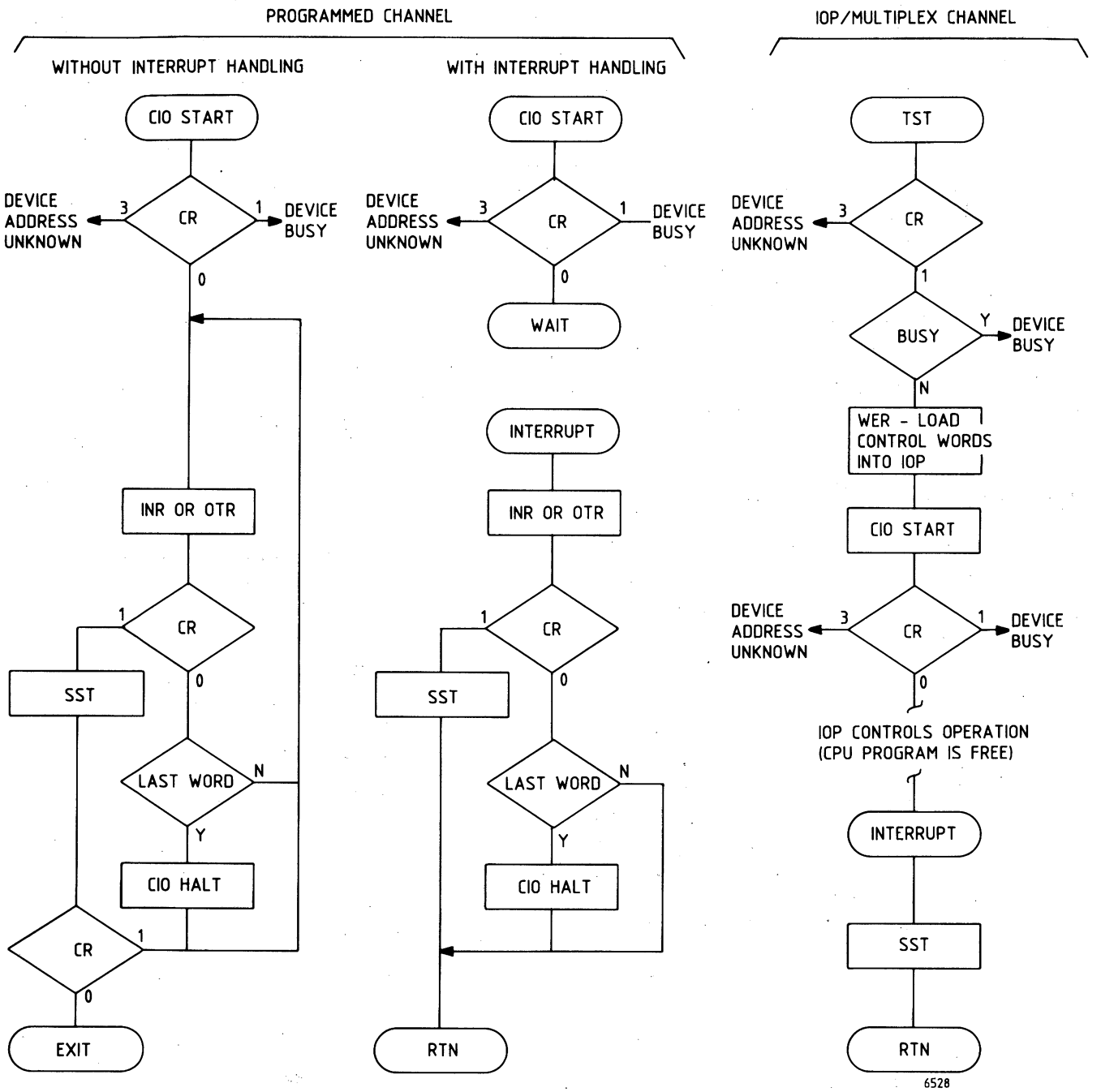


Figure 1.12 CHANNEL PROGRAMMING SEQUENCE

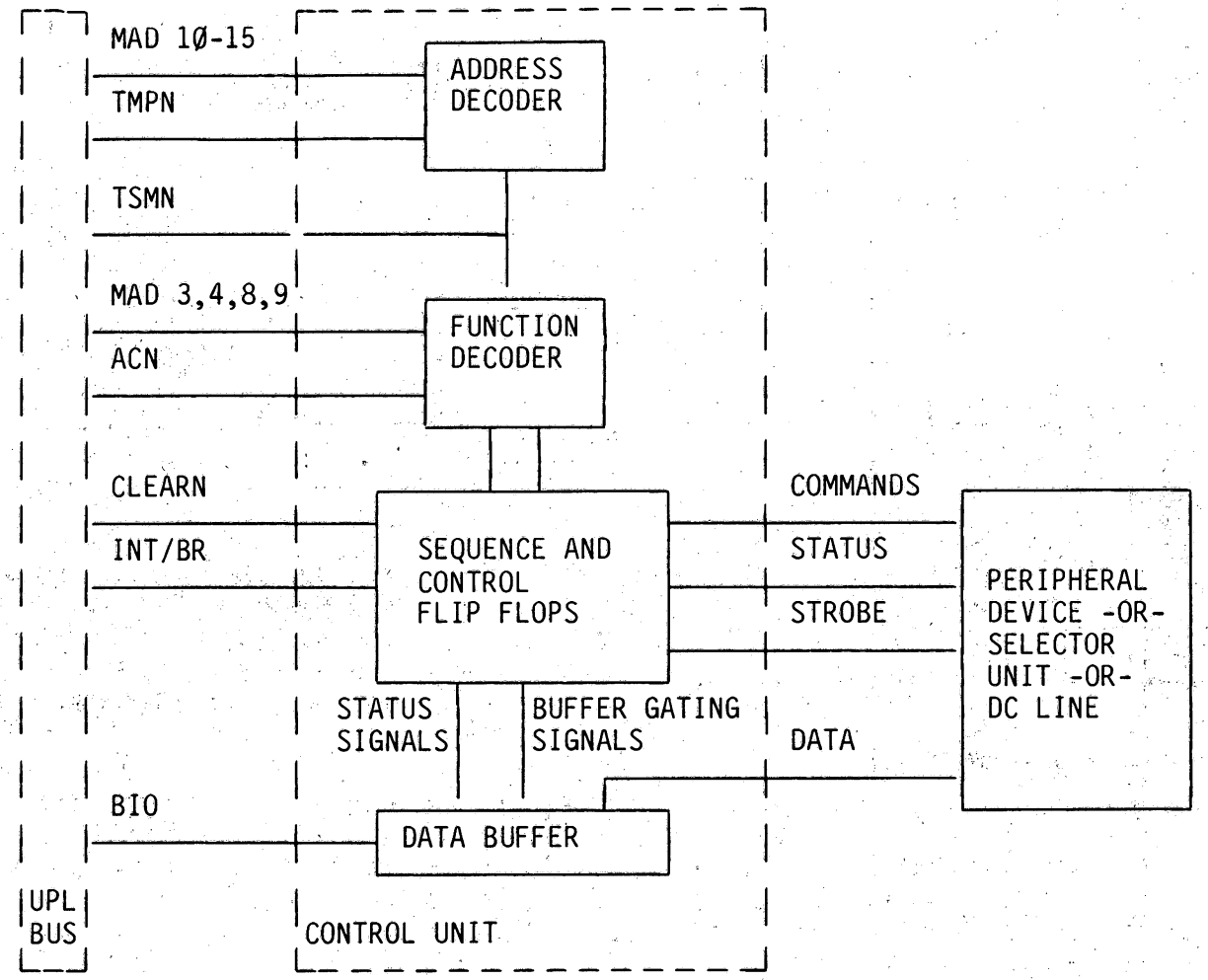
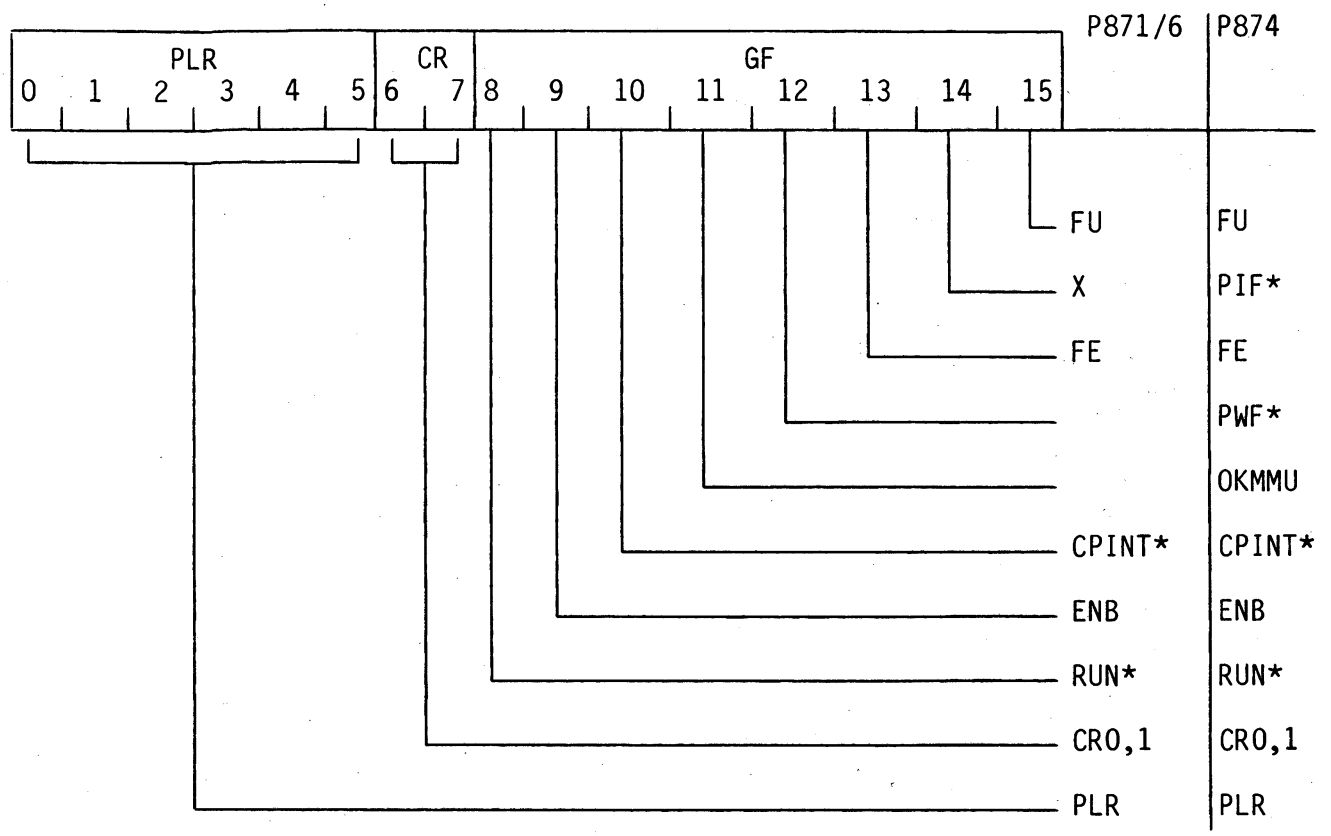


Figure 1.13 BLOCKDIAGRAM OF TYPICAL CONTROL UNIT



FE : Extended System Mode
FU : User Mode
RTC : Real Time Clock
PWF : Power Failure Interrupt
CPint : Control Panel Interrupt
ENB : Interrupt ENable
RUN : CPU in RUN Mode
CR : Condition Register
PLR : Program Level Register
PIF : Program Interrupt, Stack Overflow**

* These bits are not displayable (blanked in microprogram).

P876: Bit 10, when displayed with Control Panel Function "RST", this bit means Cache Memory Enabled (1) or disabled (0).
P871: Bit 10 is single step instruction indicator.

CRO,1:

CRO CR1	ARITHMETIC	COMPARE	I/O
00	Zero	Equal	Accepted
01	Positive	Greater	Not Accepted
10	Negative	Less	--
11	Overflow	--	Device Address Unknown

** Stackoverflow if (A15) smaller than /100.

Figure 1.14 PROGRAM STATUS WORD OLD/NEW

1.10 TRAPS

In case the CPU detects either an unknown instruction code or a priviledged instruction in USER mode, the CPU will jump to the TRAP routine.
Actions executed by the CPU are slightly different from an interrupt:

- store P (here: address of the 'wrong' instruction) ┐
- store PSW (save condition register) ├ STACK
- update A15 (for possible interrupt) ┘
- INHibit for interrupts
- USER to SYSTEM mode
- P loaded with the start address of the TRAP routine.

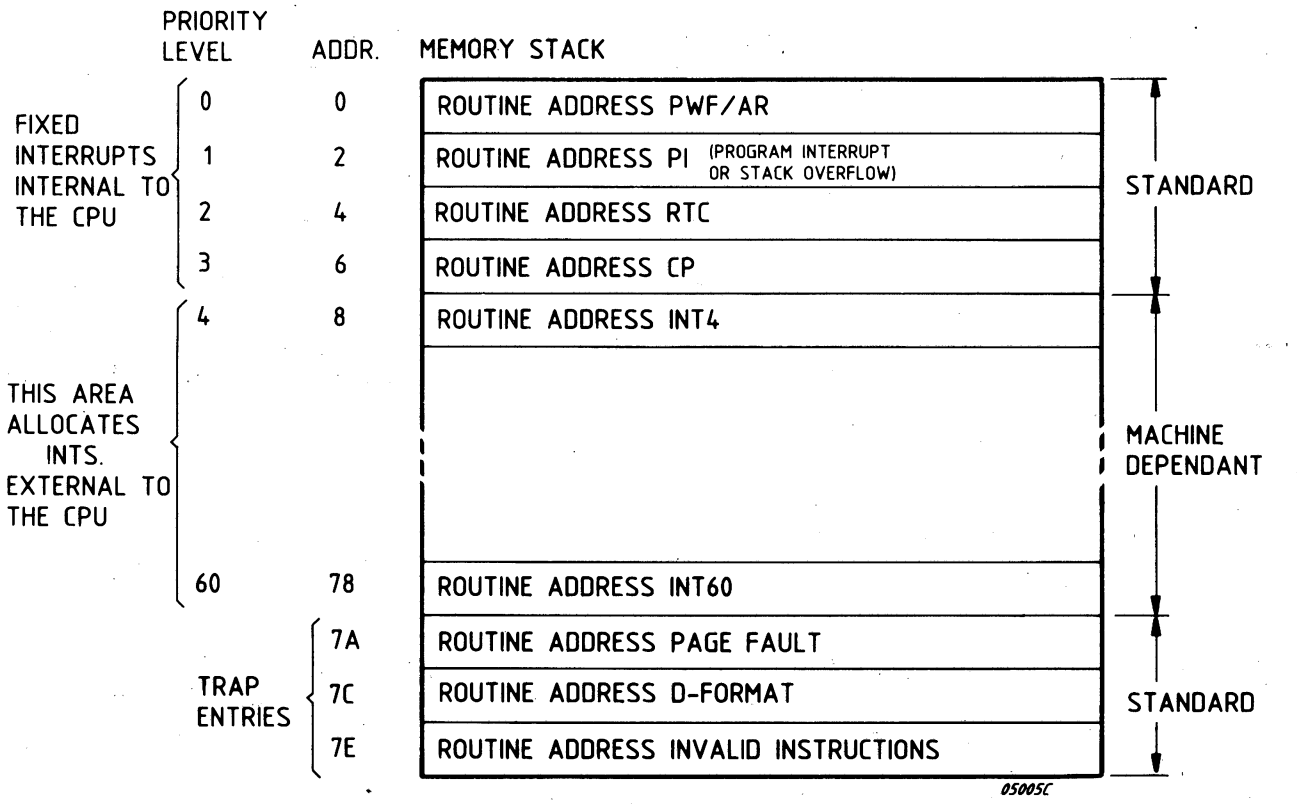
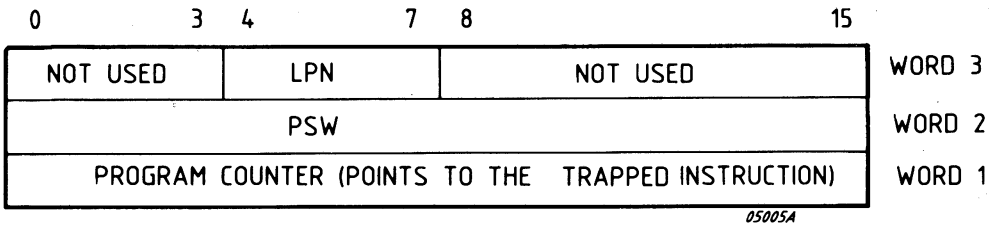


Table 1.3 INTERRUPT/TRAP ENTRIES

The Trap mechanism is similar in principle to the interrupt system except that when it is activated it does not take in account the PLR content or whether the CPU is in Enable/Inhibit interrupt mode. The CPU activates the Trap mechanism when the following conditions occur:

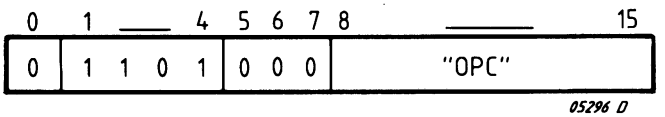
- Page Fault (Memory access fault) - generated by the CPU when in User Mode, the MMU has indicated to the CPU that a Page Fault has occured.
  In addition to P and PSW contents, a third parameter is saved in the System Stack in the following format:



  LPN = Logical page Number, on which the page fault was detected.

  The Program Counter is loaded with the contents of address /7A.

- Not wired instruction in D-format -
  The D-format instructions (Character String and Decimal instructions) have the following format:



  The instruction is trapped when "OPC" is invalid (not implemented).
  This trap may be used for software simulation of not implemented instructions.
  Program Counter is loaded with the contents of address /7C.

- Invalid Instruction:
  This trap is caused by any abnormal instruction which is not of the D-format:
  Not recognised instruction codes.
  Privileged instructions in USER-mode (e.g. HLT, I/O-instruction, ENB, INH).
  System stack access (register A15) in USER-mode.

  Program Counter and PSW are saved in the stack.

  The Program Counter is loaded with the contents of address /7E.

Note that in case of a Trap the old P-contents, pointing to the trapped instruction is pushed on the stack.

1.11 INITIAL PROGRAM LOADER (FIGURE 1.15)

The Initial Program Loader (IPL) is responsible for system initiation by enabling the eventual loading of an Object Program. For purposes of this description the IPL Sequence to load from a Sequential Device is described in 3 parts:

. Bootstrap
. Low Core IPL
. High Core IPL

BOOTSTRAP

The Bootstrap is contained in the Bootstrap ROM in the CPU in a format 1k x 4bits. The CPU assembles this format into 256 x 16-bit words which are loaded into Memory starting from 000. The CPU loads the IPL parameters (keyed in on Control Panel) into Register A15. The Bootstrap enables the loading of the Low Core IPL, from the peripheral addressed in A15.

LOW CORE IPL

The Low Core IPL has 3 principal functions:

. Calculates the size of Memory and subtracts 400 characters to find the High Core start address.
. Loads High Core IPL.
. Starts High Core IPL.

HIGH CORE IPL

The High Core IPL has 3 principal functions:

. The IDENT name of the program to be printed out on the console typewriter.
. Loads the Object Program starting from address 000.

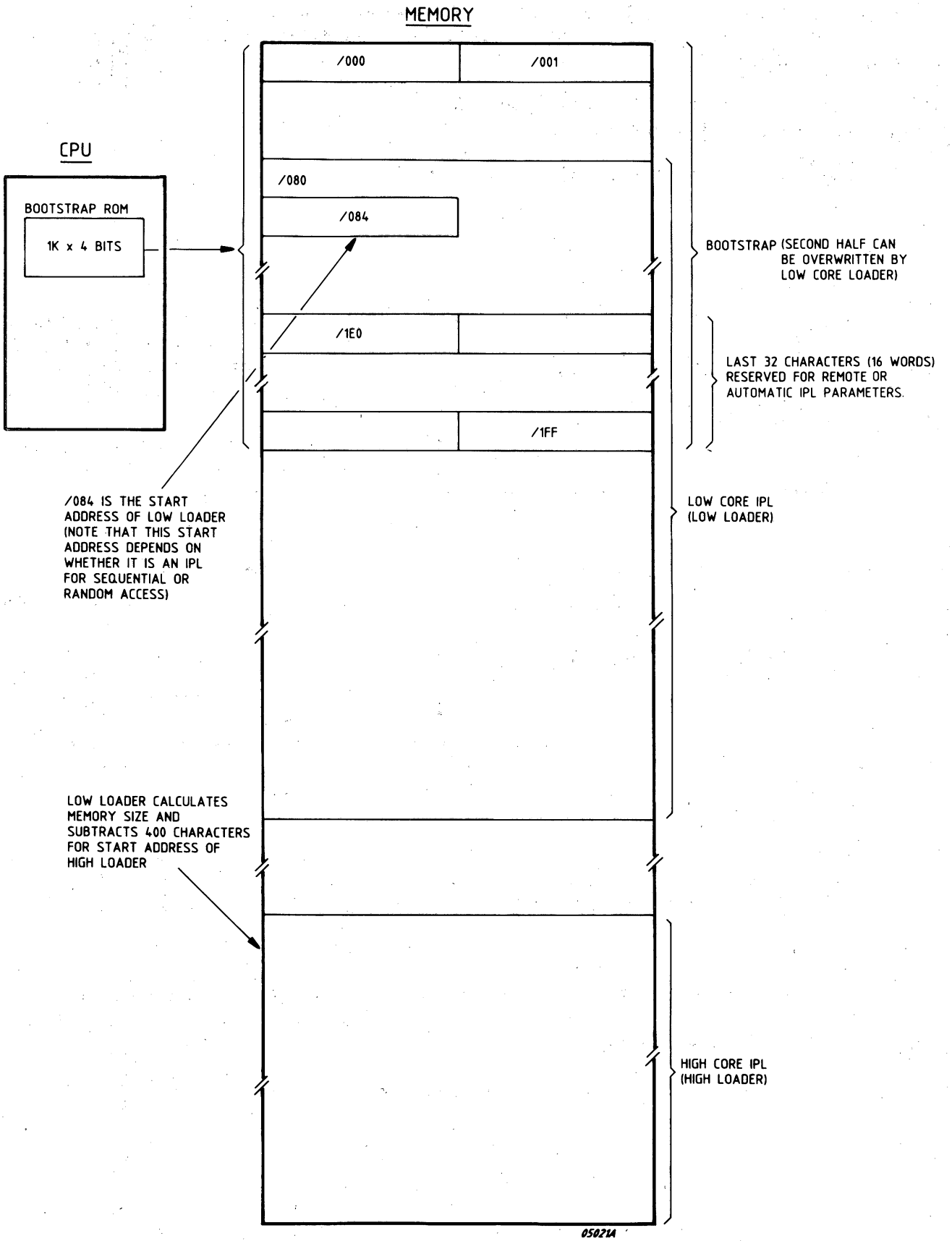


Figure 1.15 INITIAL PROGRAM LOADER - PRINCIPLE

1.12 REMOTE IPL

The last 16 words of the Bootstrap (addresses 240-255 (/1E0 to /1FF) inclusive) contain parameters for up to 16 remote devices. The system enables operation in one of two modes:

. Address is selected by card links OPSON-3N.
. Remote Device sends its own address, no links selected.

The parameter from the selected address will be loaded into A15.

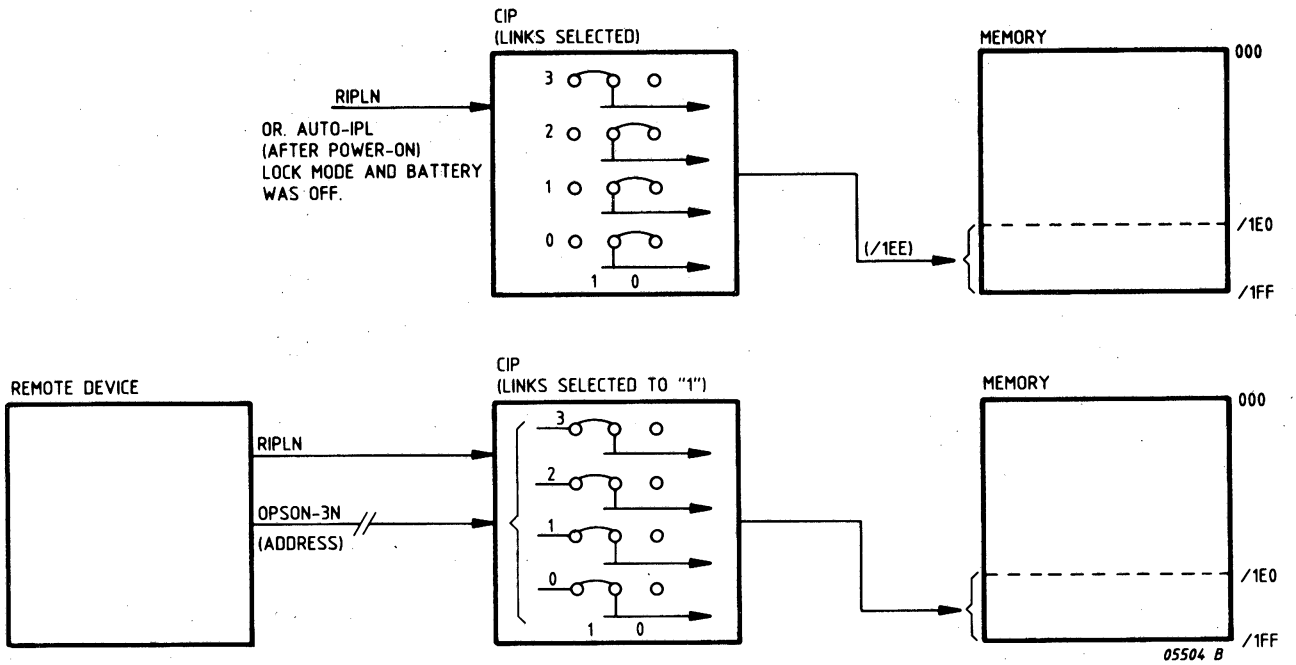


Figure 1.16 REMOTE IPL CP2B/CP1BF

The same hardware is used for AUTOMATIC IPL.
AUTOMATIC IPL is done after POWER-ON in LOCK-mode, only if the memory contents was not maintained by BATTERY supply (AUTOMATIC RESTART of the program is done when memory contents was maintained).

Note: The 4 U-links must be removed on the C7E2 (P874) if not selected.

1.13 STANDARD DEVICE ADDRESSES

Device connected to: Single Device Controllers		
Console Typewriter		/10 (FIXED)*
LP		/07
Device connected to: Multiple Device Controllers		
X1215 Disc	Drive 0 cartridge	/02
	fixed	/22
	Drive 1 cartridge	/12
	fixed	/32
X1216 Disc	Drive 0 cartridge	/01
	fixed	/21
	Drive 1 cartridge	/11
	fixed	/31
Flexible Disc	Drive 0	/03
	Drive 1	/13
	Drive 2	/23
	Drive 3	/33
Magnetic Tape	Drive 0	/04
	Drive 1	/14
	Drive 2	/24
	Drive 3	/34

* Note: DEVICE ADDRESS /10 only and always to be used for integrated Control Unit on CPU boards CP1BF and C7E2/C7E1 (P871, P874).

Table 1.4 STANDARD DEVICE ADDRESSES

```
00000                    IDENT    BOOBIG                82-05-12
00001  *
00002  *     BOOBIG SUPPORT NEW BIG DISC CONTROLLERS  BIGD2 AND FOLLOWING
00003  *     CDC BIG DISC CONTROL UNIT
00004  *
00005  *
00006  *        PROM      04063
00007  *
00008  *  BOOTSTRAP  256*16 BITS
00009  *             CONTENTS THE DISC AND SEQUENTIAL BOOTSTRAP
00010  *                          ROM  AND SEQUENTIAL BOOTSTRAP
00011  *
00012  *             ALLOWS MOREOVER IPL FROM    MINI FIXED DISK X1250
00013  *                                         FLOPPY DISK 1MB
00014  *                                         IPLRZ CARD
00015  *                                         REMOTE IPL ( ALCUZ , HLCUZ )
00016  *                                         FIXED HEAD DISK DDC
00017  *
00018  *            AND ALSO BY USE OF ONE OF THE LAST 64 WORDS OF BOOTSTRAP
00019  *                AS VALUE OF REGISTER A15
00020  *                                         AUTOMATIC IPL
00021  *                                         AUTOMATIC RE-IPL (BATTERY OFF)
00022  *
00023  *
00024                    EJECT
00025  *        THE CONFIGURATION OF REGISTER A15 IS AS FOLLOWS :
00026  *
00027  *        BITS
00028  *
00029  *        0=1                    INDICATES THE CU READING 16 BITS WORDS
00030  *                               WHEN IT IS CONNECTED ON PROGRAMMED CHANNEL
00031  *                               (FOR EX    FLOPPY DISK )
00032  *
00033  *        1=1                    DISK ON IOP OR PROGRAMMED CHANNEL
00034  *        THEN  3=1              PROGRAMMED CHANNEL
00035  *              3=0              IO PROCESSOR
00036  *              2=1              MOVING HEADS
00037  *              2=0              FIXED HEADS
00038  *
00039  *        1=0                    OTHER CASES
00040  *        THEN  2=1              ROM IPL OR DMA
00041  *              THEN    3=1      ROM IPL
00042  *                               3=0 ; 0=1 ; 9=1  DMA UPL WITH CIO IPL
00043  *                               3=0 ; 0=1 ; 9=0  FREE
00044  *                               3=0 ; 0=0 ; 9=0  BIGD2
00045  *                               3=0 ; 0=0 ; 9=1  NEW CU BIG DISC
00046  *                                                NOT YET SPECIFIED
00047  *
00048  *              2=0              SEQUENTIAL DEVICES OR CDC DISK
00049  *
00050  *              2=0              SEQUENTIAL DEVICES
00051  *                    3=1        PROGRAMMED CHANNEL
00052  *                    3=0        IO PROCESSOR
00053  *
00054  *        9                      NOT SIGNIFICANT FOR BOOTSTRAP
00055                                 BUT MUST BE SET FOR MOVING-HEAD DISKS
00056                                 WITH ABSOLUTE SEEK
00057                                 USING IPL OF X1215/1210 DISK
00058  *
00059  *        4 TO 7                BIO LINES FOR CIO START
00060  *                  -  0111           FOR K7
00061  *                  -  1010           FOR MT
00062  *                  -  0001           FOR BIG DISC WITH CIO IPL
00063  *                  -  0000           SECTOR # CONTAINING IPL
00064  *                                    FOR FLOPPY 1/4 MB
00065  *                                          FHD
00066  *                                          X1250
00067  *                                          FLOPPY 1 MB
00068  *                     - INTERLACE = SECTOR #   CONTAINING IPL
00069  *                                   FOR X1250 /X1216
00070  *                                   - 0000
00071  *                     - 0000        FOR PAPER TAPE
00072  *                                   FOR IPLRZ
00073  *                     - BITS 4,5,6 = SECTOR # OF IPL      *
00074  *                       BIT 7 = 0     MOVABLE PART       * FOR BIGD2
00075  *                             7 = 1   FIXED PART         *
00076  *
00077  *
00078  *     8=1                       MULTI DEVICE CONTROLLER
00079  *     8=2                       SINGLE DEVICE CONTROLLER
00080  *     10 TO 15                  DEVICE ADDRESS
00081  *
```

```
00082                           EJECT
00083                  *
00084                  *        DESCRIPTION
00085                  *
00086                  *        NEWB10 LOADS THE IPL ( OR THE FIRST RECORD OF IPL )
00087                  *                AT ADDRESS IPLADD
00088                  *        THEN STARTS IT
00089                  *        LOADING ADDRESS + 4 GIVEN TO THE IPL IN A14
00090                  *        FOR DISC LIKE DEVICE THE RECORD IS SECTOR # (PHYSICAL SECTOR #
00091                  *        SPECIFIED BY MEANS OF BIO LINES )
00092                  *                              THE LENGTH IS LENGTH OF A X1215 SECTOR (205 WORDS)
00093                  *                                           OR LENGTH OF A FLOPPY SECTOR (64 WORDS)
00094                  *
00095                  *                                                        ( OR 128 WORDS )
00096                  *        FOR SEQUENTIAL DEVICES LENGTH IS IPLLEN CHARACTERS
00097                  *                                        LEADING CHARACTERS ARE IGNORED
00098                  *
00099                  *        FOR CDC DISK THE IPL SECTOR IS READ ON LOCATION 0
00100                  *                BRANCH TO IPL BEGINNING IS PERFORMED IN THE
00101                  *                FOLLOWING WAY : WHEN LOADING THE IPL INTO
00102                  *                MEMORY, THE BOOTSTRAP LOOPS AT ADDRESSES /7A-/7C
00103                  *                BUT AT THE SAME LOCATIONS THE IPL CONTAINS A BRANCH
00104                  *                TO ADDRESS /0000, WHICH WILL OVERWRITE THE BOOTSTRAP
00105                  *                LOOP.
00106                  *
00107                  *        FOR ROM IPL THE NEWBOO BRANCHS TO THE FIRST NOT NULL ROM
00108                  *                LOCATION AFTER /202
00109                  *
00110                  *        FOR DMA UPL SPECIAL BLOCKS ARE ALREADY PROVIDED , A SPECIAL
00111                  *                SEQUENCE PERFORMS CIO IPL AND STARTS LOADED IPL
00112                  *                AT ADDRESS SPECIFIED AT PREMARK TIME.
00113                  *                DIRECTLY ADDRESSABLE : IMPLAN
00114                  *                (ACTUALLY THE ADDRESS GIVEN AT PREMARK IS THAT
00115                  *                OF THE LAST LOCATION DIRECTLY ADDRESSABLE :
00116                  *                E.G. FOR 32K MEMORY, 'IMPLAN' = /FFFE )
00117                  *                IPL IS STARTED DIRECTLY AT LOADING ADDRESS.
00118                  *
00119                  *
00120                  *
00121                  *        THAT VERSION OF BOOTSTRAP IS COMPATIBLE WITH EXISTING IPL
00122                  *        SO      - IPLADD = LOADING ADDRESS OF IPL = /80
00123                  *                - IPLLEN = LENGTH OF A RECORD FOR = /50
00124                  *                           SEQUENTIAL DEVICES
00125                  *                - SOME PART OF CODING USE BY SOME IPL MUST BE
00126                  *                  AT THE SAME PLACE
00127                  *
00128                  IPLADD  EQU     /80                 LOADING ADDRESS OF IPL
00129                  IPLLEN  EQU     /50                 LENGTH OF A RECORD FOR
00130                                                       SEQUENTIAL DEVICES
00131                  *
00132                  *
00133                           EJECT
00134                           AORG    0
00135                  BOOT     EQU     *
00136  0000  5700  F            RF      BOOT00
00137                           EJECT
00138                  *
00139                  *        SOME IPL ( FOR K7 , PTR , FLOPPY 1/4 MB )
00140                  *        USE A PART OF BOOTSRAP TO LOAD FURTHER RECORDS OF IPL
00141                  *        TO BE COMPATIBLE WITH THEM
00142                  *        SOME INSTRUCTIONS MUST BE AT THE SAME ADDRESS AS IN PREVIOUS
00143                  *        BOOTSTRAPS
00144                  *                AT /3E      LDKL  A5,/80CD
00145                  *                AT /42      WER   A5,0
00146                  *                AT /5A      RF(4) INR10
00147                  *
00148                  *        MOREOVER THE LOADING ADDRESS OF IPL MUST BE /80
00149                  *        SO THE PART OF BOOTSRAP WHICH LOADS THE IPL
00150                  *        MUST BE LOADED BEFORE /80
00151                  *
00152                  *        REGISTERS
00153                  *
00154                  *        (A1)  =  REGISTER OF CIO START
00155                  *        (A2)  =  INR INST. ADDRESS
00156                  *        (A3)  =  CIO INST. ADDRESS
00157                  *        (A4)  =  SST INST. ADDRESS
00158                  *        (A5)  =  REMAINING # OF CHARACTERS (WORDS) TO BE READ ( PC )
00159                  *                 OR FIRST MULTIPLEX WORD ( IOP )
00160                  *        (A6      CURRENT ADDRESS OF CHARACTER (WORD) TO BE READ ( PC )
00161                  *                 OR SECOND MULTIPLEX WORD ( IOP )
00162                  *        (A7)  =  REGISTER OF INR OR SST
00163                  *        (A8)  =  START ADDRESS OF IPL
00164                  *        (A9)  =  FLAG USED IN PC. TO IGNORE LEADING CHARACTERS
00165                  *        (A10) =  NOT USED
00166                  *        (A11) =  NOT USED
00167                  *        (A12) =  LOADING ADDRESS OF UPL PART OF BOOTSTRAP
00168                  *                 OR LOADING ADDRESS OF IPL BIG DISC WITHOUT CIO IPL
00169                  *        (A13)    USED IF UPL
00170                  *        (A14)    NOT USED
00171                  *        (A15)    INPUT REGISTER OF BOOTSTRAP
00172                  *
00173                  *
00174                  *
00175                  SSTCP    EQU     *                  SST FOR PROGRAMMED CHANNEL
00176  0002  F031               EXR*    A4                 LOOP  SST / INR
```

```
00177  0004  5400  F           RF(4)     INR
00178                    TSTSTA   EQU      *
00179  0006  A720              ANKL      A7,/4207
       0008  4207
00180                                                    13 =DATA FAULT
00181                                                    14 =THROUGHPUT ERROR
00182                                                    15 =NOT OPERABLE
00183  000A  5400  F           RF(4)     NEWIO
00184                                                THEN START BOOTSTRAP AGAIN
00185                                                FROM THE VERY BEGINNING.
00186                    BRANCH   EQU      *
00187  000C  8F02              ABR       A8                    BRANCH TO IPL
00188                    *
00189                    *
00190                    *
00191                    *
00192                    *        IO BLOCK OF COMMANDS FOR BIGD2 CONTROL UNIT
00193                    *
00194  000E  E000        BIGD20   DATA      /E000              SEEK TO ZERO
00195  0010  0800        BIGD21   DATA      /800               BIT 4 = 1 TO GET INTERRUPT
00196                                                          BITS 5 TO  10 = SECTOR #
00197                                                          BITS 11 TO 15  = HEAD #
00198  0012  00CD        BIGD22   DATA      /CD                TOTAL LENGTH
00199  0014  00CD        BIGD23   DATA      /CD                PARTIAL LENGTH
00200  0016  0000        BIGD24   DATA      0                  BUFFER ADDRESS MOST SIGNIF. BITS
00201  0018  0000        BIGD25   DATA      0                  BUFFER ADDRESS LEAST SIGNIF. BITS
00202                    *
00203                    *        IO BLOCK OF COMMANDS FOR FURTHER BIG DISC CONTROL UNIT
00204                    *
00205  001A                       RES       5
00206                    TSTA     EQU       *
00207  0024  A720                ANKL      A7,/4207             IF STATUS CORRECT
       0026  4207
00208  0028  5000  F             RF(0)     CIOSTA                  EXECUTE CIO START
00209                    NEWIO    EQU       *
00210  002A  871E                LDR       A7,A15
00211  002C  3FC1                SLC       A7,1                 DISK ?
00212  002E  5600  F             RF(6)     SEQUEN               NO : SEQUENTIAL OR CDC
00213                    *
00214                    *
00215                    *
00216                              AORG      /30
00217                    DISK     EQU       *                    DISK ON IOP OR PC
00218  0030  3FC1                SLC       A7,1                 MOVING HEADS ?
00219  0032  5600  F             RF(6)     NOSEEK               NO                              3A
00220  0034  0103                LDK       A1,3                 YES : PERFORM A CIO             3C
00221  0036  41C0        CIO      CIO       A1,1,0               SEEK TO CYLINDER 0
00222                    *
00223                    *  PREPARE NEXT IO ON DISK
00224                    *
00225                    NOSEEK   EQU       *
00226  0038  811E                LDR       A1,A15               GET                             40
00227  003A  3966                SRL       A1,6                 SECTOR #                        42
00228  003C  213C                ANK       A1,/3C               IN A1                           44
00229  003E  8520                LDKL      A5,/80CD             READ  205 (/CD) WORDS           46
       0040  80CD
00230                    *
00231                    * EXECUTE WER INSTRUCTIONS , WHATEVER THE CHANNEL IS
00232                    *
00233                    SEQUEN   EQU       *
00234                    WER1     EQU       *
00235  0042  7500                WER       A5,0                 INIT LENGTH OF THE BUFFER       4A
00236                    WER2     EQU       *
00237  0044  7601                WER       A6,1                 INIT LOADING ADDRESS            4C
00238                    DMACDC   EQU       *
00239  0046  F031                EXR*      A4          SST                                      4E
00240  0048  5826                RB(0)     TSTA                 TEST STATUS BEFORE CIO START
00241                    CIOSTA   EQU       *
00242  004A  F02D                EXR*      A3          CIO                                      50
00243  004C  5C08                RB(4)     DMACDC               52
00244  004E  871E                LDR       A7,A15                                               54
00245  0050  3F43                SLL       A7,3                                                 56
00246  0052  5600  F             RF(6)     SST                  MULTIPLEX
00247                    *
00248                    *   PROGRAMMED CHANNEL
00249                    *
00250                    *        IF A9=A5 IGNORE LEADING CHARACTERS
00251                    INR      EQU       *
00252  0054  4F00                INR       A7,0,0      READ ONE CHAR                            5C
00253  0056  5C56                RB(4)     SSTCP       EXECUTE SST                              5E
00254  0058  E994                CWR       A9,A5       LEADING  CHAR ?                          60
00255  005A  5400  F             RF(4)     INR10       NO                                       62
00256  005C  871C                LDR       A7,A7       CHECK IF NULL                            64
00257  005E  580C                RB(0)     INR         YES : IGNORE                             66
00258                    *
00259                    INR10    EQU       *
00260  0060  879E                LDR       A15,A15     TEST IF CU 16 BITS ON PC.                68
00261  0062  5600  F             RF(6)     STORE       NO : 8+8                                 6A
00262                    *
00263  0064  8739                STR       A7,A6       STORE WORD                               6C
00264  0066  1601                ADK       A6,1        INCREMENT CHARACTER ADDR                 6E
00265                    STORE    EQU       *
```

```
00266  0068  E739            SCR     A7,A6       STORE CHARACTER                    70
00267  006A  1601            ADK     A6,1        NEXT  CHARACTER ADDR               72
00268  006C  1B01            SUK     A5,1        COUNT DONE ?                       74
00269  006E  5C1C            RB(4)   INR         NO                                 76
00270                *                            YES :CIO HALT
00271  0070  0700            LDK     A7,0
00272  0072  4780      HIO   CIO     A7,0,0
00273  0074  5700  F         RF      SST
00274                *
00275                *       FOR IPL FROM CDC LOOP UNTIL SST ACCEPTED AT @ /7A
00276                *
00277  0076                  RES     2
00278                         AORG    /7A
00279                SST      EQU     *
00280  007A  4FC0            SST     A7,0                LOOP UNTIL SST ACCEPTED
00281  007C  5C04            RB(4)   *-2
00282  007E  5F7A            RB      TSTSTA              TEST STATUS
00283                *
00284                *       /80     ADDRESS OF AWORD FOR UPL RESTART
00285                *
00286  0080  0000  F         DATA    HARD
00287                BOOT00   EQU     *
00288  0082  8720            LDKL    A7,/AAAA            PATTERN TO BE CHECKED
       0084  AAAA
00289  0086  84A0            LDKL    A12,/F800           STACK
       0088  F800
00290                BO0010   EQU     *
00291  008A  8733            STR     A7,A12
00292  008C  EF32            CWR*    A7,A12
00293  008E  5000  F         RF(0)   BO0020
00294  0090  9CA0            SUKL    A12,/1000
       0092  1000
00295  0094  5F0C            RB      BO0010
00296                BO0020   EQU     *                   MOVE BOOT UPL TO HIGH-CORE
00297  0096  8120            LDKL     A1,BASE+0           BEGIN OF BOOT
       0098  0000  F
00298  009A  8212            LDR     A2,A12
00299  009C  8320            LDKL    A3,LIMIT-BASE       LENGTH OF BOOT
       009E  0000  F
00300                BO0030   EQU     *
00301  00A0  8424            LDR*    A4,A1
00302  00A2  8429            STR     A4,A2
00303  00A4  1202            ADK     A2,2
00304  00A6  1102            ADK     A1,2
00305  00A8  1B02            SUK     A3,2
00306  00AA  590C            RB(1)   BO0030
00307                *
00308                *  BASE REGISTERS INITIALIZATION
00309                *
00310                INIT10   EQU     *
00311  00AC  0254            LDK     A2,INR              (A2) = INR @
00312  00AE  0336            LDK     A3,CIO              (A3) = CIO @
00313  00B0  047A            LDK     A4,SST              (A4) = SST @
00314                *
00315                *  GET DEVICE ADDRESS TO INITIALIZE THE  I/O COMMANDS
00316                *
00317  00B2  861E            LDR     A6,A15      A6 = KEYS VALUE                    6
00318  00B4  263F            ANK     A6,/3F      KEEP JUST DEVICE ADDRESS           8
00319  00B6  AE29            ORRS    A6,A2       INIT INR INST WITH DA              A
00320  00B8  AE2D            ORRS    A6,A3            CIO                           C
00321  00BA  AE41            ORS     A6,HIO           HIO
       00BC  0072
00322                *
00323                * GET CONTROLLER TYPE AND ADDRESS.
00324                *
00325  00BE  871E            LDR     A7,A15      MULTIPLE OR SINGLE                 12
00326  00C0  3FC8            SLC     A7,8        DEVICE CONTROLLER ?                14
00327  00C2  5600  F         RF(6)   INIT20      IF SINGLE BRANCH                   16
00328  00C4  260F            ANK     A6,/F       KEEP THE DEVICE CONTROLLER ADDRESS 18
00329                *
00330                * INITIALIZE THE WER INSTRUCTIONS AND SST ONE.
00331                *
00332                INIT20   EQU     *
00333  00C6  AE31            ORRS    A6,A4               SST INSTRUCTION            1A
00334  00C8  3E41            SLL     A6,1                CHANNEL AND SUBCHANNEL VALUES 1C
00335  00CA  AE41            ORS     A6,WER1             IN WER
       00CC  0042
00336  00CE  AE41            ORS     A6,WER2             INSTRUCTIONS
       00D0  0044
00337  00D2  811C            LDR     A1,A7               LOAD A1 WITH BIO CONTENTS  22
00338  00D4  0550            LDK     A5,IPLLEN           (A5) = LENGTH TO BE LOADED
00339  00D6  8194            LDR     A9,A5               USED FOR LEADING CHARACTERS
00340  00D8  8620            LDKL    A6,IPLADD           LOADING ADDRESS OF IPL
       00DA  0080
00341  00DC  8098            LDR     A8,A6
00342  00DE  90A0            ADKL    A8,4                (A8)  = START ADDRESS OF IPL
       00E0  0004
00343  00E2  8698            LDR     A14,A6              (A14) = LOADING AADDRESS OF IPL
00344                *
00345                * CHECK DEVICE TYPE
00346                *
```

```
00347  00E4  3FE7            SRC     A7,7                IS IT DISK ON IOP OR PC ?          2A
00348  00E6  5AB8            RB(2)   DISK                YES                                2C
00349  00E8  3FC1            SLC     A7,1                ROM IPL OR DMA UPL ?
00350  00EA  5EAA            RB(6)   SEQUEN              NO: INIT WER                       30
00351  00EC  3FC1            SLC     A7,1                YES : ROM IPL ?
00352  00EE  5200  F         RF(2)   ROMIPL              YES
00353  00F0  3FE3            SRC     A7,3                BIG DISC ?
00354  00F2  5600  F         RF(6)   BIGDIS              YES
00355  00F4  8112            LDR     A1,A12              NO : BRANCH TO BOOT UPL
00356  00F6  1100  F         ADK     A1,DMAUPL-BASE      IN HIGH-CORE
00357  00F8  8F04            ABR     A1                  (A12) = LOADING ADDRESS
00358                        EJECT
00359                 BIGDIS EQU     *
00360                 *
00361                 *      2 TYPES OF BIG DISC CONTROL UNIT WITHOUT CIO IPL
00362                 *             - BIGD2
00363                 *             - OTHER NOT YET SPECIFIED
00364                 *
00365  00FA  3FC9            SLC     A7,9                BIGD2 ?  (BIT 9 = 0 )
00366  00FC  5200  F         RF(2)   BIGNEW              NO
00367                 BIGD2  EQU     *
00368                 *
00369                 *      FOR CU BIGD2 2 TYPES OF DRIVES
00370                 *             SMD         1 PART   AMOVIBLE       BIT  7 = 0
00371                 *
00372                 *             CMD         2 PARTS  1 FIXED        BIT  7 = 1
00373                 *                                  1 AMOVIBLE     BIT  7 = 0
00374                 *
00375                 *             BITS  4,5,6  GIVE SECTOR NUMBER
00376                 *
00377  00FE  3FC3            SLC     A7,3                PUT SECTOR #   BITS 4,5,6
00378  0100  27F0            ANK     A7,/F0                 VOLUME #    BIT  7
00379  0102  AF41            ORS     A7,BIGD21           IN  BLOCK OF COMMANDS
       0104  0010
00380                                                        BITS  8 9 10 11
00381  0106  010E            LDK     A1,BIGD20           (A1) = ADDRESS OF BLOCK OF
00382                                                          COMMANDS
00383  0108  5FC4            RB      DMACDC              START LOADING
00384                 *
00385                 *      SEQUENCE  FOR NEW CONTROLLER BIG DISC
00386                 *
00387                 BIGNEW EQU     *
00388  010A  5F0E            RB      BIGD2
00389                 *
00390                        EJECT
00391                 ROMIPL EQU     *
00392                 *
00393                 *  FETCH FOR THE FIRST LOCATION ROM , NOT NULL ,FROM ADD /202
00394                 *  AND  BRANCH TO IT
00395                 *
00396  010C  8620            LDKL    A6,/200
       010E  0200
00397                 LOOP   EQU     *
00398  0110  1602            ADK     A6,2
00399  0112  8618            LDR     A6,A6               LOOP IF NO ROM
00400  0114  5802            RB(0)   *
00401  0116  8238            LDR*    A2,A6       TAKE CONTENTS OF CURRENT LOCATION      90
00402  0118  580A            RB(0)   LOOP             ROM CONTENT =0 NOT SIGNIFICANT VALUE  92
00403  011A  9039            IMR     A6               TRY TO MODIFY THE CURR MEMORY         94
00404  011C  EA38            CWR*    A2,A6       TEST IF STORE WAS SUCCESSFULL          96
00405  011E  8818            ABR(0)  A6          NO  THE LOCATION CONTENTS NOT CHANGED  98
00406                                                BRANCH TO IT                          9A
00407  0120  8239            STR     A2,A6            RESTORE PREVIOUS CONTENTS            9C
00408  0122  5F14            RB      LOOP             GO TO TEST NEXT LOCATION             9E
00409                        EJECT
00410                 *
00411                 *     DMA UPL
00412                 *
00413                 HARD   EQU     /100
00414                 *      BIT 0 AT LOCAATION /100 MUST BE 0
00415                 BASE   EQU     *
00416                 CSD    EQU     *
00417  0124  0000            DATA    0                   CID ADDRESS  0  ,  1
00418  0126  0000            DATA    0                   CID ADDRESS  2  ,  INTD = ****
00419  0128  0000            DATA    0           INTS = ****     ,  0                       A4
00420                 CID    EQU     *
00421  012A  0000            DATA    0                   IOD ADD OUT  0  ,  1
00422  012C  0000            DATA    0                   IOD ADD OUT  2  ,  IOD ADD IN 0
00423  012E  0000            DATA    0                   IOD ADD IN  1  ,  2
00424  0130  0000     ITSPEC DATA    0           INT SPEC        ,  RDN IN                  AC
00425  0132  0000            DATA    0           PAI CODE        ,  0                       AE
00426                 IOD    EQU     *
00427  0134  0082            DATA    /82                 RDN OUT      , COM= /82 (IPL)
00428  0136  0000     LOGSTA DATA    0                   LOGICAL STATUS
00429  0138  0000     PHYSTA DATA    0           PHYSICAL STATUS                            B4
00430  013A  0000            DATA    0                   IO AREA LENGTH
00431  013C  0000            DATA    0                                                      B8
00432  013E  0000     MEDCAR DATA    0                   MEDIUM CHARACTERS ,  *
00433  0140  0000            DATA    0           **            ,  IO AREA ADD  0          BC
00434  0142  0000     IOAREA DATA    0                   IO AREA ADD  1  ,  2
00435  0144  0000            DATA    0           REL SECT #   0  ,  1                       C0
00436  0146  0000     RSN    DATA    0           REL SECT #   2  ,  **                      C2
```

```
00437  0148  0000                DATA    0,0,0,0,0,0
       014A  0000
       014C  0000
       014E  0000
       0150  0000
       0152  0000
00438                    IODEND  EQU     *
00439                    DMAUPL  EQU     *
00440                    *
00441                    *       INIT CSD BLOCK WITH CID ADDRESS
00442                    *       AND CID BLOCK WITH IOD ADDRESS
00443                    *       THE ADDRESS FOR UPL IS ON 3 OCTADS
00444                    *       PUT IN A13 CSD BLOCK ADDRESS TRANSMITTED TO IPL
00445                    *
00446  0154  E592                ECR     A13,A12
00447  0156  E5D3                SC      A13,CSD+1-BASE,A12
       0158  0001
00448  015A  0106                LDK     A1,CID-BASE
00449  015C  E153                SC      A1,CSD+2-BASE,A12
       015E  0002
00450  0160  E5D3                SC      A13,CID+1-BASE,A12
       0162  0007
00451  0164  0110                LDK     A1,IOD-BASE
00452  0166  E153                SC      A1,CID+2-BASE,A12
       0168  0008
00453  016A  8592                LDR     A13,A12
00454  016C  E5D2                LC      A13,CSD+2-BASE,A12
       016E  0002
00455  0170  0100                LDK     A1,CSD-BASE             PUT CSD BLOCK ADDRESS
00456  0172  9112                ADR     A1,A12
00457  0174  8220                LDKL    A2,HARD                 AND HARD BLOCK @
       0176  0100
00458  0178  B941                MS      2,/80                   INTO LOCATION /80 AND /82
       017A  0080
00459  017C  E11E                ECR     A1,A15
00460  017E  8204                LDR     A2,A1
00461  0180  210F                ANK     A1,/F                   BITS  4,5,6,7  OF A15
00462  0182  3944                SLL     A1,4                    ARE BITS  0,1,2,3 OF
00463  0184  E153                SC      A1,MEDCAR-BASE,A12      MEDIUM CHARACTERS
       0186  001A
00464  0188  3A6E                SRL     A2,14                   BITS 8, 9 OF A15 ARE RELATIVE
00465  018A  3A48                SLL     A2,8                    DEVICE NUMBER
00466  018C  2A82                ORK     A2,/82                  IPL COMMAND CODE
00467  018E  8253                ST      A2,IOD-BASE,A12         --> IOD
       0190  0010
00468  0192  821E                LDR     A2,A15                                                  D6
00469  0194  223F                ANK     A2,/3F                  PUT DMA UPL ADDRESS             D8
00470  0196  AA53                ORS     A2,CIOUPL-BASE,A12
       0198  0000  F
00471  019A  A053                CM      ITSPEC-BASE,A12         CLEAR INTERRUPTS FIELD
       019C  000C
00472  019E  41C0       CIOUPL   CIO     A1,1,0                  CIO IPL
00473                    TSTIT   EQU     *
00474  01A0  E652                LC      A6,ITSPEC-BASE,A12      LOOP UNTIL
       01A2  000C
00475  01A4  2620                ANK     A6,/20                  END OF IO
00476  01A6  5808                RB(0)   TSTIT
00477  01A8  8152                LD      A1,PHYSTA-BASE,A12      TEST STATUS  PHYSTA
       01AA  0014
00478  01AC  A952                OR      A1,LOGSTA-BASE,A12              AND    LOGSTA
       01AE  0012
00479  01B0  5C5E                RB(4)   DMAUPL                  IF ONE OF THESE BITS SET
00480  01B2  8F52                ABI     IOAREA-BASE,A12         BRANCH TO LOAD ADDRESS
       01B4  001E
00481                    *       EJECT
00482                    *
00483                    *     16 WORDS ARE RESERVED AT END OF BOOTSTRAP
00484                    *     THEIR CONTENTS ARE LOADED AT IPL IN REGISTER A15
00485                    *     TO CHOOSE THE VALUE, THE HARDWARE USES AS INDEX
00486                    *        (WORD 0 IS THE LAST ONE AT LOCATION /1FE)
00487                    *        (WORD 15 IS THE FIRST ONE AT LOCATION /1E0)
00488                    *        THE VALUE OF A WHEEL WITH INDEXES FROM 0 TO /F
00489                    *
00490                    *                 OR STRAPS WITH INDEXES FROM  0 TO   7    3 STRAPS
00491                    *                                          OR        0 TO / F    4 STRAPS
00492                    *
00493                    *
00494                    *     THIS WAY OF LOADING A15 IS USED WHEN IPL IS NOT DONE
00495                    *     FROM A CONTROL PANEL
00496                    *                              - AUTOMATIC IPL
00497                    *                              - AUTOMATIC RE-IPL  (BATTERY OFF)
00498                    *                              - REMOTE IPL
00499                    *
00500                            AORG    /1E0
00501  01E0  FFFF                DATA    /FFFF   DMA UPL                                 15
00502  01E2  2116                DATA    /2116           CMD FIXED PART                  14
00503  01E4  65E2                DATA    /65E2           X1215 FIXED DISC INTERFACE 5    13
00504  01E6  2056                DATA    /2056           NEW CU BIG DISC EUROBOARD       12
00505  01E8  2016                DATA    /2016           CMD CARTRIDGE OR SMD            11
00506  01EA  0116                DATA    /0116   CDC                     0               10
00507  01EC  400A                DATA    /400A           FHD DISC                         9
00508  01EE  103F                DATA    /103F   IPLRZ                                    8
00509  01F0  0785                DATA    /0785   K7          IOP         0                7
00510  01F2  3000                DATA    /3000   ROM IPL                                  6
00511  01F4  150D                DATA    /150D   REMOTE IPL                               5
00512  01F6  63C2                DATA    /63C2   X1215     3 CARTRIDGE   0                4
00513  01F8  60C1                DATA    /60C1             X1250 DISC                     3
00514  01FA  6083                DATA    /6083   FLOPPY 1MB             0                2
00515  01FC  4083                DATA    /4083           FLOPPY IOP 1/4 MB                1
00516  01FE  1020                DATA    /1020           PTR                              0
00517                    LIMIT   END     BOOT
```

```
                SYMBOL TABLE

  IPLADD  0080  A    IPLLEN  0050  A    BOOT    0000  A    BOOT00  0082  A
  SSTCP   0002  A    INR     0054  A    TSTSTA  0006  A    NEWIO   002A  A
  BRANCH  000C  A    BIGD20  000E  A    BIGD21  0010  A    BIGD22  0012  A
  BIGD23  0014  A    BIGD24  0016  A    BIGD25  0018  A    TSTA    0024  A
  CIOSTA  004A  A    SEQUEN  0042  A    DISK    0030  A    NOSEEK  0038  A
  CIO     0036  A    WER1    0042  A    WER2    0044  A    DMACDC  0046  A
  SST     007A  A    INR10   0060  A    STORE   0068  A    HIO     0072  A
  HARD    0100  A    BOOO10  008A  A    BOOO20  0096  A    BASE    0124  A
  LIMIT   0200  A    BOO30   00A0  A    INIT10  00AC  A    INIT20  00C6  A
  ROMIPL  010C  A    BIGDIS  00FA  A    DMAUPL  0154  A    BIGNEW  010A  A
  BIGD2   00FE  A    LOOP    0110  A    CSD     0124  A    CID     012A  A
  ITSPEC  0130  A    IOD     0134  A    LOGSTA  0136  A    PHYSTA  0138  A
  MEDCAR  013E  A    IOAREA  0142  A    RSN     0146  A    IODEND  0154  A
  CIOUPL  019E  A    TSTIT   01A0  A

          ASS.ERR.    00000
:EOF

EXIT CODE= /00
SKP
```

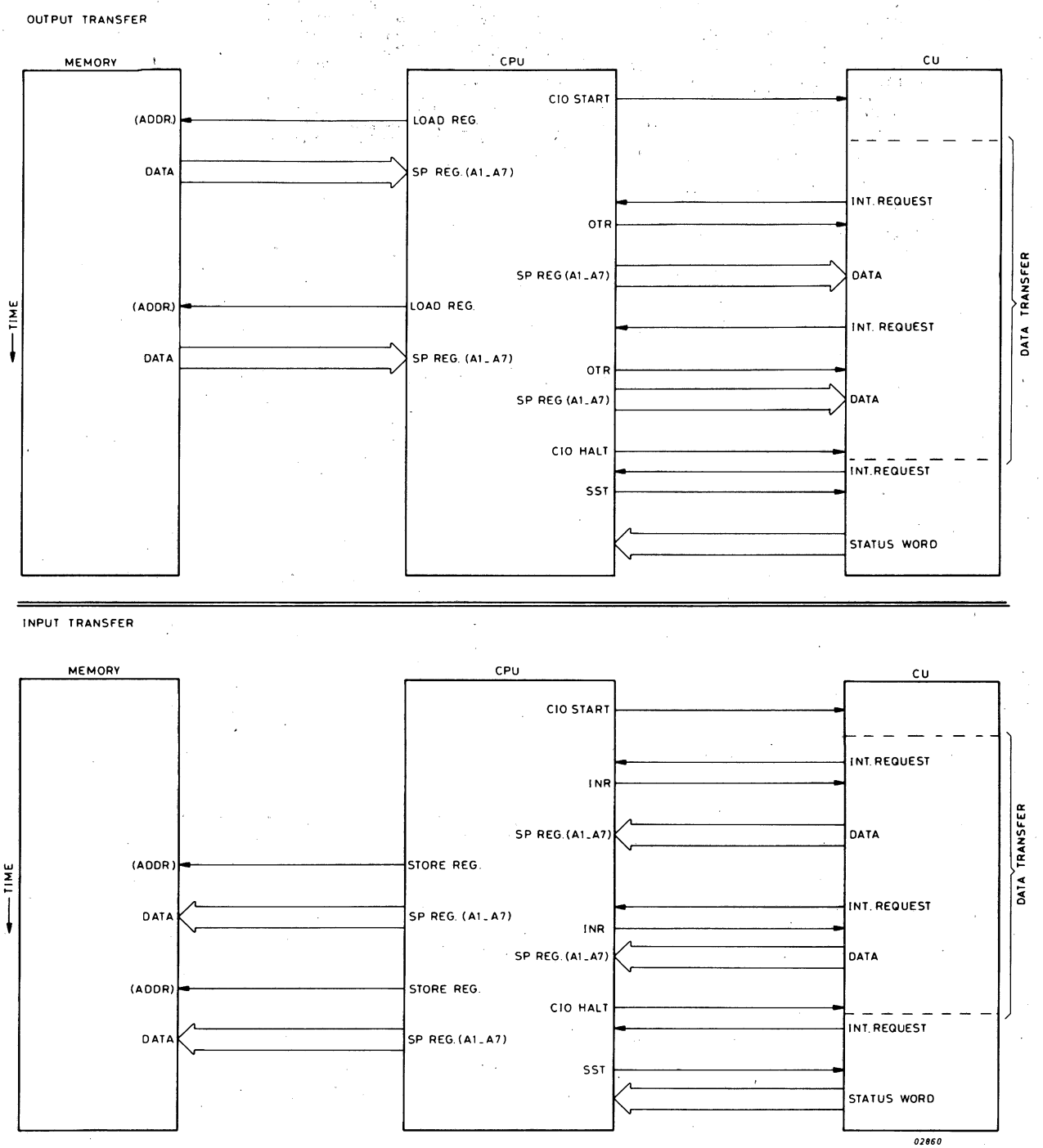
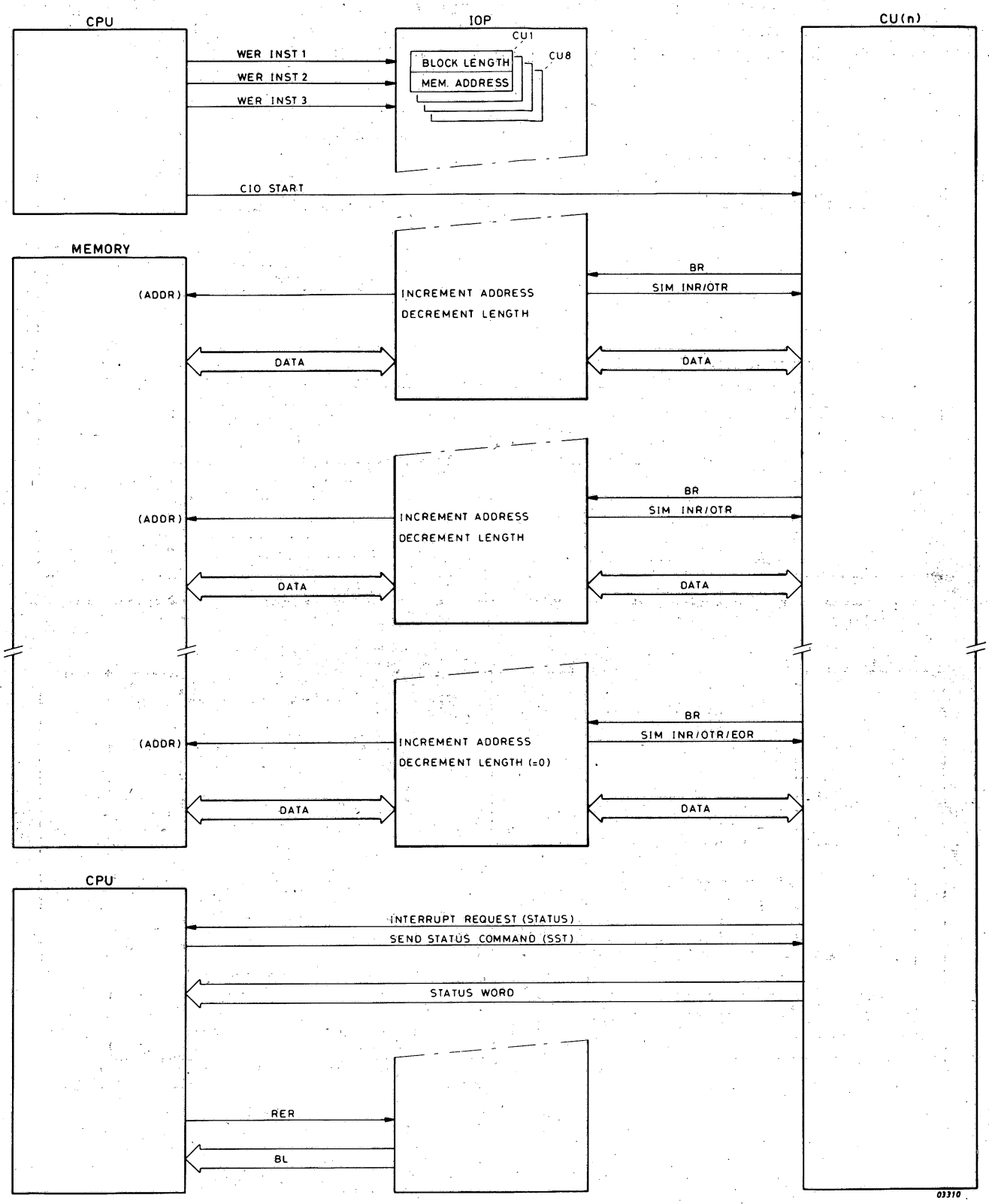


Figure 1.17 INPUT AND OUTPUT PROGRAMMED CHANNEL TRANSFERS



*Note: WER 1,2 and 3 must be executed in this order.

Figure 1.18 IOP CHANNEL TRANSFERS

The DMA Channel enables a high speed control unit to make direct exchanges with memory. The following figure shows the sequence of events for a DMA transfer. The principle of operation is the same as for the IOP but as only one device is used the IOP/CU function is incorporated in the DMACU.

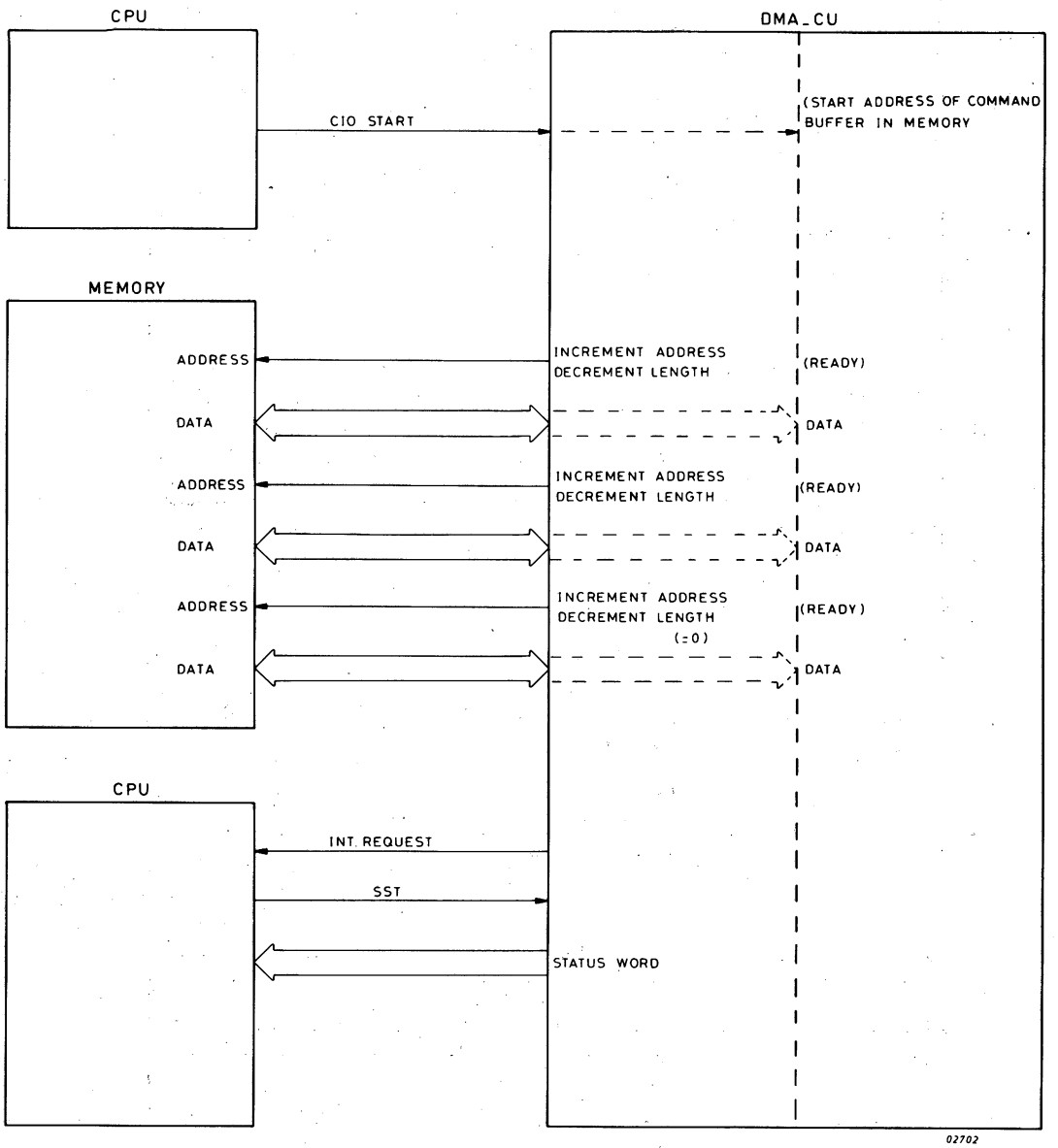


Figure 1.19 DIRECT MEMORY ACCESS CHANNEL TRANSFER

1.16 BASIC SYSTEM TYPES

In the P800 series "BASIC SYSTEMS" have been defined.
A basic system consists of:

- a mounting box (rack) with a certain number of slots in which memory and control units cards can be inserted
- an integrated power supply unit
- a control panel and/or control panel interface
- a CPU card or card-set

The systems as described below do not contain any memory.
However, for reasons of system responsibility no systems without memory can be delivered, unless a special arrangement with the customer has been made.
The basic systems are equipped with a battery pack and logic for power supply during (mains) power failure and with a filter.
Mounting gear for standard 19" cabinets is supplied with all basic systems.

TYPE NUMBERS AND MODELS

TYPE NUMBER	DESCRIPTION
P871-300	P871 Basic System with 11 free general purpose slots. Incl. battery back-up, mains filter, control panel interface for either Hand Held Panel (HHP) or Extended Digital Panel (FRCP), facility for connection of Winchester disc drives.
P874-300	P874 Basic System with 9 free general purpose slots. Incl. battery back-up, mains filter, control panel interface for either Hand Panel (HHP) or Extended Digital Panel (FRCP), or Extended Digital Panel (FRCP), facility for connection of Winchester disc drives. A ventilation unit is mandatory if the system is mounted in a cabinet, otherwise it is strongly recommended: Ventilation unit for Logic Rack: P843-200
P873-400	P874 Basic System with 20 free general purpose slots. Incl. power supplies PSU-B1E and PSUM, battery back-up filter board PSU8B, ventilation units, control panel interface for either Hand Held Panel (HHP) or Extended Digital Panel (FRCP), facility for connection of Winchester disc drives.
P876-400	P876 Basic System with 18 free general purpose slots. Incl. power supplies PSU-B1E and PSUM, battery back-up, filter board PSU8B, ventilation units, cable support, control panel interface for either Hand Held Panel (HHP) or Extended Digital Panel (FRCP), facility for connection of Winchester disc drives.

BASIC SYSTEM COMPONENTS

	P871	P874	P876
Racks: RA12F rack	-300	-300	
RAL22F rack	-400	-400	-400
CPU's: CP1BF card	x		
CP7E: C7E2, C7E1, MIOP cards		x	
CP2B: CIPC, CIPA, CIPB, CIPG, CIPF cards			x

1.17 BASIC SYSTEM MOUNTING CODES AND POWER CHARACTERISTICS

Type Number	Free slots	Mounting Code	power available (in AMP) --logic-					--memory--	
			+5V	-5V	+12V	-12V	+24V	+5V	+12V
P871-300	11	rack 6U	27.4		0.98	0.48	3.5	3.0	
P874-300	9	rack 6U	21.2		0.9	0.47	3.5	3.0	
P874-400	20	rack 10U	31.2	1.0	1.25	0.95	3.5	3.0	1.5
P876-400	18	rack 12U	15.0	1.0	1.25	0.95	3.5	3.0	1.5

Remark: The number of U(nits) denotes the height of the rack.
1U is 1.75 (44.45).
The standard 19" rack is 36U of which 33U is available.
The configurations include a battery pack with the following characteristics:

System	Capacity	Charging time
P871-300	2.5Ah	48h
P874-300	2.5Ah	48h
P874-400	5.0Ah	48h
P876-400	5.0Ah	48h

A second PSU-B1E is optional for the P874/6-400 systems

Maximally two racks P829-001 or P829-005 may be connected to one system.

For further information refer to chapters 2 and 3.

2 CABINETS

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2.1 BASIC AND EXTENSION CABINETS

2.1.1. IDENTIFICATIONS

The Basic Cabinet is 19" wide with a usable depth of 0.7 m (27.5") and a mounting height of 36 standard units (36U) enclosed by side panels and rear door.
The extension cabinet has the same characteristics except they have no side panels.

BASIC CABINETS 19"

P849-076	BAS. CAB. 36U NON EQUIPPED	5111 010 03440
	STANDARD DOOR (FOR ALL CABINETS)	5111 199 71350
P849-077	BAS. CAB. 36U POWER DIS. 14A/220V, 2 VENT.	5111 199 54850
	KIT WITH BASIC SPARE PARTS	5111 199 60960
	VENTILATION ASSEMBLY (2 FANS)	5111 199 60980
	POWER DISTRIBUTION ASSEMBLY	5111 199 64840

EXTENSION CABINETS 19"

P849-176	EXT. CAB. 36U NON EQUIPPED	5111 199 03450
	FILTER	5111 199 03730
	EXT. CONNECTION ASSEMBLY	5111 199 61000
P849-177	EXT. CAB. 36U VENT. UNIT	5111 199 54840
	KIT WITH BASIC SPARE PARTS	5111 199 60960
	VENTILATION ASSEMBLY (2 FAN)	5111 199 60980
	EXT. CONNECTION ASSEMBLY	5111 199 61000
P849-078	PEDESTAL STABILISER	5111 199 03500

POWER DISTRIBUTION UNITS

P849-042	POWER DISTRIBUTION PANEL 14A/220V	5111 199 64840
	KIT WITH BASIC SPARE PARTS	5111 199 60960
P849-043	POWER DISTRIBUTION PANEL 25A/220V	5111 199 83010
	KIT BASIC CABINET	5111 199 81170

VENTILATION UNITS

P849-070	VENTILATION UNIT 2 FANS	5111 199 60980
P849-071	VENTILATION UNIT 4 FANS	5111 199 60990
P843-200	VENTILATION UNIT LOGIC RACK P871/P874 (STANDARD ON P876)	5111 199 61260

PANELS

P849-029	MODEM PANEL (AT REAR OF CABINET)	5111 199 75210
P849-046	FRONT PANEL 1U	5111 199 82870
	ADAPTATION (FOR ALL FRONT PANELS)	5111 199 71410
P849-047	FRONT PANEL 3U	5111 199 85260
P849-048	FRONT PANEL 5U	5111 199 85250
P949-049	FRONT PANEL 7U	5111 199 85240

SYSTEM FRONT PANELS

P843-501	PANEL 4U, FOR HHP CONTR. PANEL	5111 199 59660
P843-502	PANEL 6U, PANEL FOR P874/6-400 (RAL22F)	5111 199 54560
P843-503	PANEL 4U, NO CONTR. PAN. P874/6-400	5111 199 59430
P843-510	PANEL 4U, WITH FRCP CONTR. PAN. INCLUDED	5111 199 59670
	NOTE: KIT WITH KEY-SWITCH COVER-PLATES (DELIVERED WITH P843-501/502/503/510)	5111 199 59440
P843-504	PANEL 6U, FOR P871/4-300 (RA12F)	5111 199 54280

2.1.2 MOUNTING DEVICES

The different mounting devices include:

. Telescopic slides for the Magnetic Tape Formatter Floppy-Drive Racks, and moving head disc drives.
. Mounting Hinges for the Magnetic Tape Transport.
. Fixed slides for Floppy-Drive Racks and Ventilation Unit.

Some units such as the card Mounting Box are fitted directly to the rack by screws.

2.1.3 FRONT PANELS

Front panels of either 1, 3 5 or 7 rack units are available to fill the spaces not used (or cover items like equipment shelves) in the cabinet.
Front panels of 4 and 6 rack units are available for the RA12F and RAL22F racks (see: Identifications).
The 6U panel covers the Logic Card rack and the 4U panel must be fitted just above, to hold the Control Panels FRCP or HHP, or to cover the Key-Switch or Ventilation unit of the RAL22F rack.

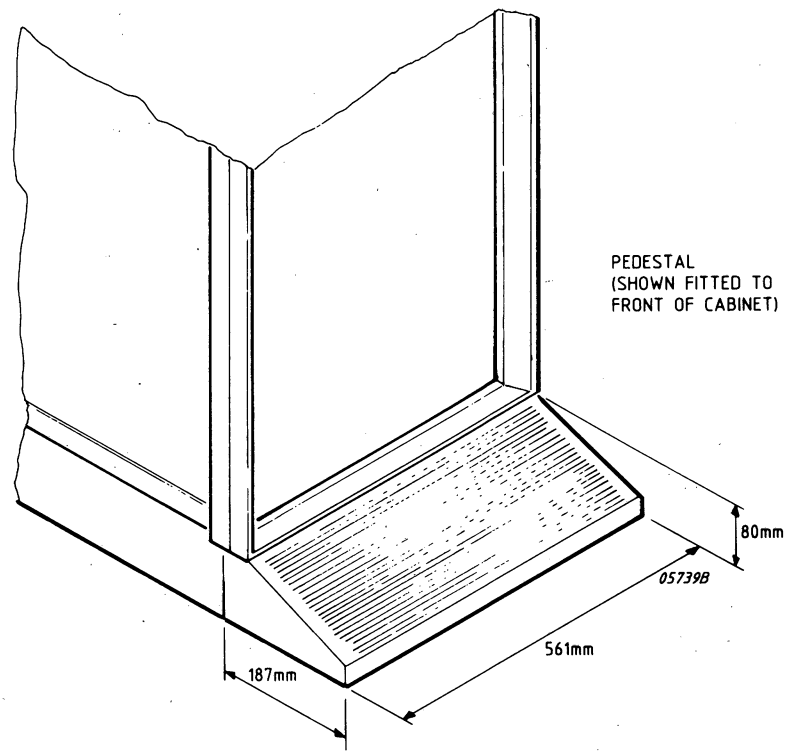


Figure 2.1.1 MOUNTING KIT PEDESTAL (P849-078)

2.1.4 VENTILATION UNITS

Convection cooling is sufficient if the total heat dissipation of the equipment in the cabinet is les the 700 kcal/h (800 watts). Above this level forced air circulation by one of the following ventilation units is necessary. Both units are similar except for the number of fans and the unit needs 1U space in the cabinet. The heat dissipation capabilities of the units are:

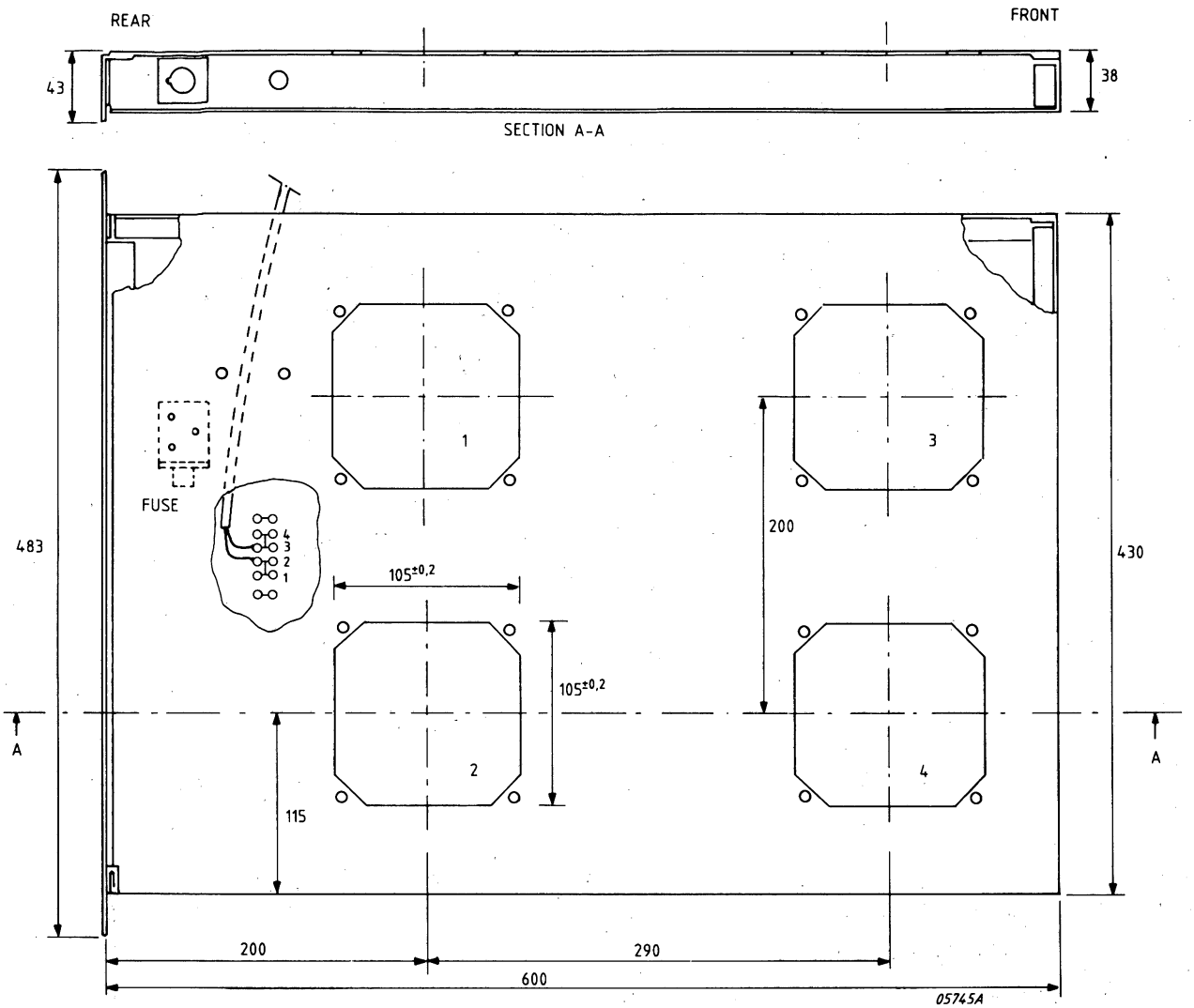
- P849-070 between 700 and 1030 kcal/h (800 to 1200 watts)
- P849-071 between 1030 and 1300 kcal/h (1200 to 1500 watts)

Extra ventilation units are necessary for the rack RAL22F.

2.1.5 POWER DISTRIBUTION PANELS

Two types of distribution panels are available to suit different power consumption levels. Both panels are 2U high and have a main filter, mains isolation switch, neon indicator, fuse and terminal block. The current carrying capacities are:

- P849-042 14 amperes
- P849-043 25 amperes



P849-070: 2 FANS-220V(1,2), FUSE: 0,25A/220V SLOW
P849-071: 4 FANS-220V(1-4), FUSE: 0,5A/220V SLOW

VENTILATOR UNITS ARE SUPPLIED WITH FIXED SLIDES

ALL DIMENSIONS ARE IN mm

Figure 2.1.2 VENTILATOR UNITS P839-070/71

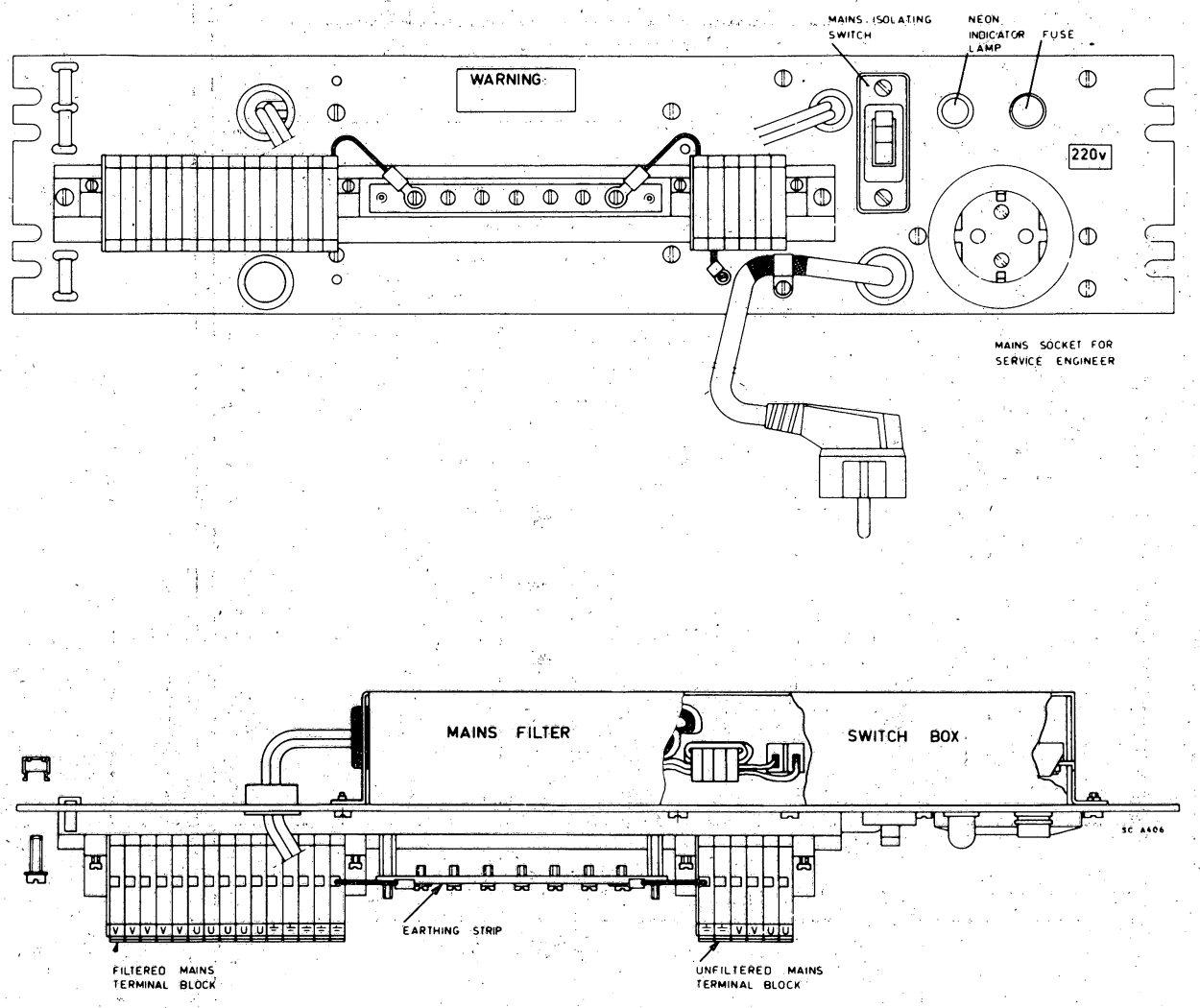


Figure 2.1.3 14 AMPERE DISTRIBUTION PANEL

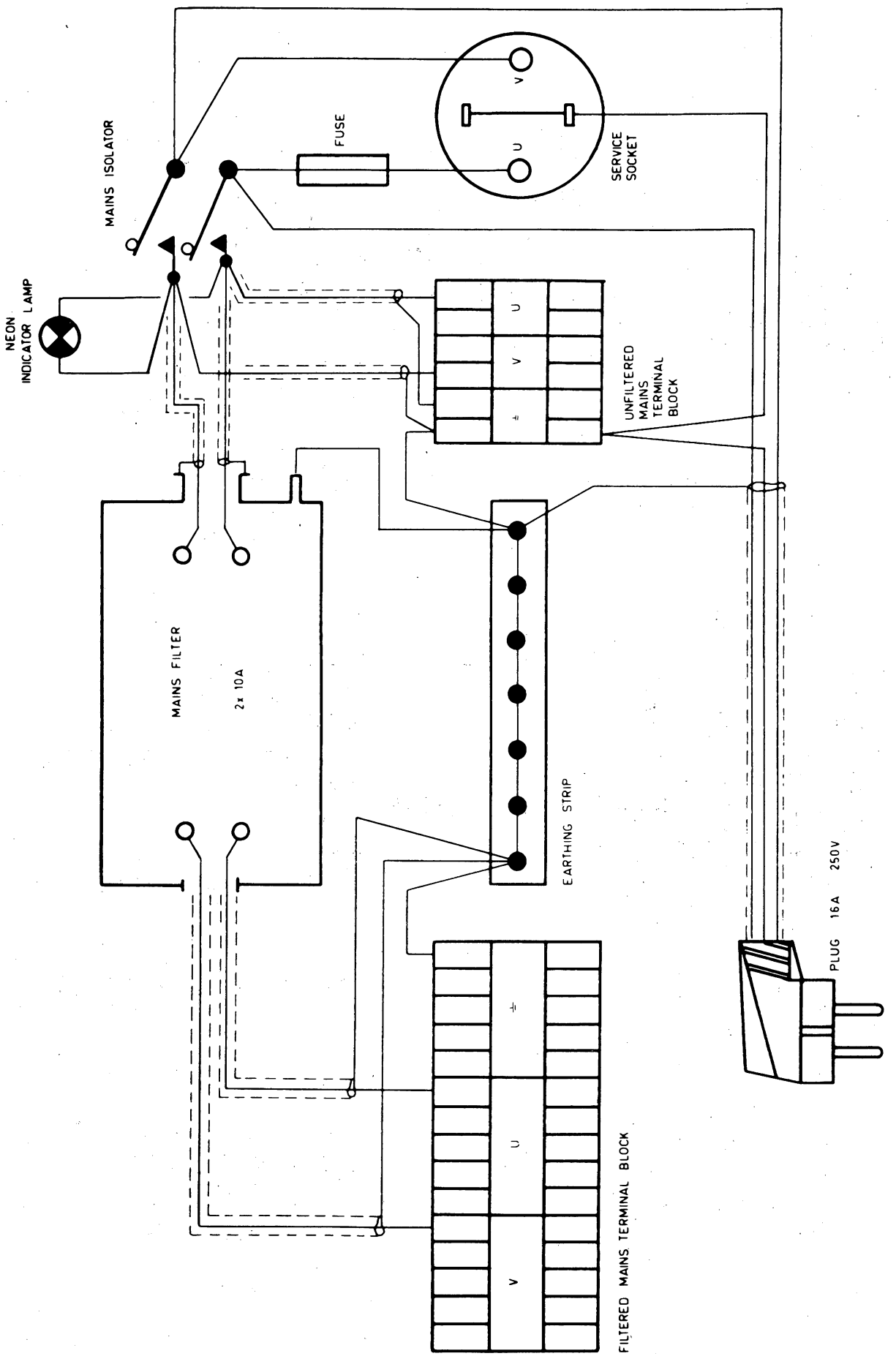


Figure 2.1.4 14 AMPERE DISTRIBUTION PANEL, CIRCUIT

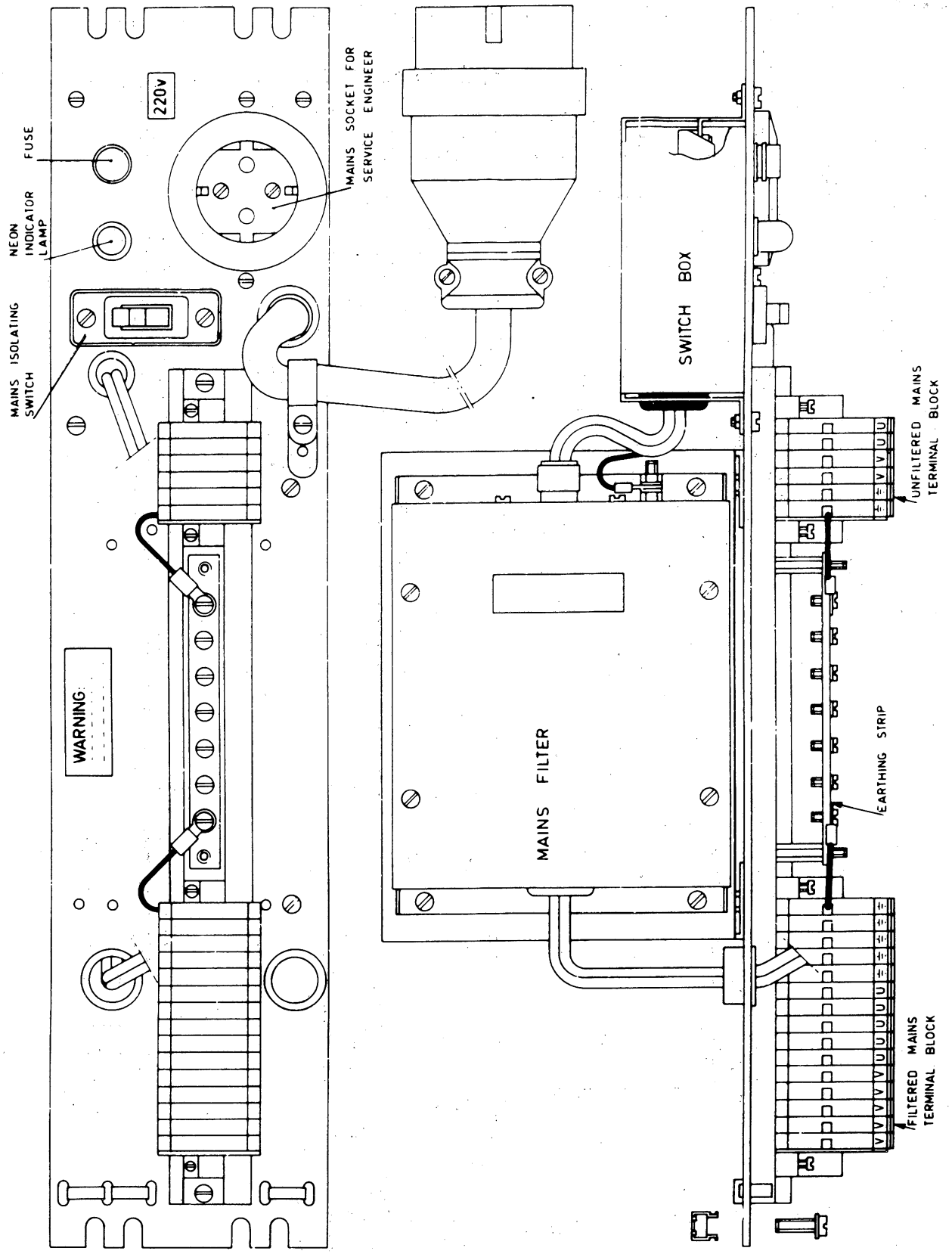


Figure 2.1.5 25 AMPERE DISTRIBUTION PANEL

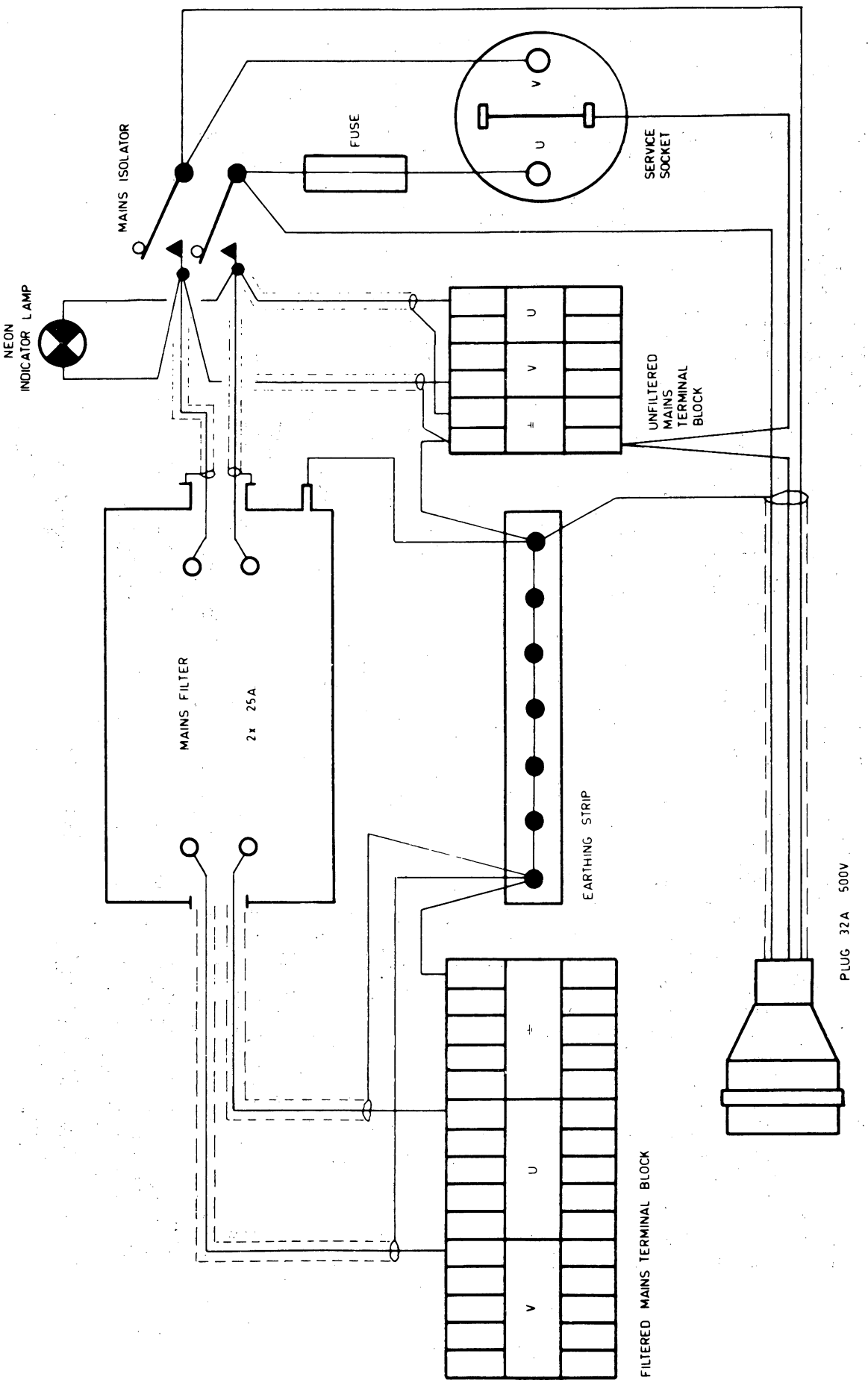


Figure 2.1.6 25 AMPERE DISTRIBUTION PANEL, CIRCUIT

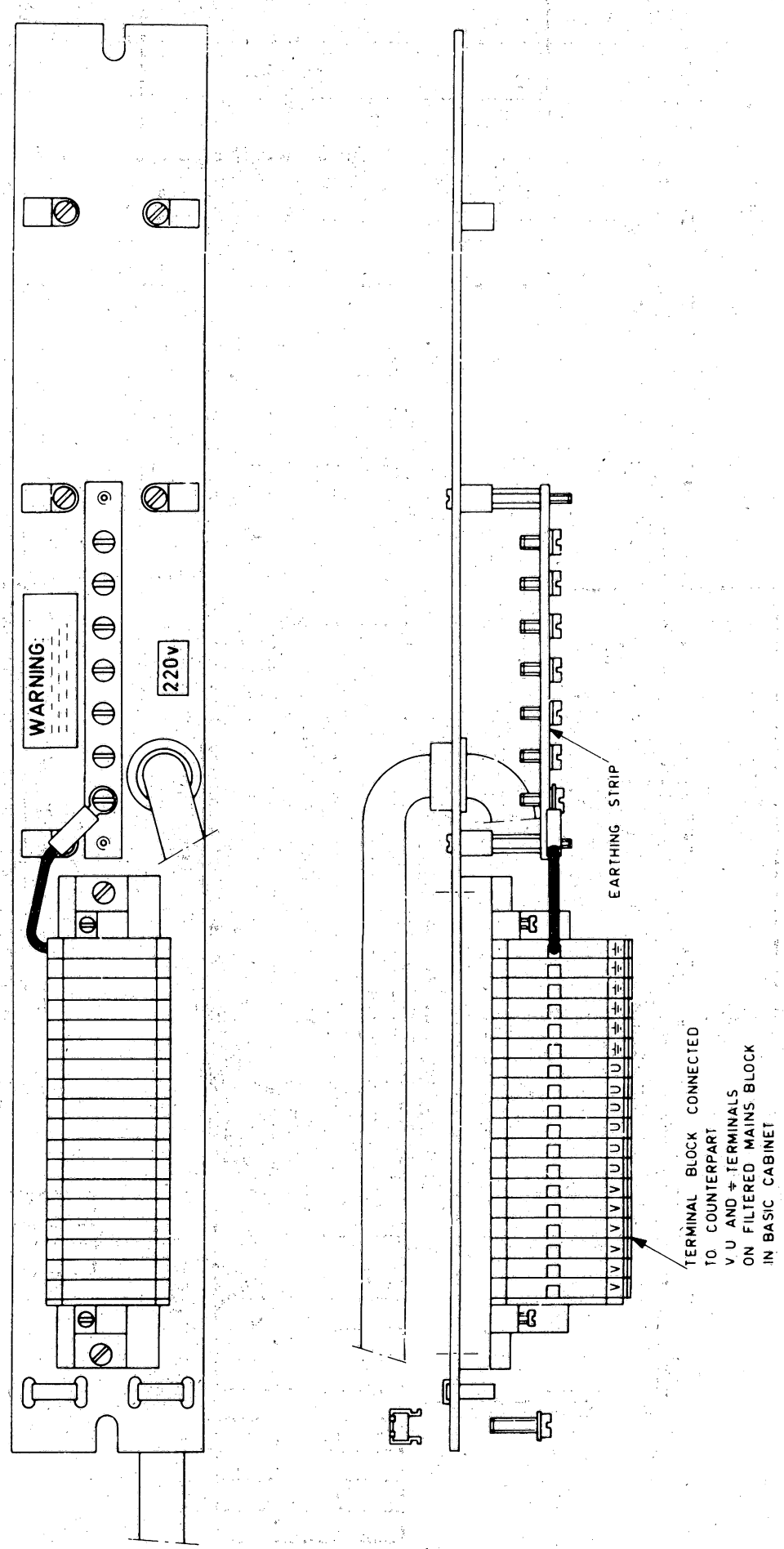


Figure 2.1.7 EXTENSION CABINET DISTRIBUTION PANEL

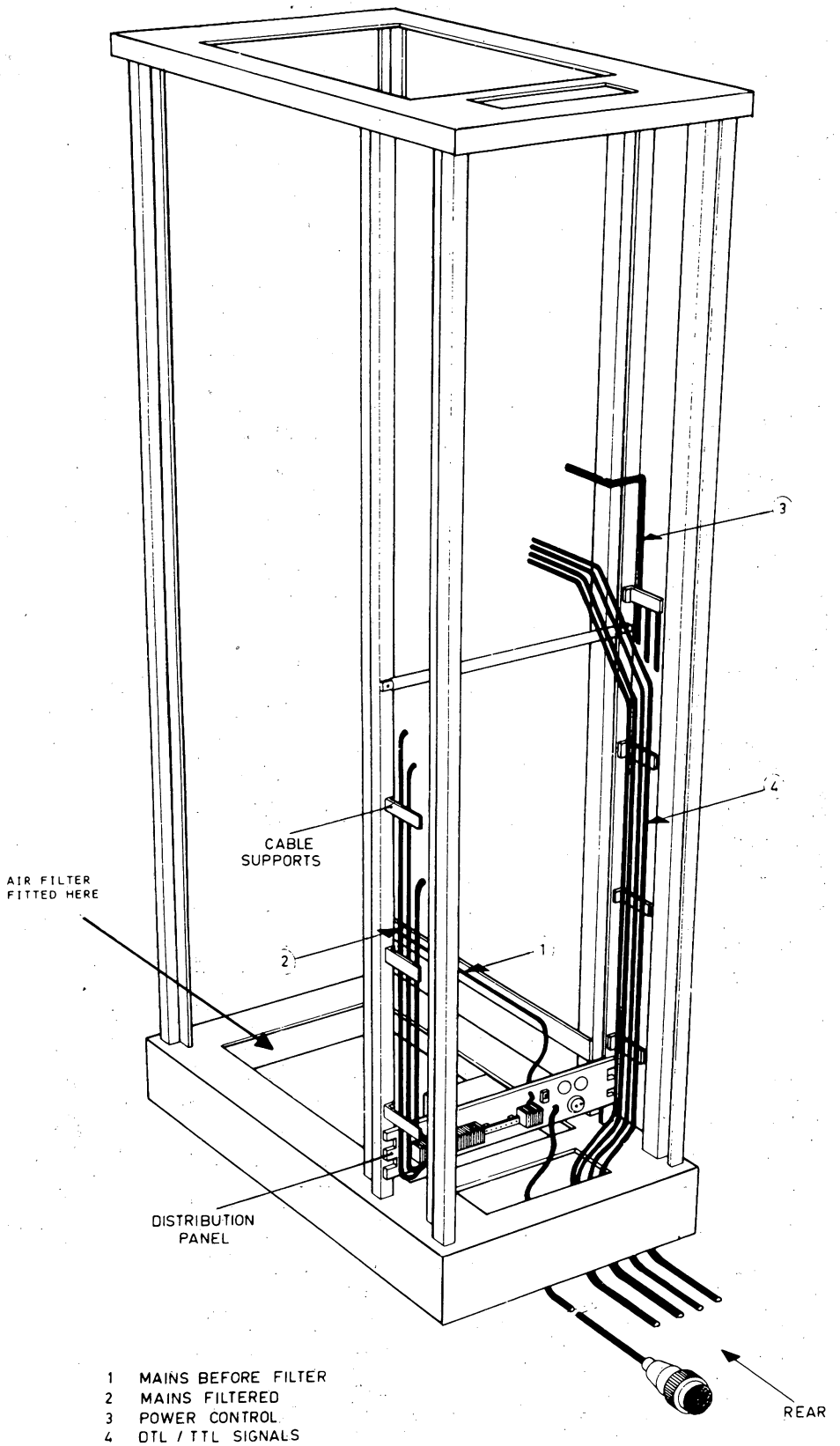


Figure 2.1.8 EXAMPLE OF CABINET WIRING

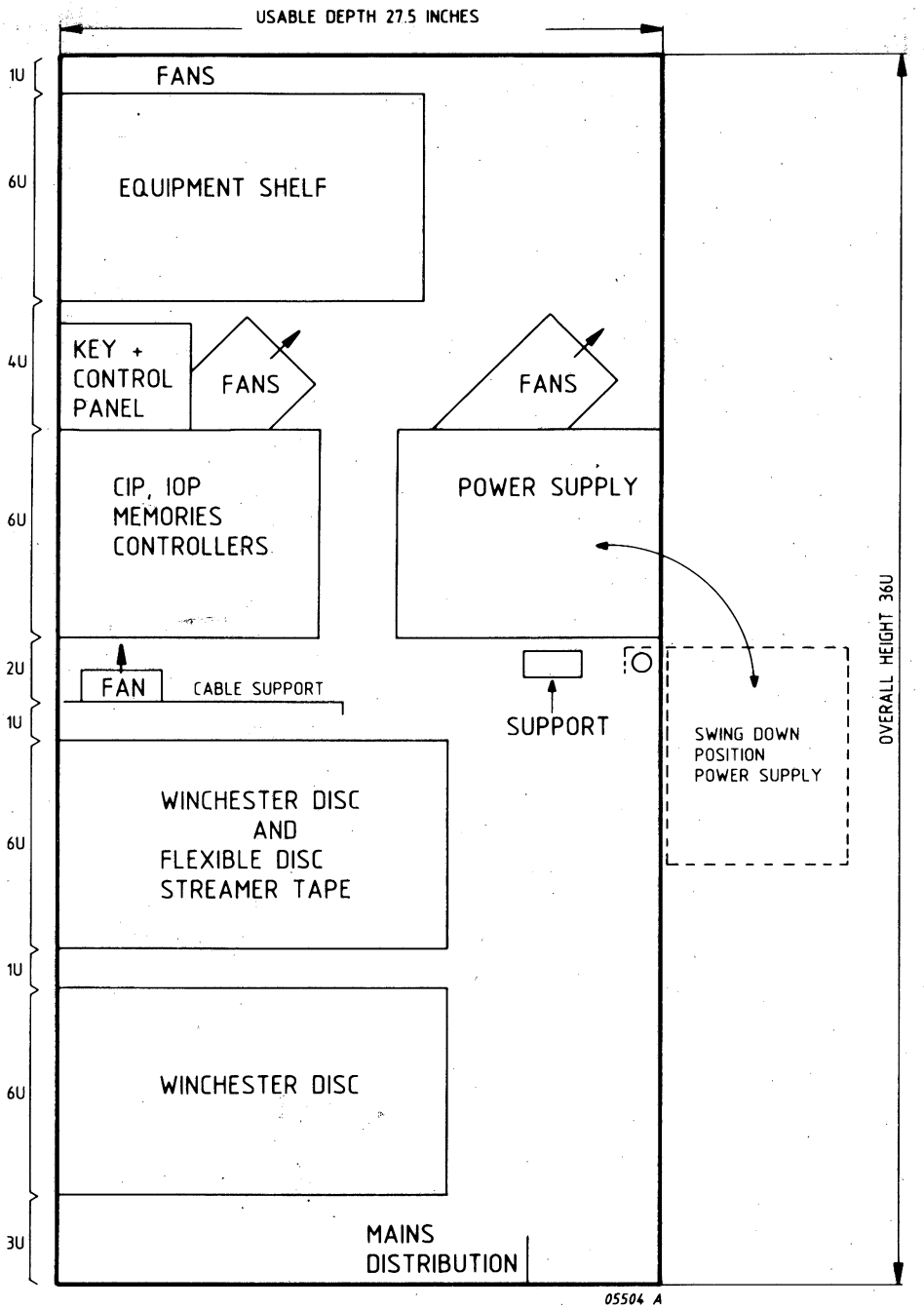


Figure 2.1.9 CABINET CONFIGURATION P876-400

Notes: P871/874-300 : RA12F Logic rack with integrated Power Supply.
CABLE SUPPORT: 1U, optional, without FAN
4U FANS ASSEMBLY: optional
KEY SWITCH on integrated Power Supply.

P874-400 : RAS22F rack without 2U Cable Support.
CABLE SUPPORT: 1U, optional, without FAN.

2.2 DISC CABINETS P825-008

2.2.1 IDENTIFICATIONS

P825-008/04	DISC DRIVE 80MB (1ST. DRIVE) EURO	
	DISC DRIVE SMD 80MD BJ9-E8D	5111 010 08890
	CABLE "A" SMD 7.5M	5111 199 52720
	CABLE "B" SMD 7.5M	5111 199 56670
P825-008/14	DISC DRIVE 80MB (2nd. DRIVE) EURO	
	DISC DRIVE SMD 80MB BJ9-E8D	5111 010 08890
	CABLE "A" DAISY CHAIN	5111 199 52710
	CABLE "B" SMD 7.5M	5111 199 56670
P825-200	DISC PACK 80MB FOR P825-008	8709 001 20801

2.2.2 OPERATING DISC UNIT

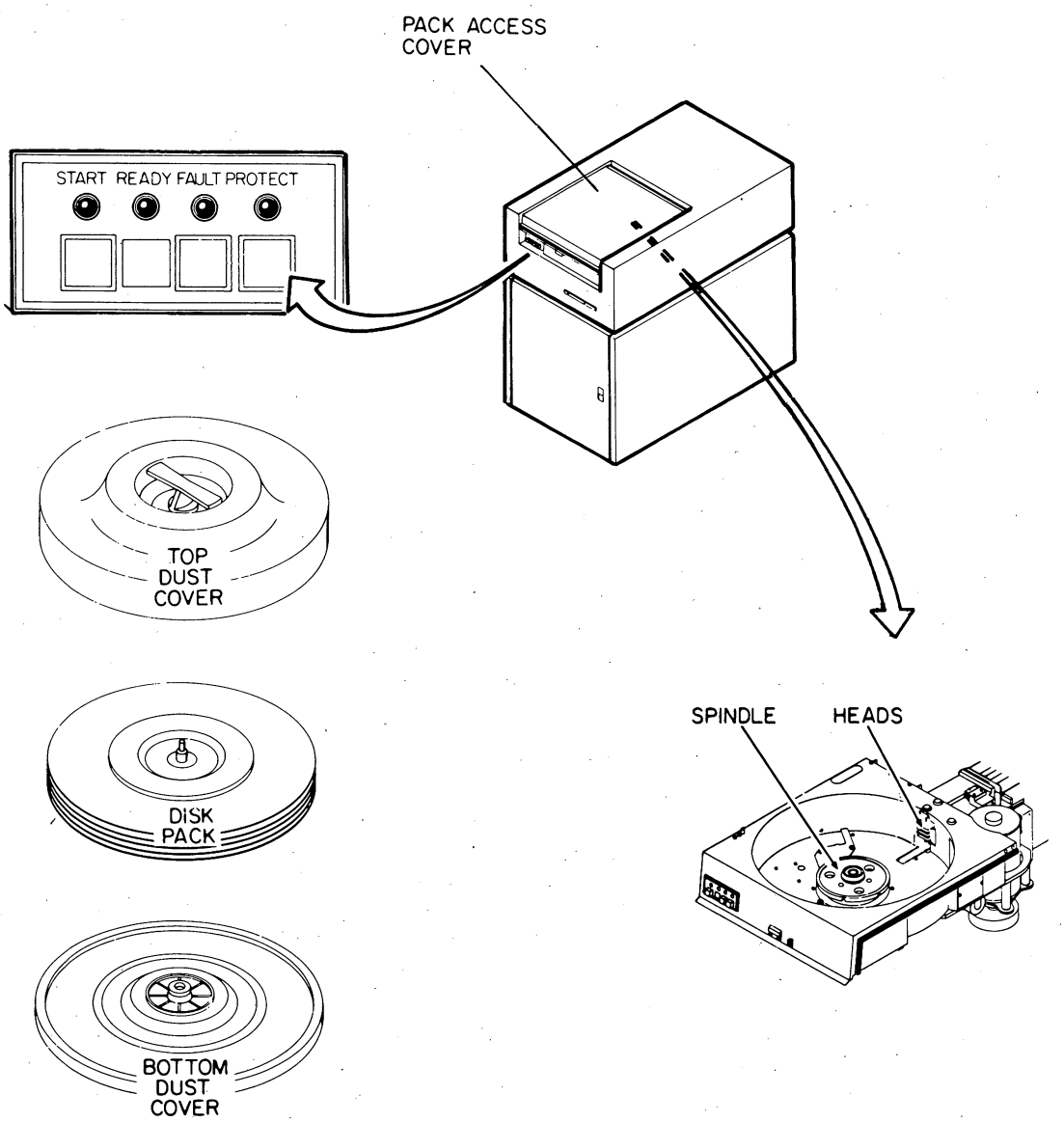


Figure 2.2.1 OPERATING DISC UNIT P825-008

To install a disc pack (P825-200):

. Make certain that the disc pack to be installed has been maintained according to the preventive maintenance instruction.

. Ensure that AC POWER is ON and raise pack access cover.

. Lift disc pack by plastic canister handle.

. Disengage bottom dust cover from disc pack by turning canister handle counter-clockwise or, for newer disc packs, squeeze the levers in the center of the bottom dust cover. Set cover aside in an uncontaminated area.

CAUTION

Avoid abusive contact between the disc pack and the spindle. The read/write heads are sometimes manually positioned during maintenance procedures. Make certain that the heads are fully retracted.

. Place disc pack onto spindle. A spindle lock mechanism is actuated when the disc pack canister cover is on the spindle. The mechanism holds the spindle stationary while loading or unloading disc pack.

. Twist canister handle colockwise to lock disc pack in place. a click may be heard as the spindle lock mechanism engages.

. Lift canister clear of disc pack, place bottom dust cover on canister, and set aside in an uncontaiminated area.

. Close pack access immediately to prevent entry of dust and contamination of disc surfaces.

To remove a disc pack:

. Press the operator panel START switch to extinguish the START indicator.

. Check that disc pack rotation has stopped. (Stopping time is approximately 1.5 minutes without brake and 20 seconds with brake).

. Raise access cover.

CAUTION

The read/write heads are sometimes manually positioned during maintenance procedures. Make certain that the heads are fully retracted.

. Place plastic canister over mounted disc pack so that post protruding from center of disc pack is received into canister handle.

. Twist canister handle counter-clockwise until disc pack is free of spindle.

CAUTION

Avoide abusive contact between the disc pack and the spindle assembly.

. Lift canister and disc pack clear of spindle and close access cover.

. Place bottom dust cover in position on disc pack and lock it.

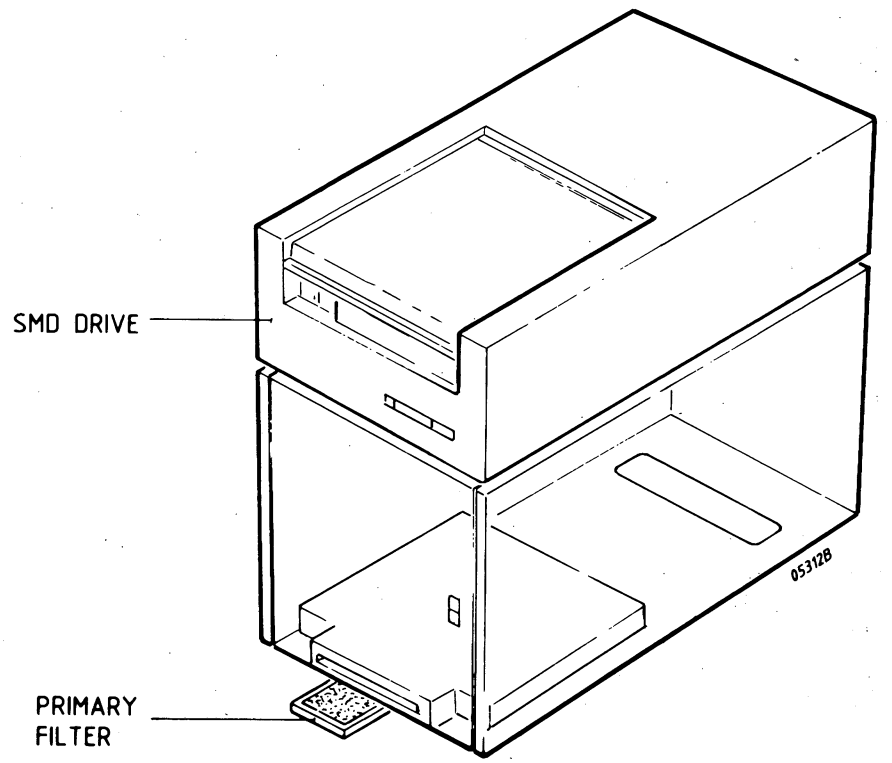


Figure 2.2.2 CABINET P825-008

PACKING/UNPACKING

During unpacking, exercise care so that any tools being used do not cause damage to the unit. As the unit is unpacked, inspect if for possible shipping damage. All claims for this type of damage should be filed promptly with the transporter involved. If a claim is filed for damages, save the original pakcing materials.

- During unpacking take care to avoid damage.
- Open the top cover.
- Remove the screw securing deck holddown bracket of the deck assembly. Loosen the screw securing the bracket to base assembly. Slide bracket away from deck and rotate it 90 degrees toward front of the drive. Tighten the screw securing the bracket to the base. Replace screw that secured the bracket to the deck and tighten it.
- Loosen the deck to frame hold down screws.
- Raise deck to maintenance position.
- Inspect base assembly, deck assembly and power supply for damage. Note damagings on the installation form.
- Inspect and if necessary rewire A1TB1 for the desired AC voltage.
- Lower the deck again and secure deck assembly to the base assembly with the two hold down screws.
- Remove the rear deck hold down screw and spacer. Install them in the keeper hole on rear of the deck.
- Inspect top of deck assembly for damage. Note damagings.
- Raise pack access cover and inspect the read/write heads and arms for physical damage and foreign material.
- When necessary use a vacuum cleaner to remove dust and other foreign material from interior of shroud and cabinet.
- Remove spindle cover and inspect for any foreign material around pack locator and spindle. Remove this material.

- Raise logic chassis in maintenance position and inspect connectors and wiring for loose or broken connections. Make sure all connectors and logic cards are firmly seated and check for loose hardware. Lower the rack to the normal position.
- Remove carriage locking pin from the shipping hole and put it into the storage hole.
- Check pack access cover for tight seal.
- Check and/or install the primary air filter. With new disc units there is maybe a wooden shelf installed, remove it.
- Turn down leveling pads until casters are completely off the floor.
- Adjust leveling pads until top surface is horizontal.

INSTALLATION

- Connect the drive to a suitable external power source. Maximum start up current is 23Amp.
  Do not switch on yet.
- Install the unit select plug in the front panel, select that plug which indicates the correct number for that drive.
- Connect the A-cable(s) and the B-cable(s).
- Put a terminator on the last drive in the daisy chain.
- Check if the number of sectors installed in the switches on card LTV on place A03 is correct, this should be as indicated in Section "Switch Setting".
- Remove the black voice coil wire.
- Set AC power circuit breaker to ON. The blower should start.
- Set POWER SUPPLY circuit breaker to ON. The logic fan should start.
  Observe START indicator on front panel. If on press the START switch to extinguish it.

  Caution: Ensure the carriage is in full retract position to avoid contact between data pack cover and head arm assemblies.

- Install a data pack and press START.
  Observe the following:
  a. Start indicator lights.
  b. Drive motor starts.

Allow the drive to operate in this condition for 5 to 10 minutes.
- Press START switch to stop the spindle motor. When the motor is stopped switch off the power.
- Reconnect the black voice coil wire and switch on the power again.
- Press START switch and observe the following:
  a. START indicator lights and READY indicator flashes.
  b. Spindle motor starts.
  c. After about 25 seconds the heads should be loaded and the READY indicator lights steady.
- Perform head/arm alignment check as described in section 3B of the CDC Hardware Maintenance Manual. Use the CE-pack.
- Run the On-line test program.

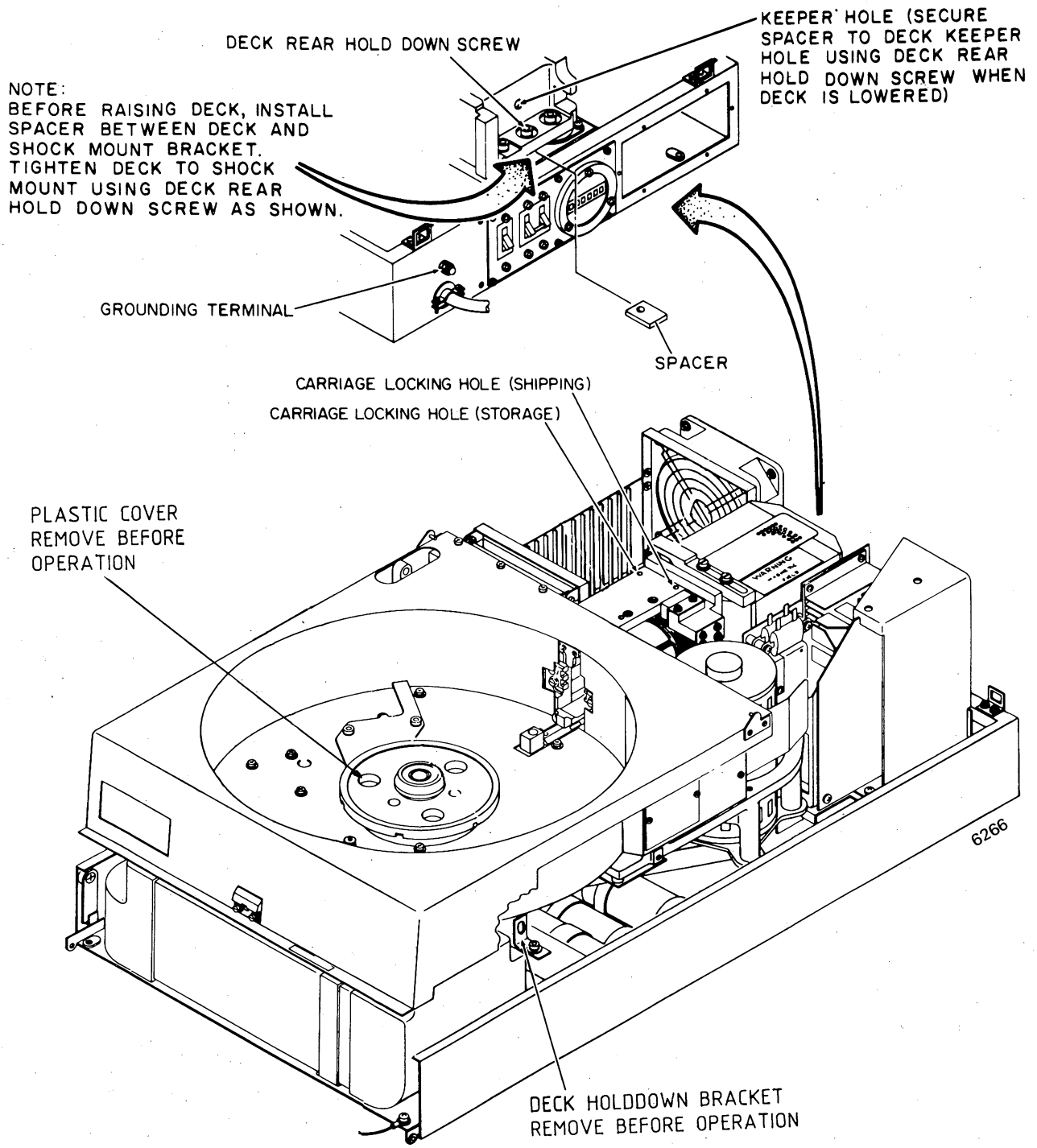


Figure 2.2.3 DRIVE SHIPPING LOCKS

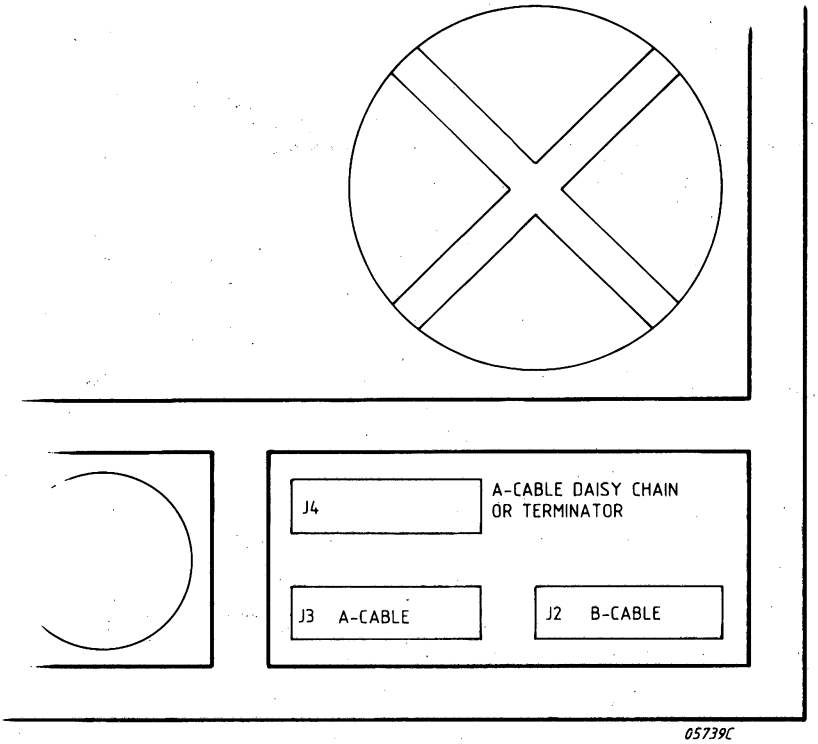


Figure 2.2.4 I/O CABLE INSTALLATION SMD (REAR OF CHASSIS)

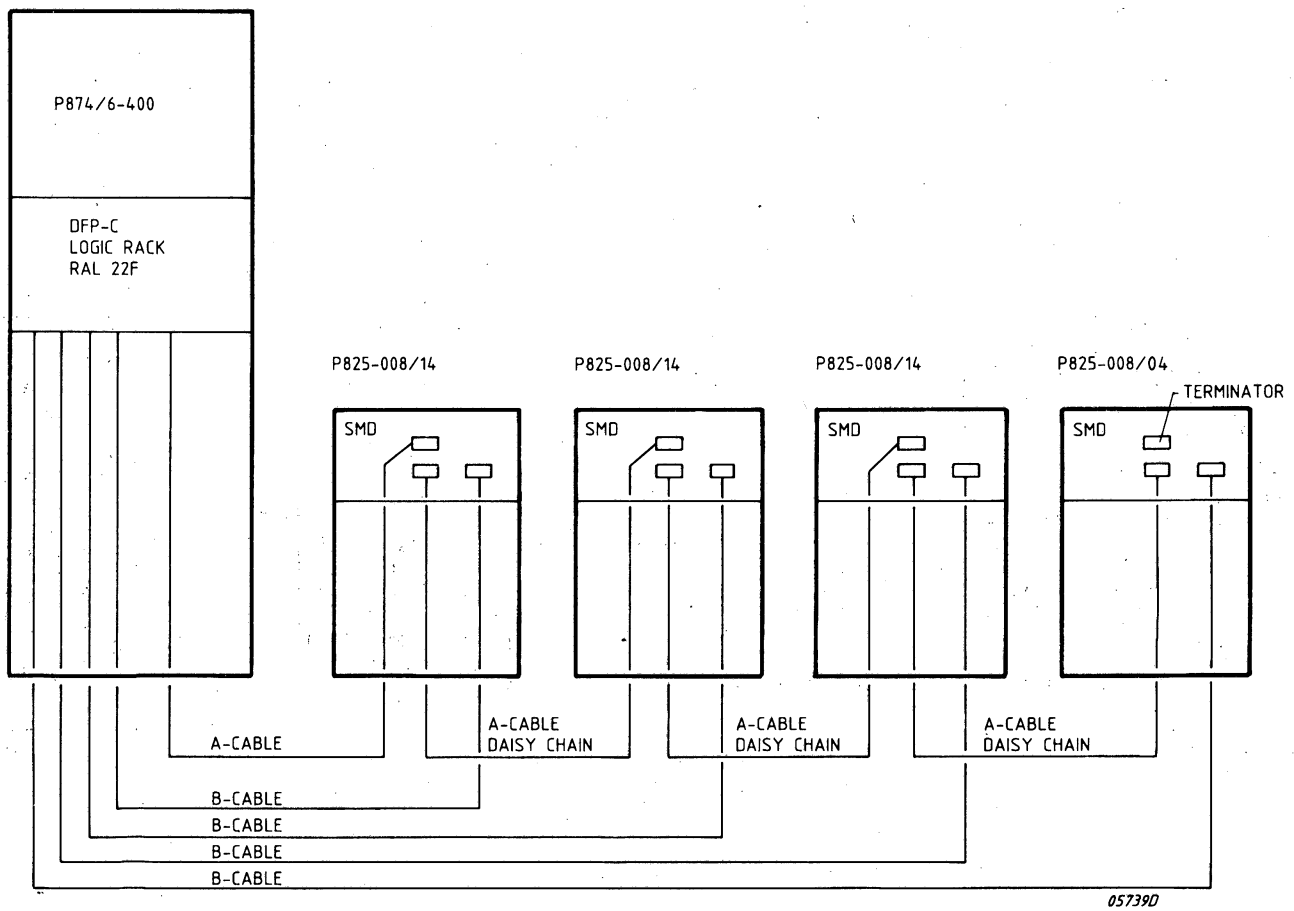


Figure 2.2.5 P874/6-400 CONFIGURATION WITH P825-008

2.2.4 CABLE SMD

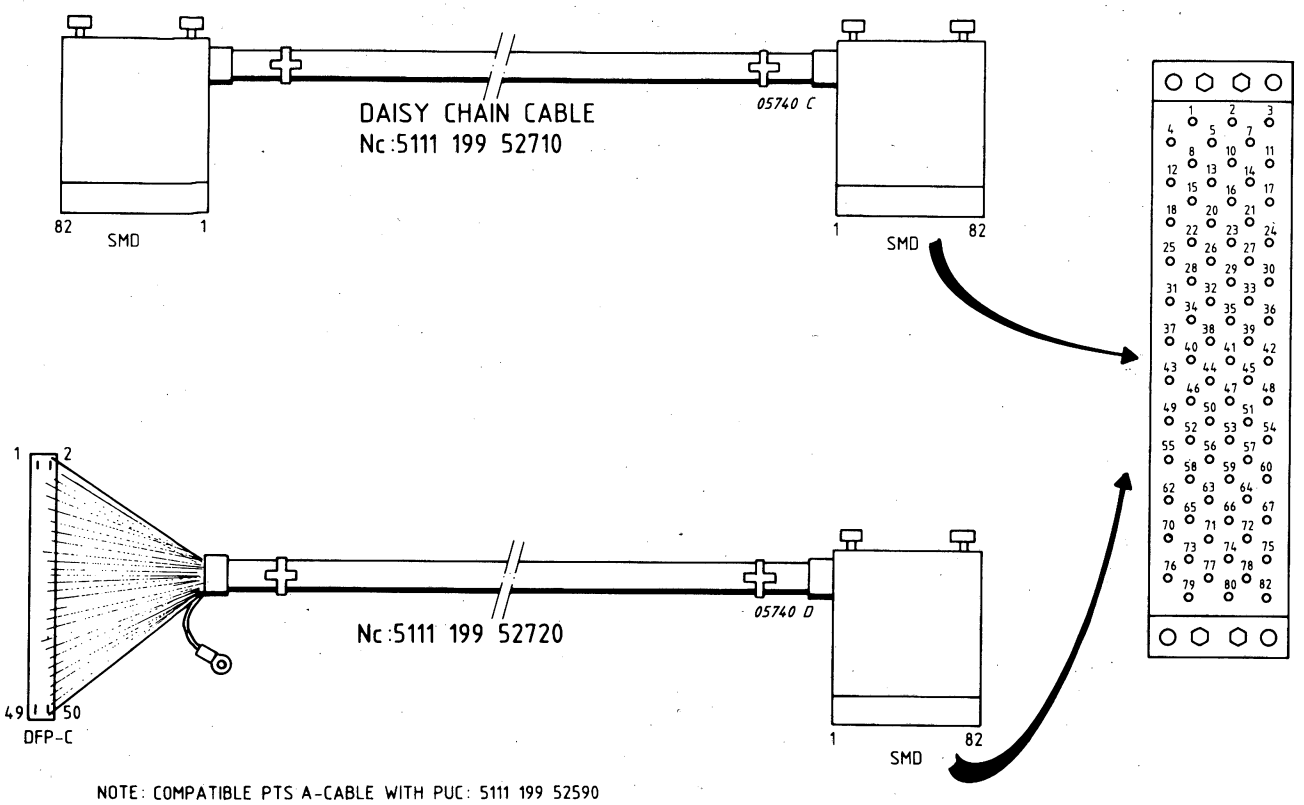


Figure 2.2.6 A-CABLES SMD

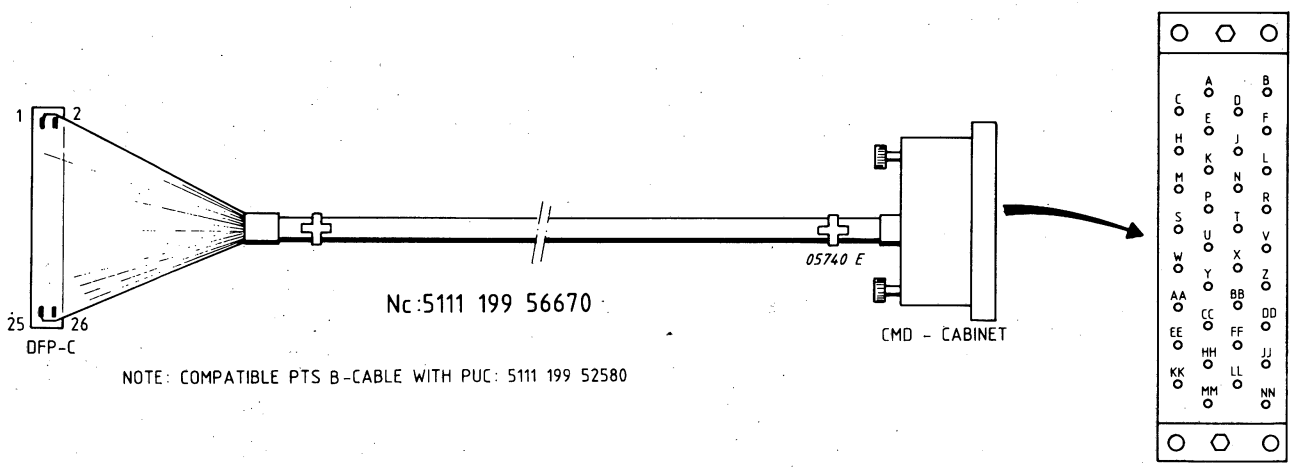


Figure 2.2.7 B-CABLE SMD/CDM

SIGNAL	BERG(CU) CONN.PIN	AMP(SMD) CONN.PIN	SIGNAL NAMES, REMARKS
A CABLE OUTPUT SIGNALS			
USL, N	45, 46	25, 22	UNIT SELECT
SC, N	1, 2	49, 46	TAG1, Cylinder Selection
HS, N	3, 4	51, 48	TAG2, Head Selection
CTS, N	5, 6	55, 52	TAG3, Control Selection
AL0, N	7, 8	26, 23	
AL1, N	9, 10	27, 24	
AL2, N	11, 12	31, 28	
AL3, N	13, 14	32, 29	
AL4 N	15, 16	33, 30	,Bit 0-9 Data Lines
AL5 N	17, 18	37, 34	
AL6 N	19, 20	38, 35	
AL7 N	21, 22	39, 36	
AL8, N	23, 24	43, 40	
AL9, N	25, 26	44, 41	
AL10, N	43, 44	- -	,Bit 10 not used
USB0, N	47, 48	4, 1	UNIT SELECT 0, Disc Adr.
USB1, N	49, 50	5, 2	UNIT SELECT 1, Disc Adr.
OCD, N	27, 28	20, 16 3, 7 8, 12	OPEN CABLE DETECTOR ,UNIT SELECT 2 and 3 are connected invertedly to OCD signal (not active)
A CABLE INPUT SIGNAL			
IX, N	39, 40	13, 10	INDEX PULSE
SEC, N	37, 38	77, 74	SECTOR PULSE
SER, N	35, 36	78, 75	SEEK ERROR
RDY, N	31, 32	21, 17	UNIT READY
WP, N	41, 42	56, 53	WRITE PROTECTED
FAULT, N	33, 34	14, 11	FAULT, Fault detected
- - - - -	(29),30	(18),15	,29 is dummy pin
B CABLE OUTPUT SIGNALS (1 set for each disc)			
WD, N	14, 15	B, A	WRITE DATA, Bit Ser.
Ground	13	D	
WC, N	12, 11	J, H	WRITE CLOCK
Ground	10	E	
B CABLE INPUT SIGNALS (1 set for each disc)			
RC, N	8, 9	X, W	READ CLOCK
Ground	7	Y	
RD, N	6, 5	V, U	READ DATA, Bit Serial
Ground	4	T	
SC, N	2, 3	N, M	SERVO CLOCK,Write Cl.Pulse
Ground	1	K	
SEN, N	19, 20	CC, AA	SEEK END
US, N	17, 18	BB, DD	UNIT SELECTED
Ground	16	C	
Ground	21	EE — HH L	,Not used (grounded)
Ground	24	FF — JJ F	,Not used (grounded)

Table 2.2.1 DFP-C INTERFACE SMD

2.2.5 SWITCH SETTINGS A03 CARD

Actual switch setting for SMD is given below.
SMD as well as CMD uses 47 sectors per track.
These switches are located on logic card A03.

NUMBER OF SECTORS	SWITCH NUMBER											
	0	1	2	3	4	5	6	7	8	9	10	11
47	0	0	C	C	C	0	0	0	C	0	0	0

C = Closed = ON
O = Open = OFF

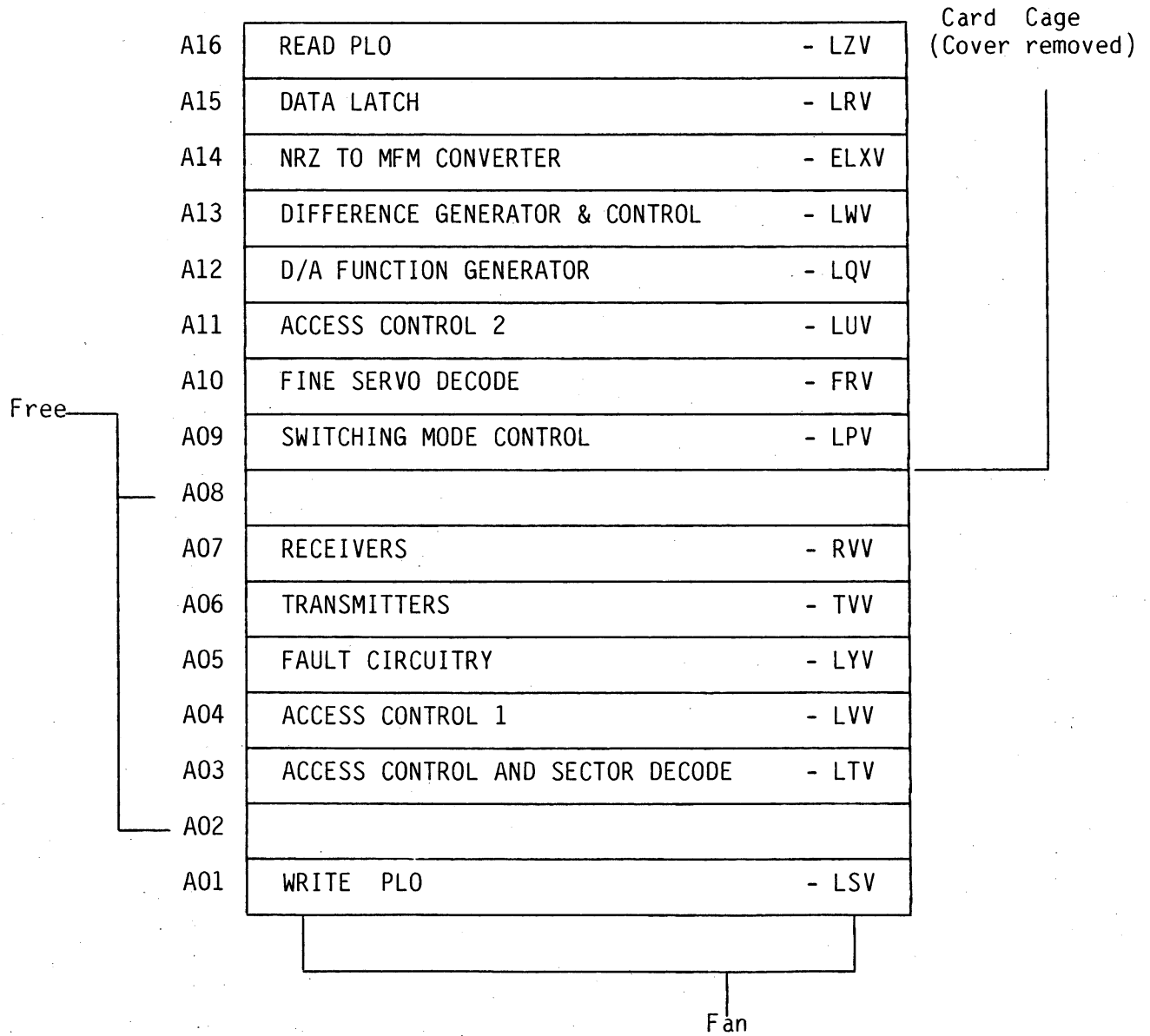
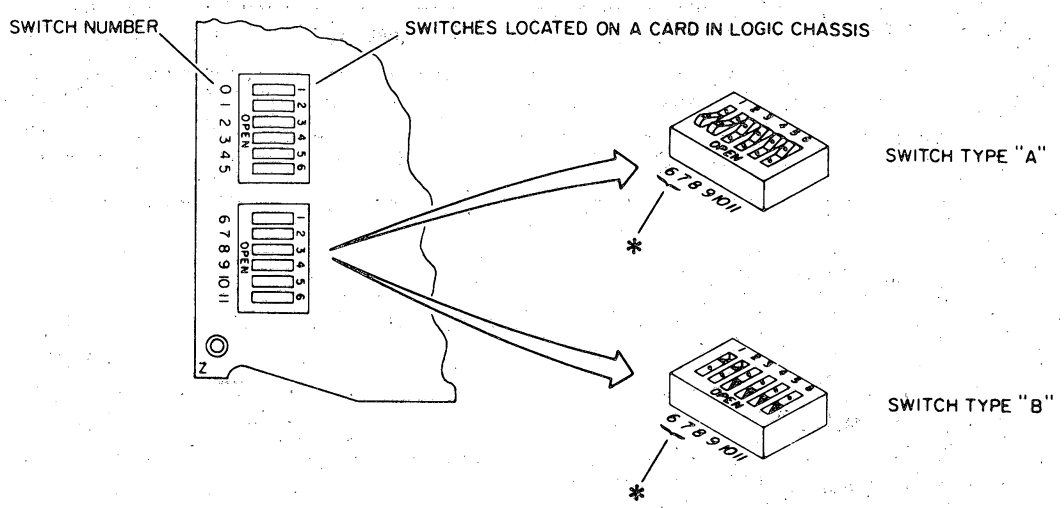


Figure 2.2.8 LOCATIONS OF LOGIC BOARDS

ROCKER-TYPE SWITCHES

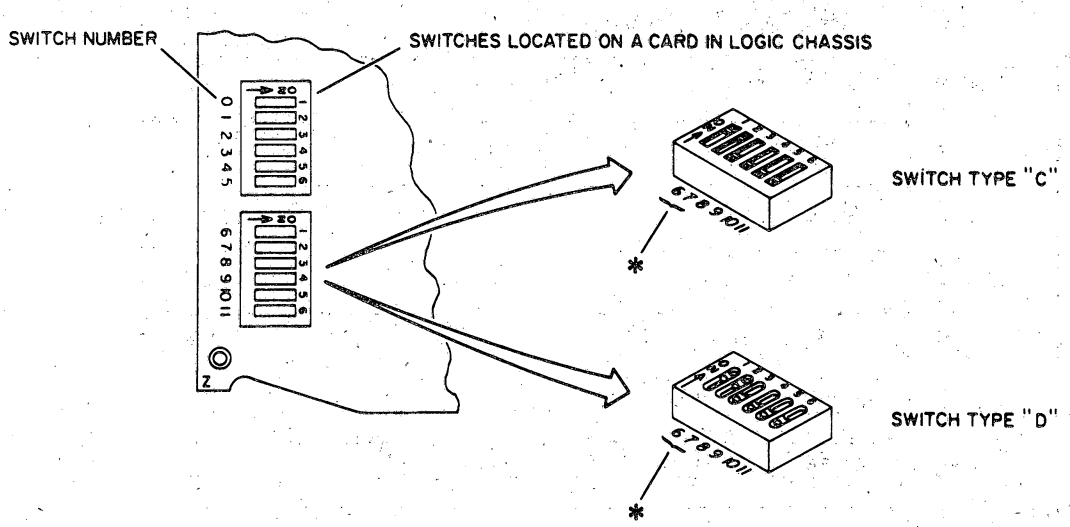


ROCKER-TYPE SWITCHES:

TO ACTUATE A SWITCH TO ITS CLOSED POSITION,
PRESS ON END OF SWITCH FARTHEST FROM "OPEN" LETTERING.

* SWITCHES 6 AND 7 SHOWN IN CLOSED POSITION.

SLIDE-TYPE SWITCHES



SLIDE-TYPE SWITCHES:

TO ACTUATE A SWITCH TO ITS ON POSITION,
SLIDE SWITCH IN DIRECTION OF ARROW SHOWN ON SWITCH.

* SWITCHES 6 AND 7 SHOWN IN ON POSITION.

Figure 2.2.9 SECTOR SELECT SWITCHES

2.3 DISC CABINETS P825-011/12

2.3.1 IDENTIFICATIONS

P825-011/04	DISC DRIVE 64MB (IST. DRIVE) EURO	
	DISC DRIVE CMD 9448-64	5111 010 07980
	CABLE "B" CMD 7.5M	5111 199 56670
	CABLE "A" CMD 7.5M	5111 199 56680
	KIT MOUNTING CMD	5111 199 60330
	DISTRIBUTION PANEL	5111 199 60450
	CABINET CMD ASSEMBLY	5111 199 61270
	CABLE ADAPTATION "B"	5111 199 61480
	CABLE ADAPTATION "A"	5111 199 61490
	KIT PRE-FILTER	5111 291 72891
P825-011/04	DISC DRIVE 64MB (2ND. DRIVE) EURO	
	SAME AS P825-011/04, EXCEPT:	
	CABLE "A" DAISY CH (INSTEAD OF CABLE "A")	5111 199 60340
	CABLE ADAPTATION "A" EXTRA (TOTAL 2 CABLES)	5111 199 61490

DISC CABINETS P825-012

P825-012/04	DISC DRIVE 96MB (1ST. DRIVE) EURO	
P825-012/14	DISC DRIVE 96MB (2ND. DRIVE) EURO	
	SAME AS P825-011, EXCEPT	
	DISC DRIVE CMD 9448-96	5111 010 07970
P825-201	DISC CARTRIDGE 16MB FOR P825-011/12	5111 199 21001

2.3.2 OPERATING DISC UNIT

To install a cartridge:

. Make certain that; the power is on, the START/STOP switch is out and that the indicators READY and FAULT are off.

. Release latch under lip of access door recess and pull down cartridge access door.

. To separate dust cover from the disc caridge, push cover release button on the bottom dust cover toward the center of the cartridge.

. Slide the disc cartridge into the receiver track in the direction of the plastic arrow on the top dust cover, so that the guide pins on the top dust cover ride smoothly in the receiver track. Use the cartridge handle to insure proper horizontal insertion of the cartidge and engagement of the guide pines in the receiver track.

. Push the top-cover handle down. Push the cartridge rearward until it stops.

. close the cartridge access door and press the door closed until it is latched. The cartridge slides into place and centers on the spindle automatically as the access door is closed.

. Store cartridge cover upside down in some convenient location.

. Operate START/STOP switch to apply power to spindle motor.

NOTE

If the spindle motor will not rotate, disc cartridge access door may not be completely closed, the cartridge may not be properly seated on the spindle chunk or the cartridge receiver/base may not be all the way down on the lower chassis.

To remove a cartridge:

. Operate START/STOP switch to STOP (out).

. Pull down the cartridge access door after the READY indicator ceases blinking and extinguishes entirely.

. Grasp the cartridge handle and pull the cartridge out of the receiver with sufficient force to overcome the detent action.

. Replace the bottom dust cover by lining up the arrows on the top and bottom covers, so that the guide bars on the bottom cover slip into the slots on the top cover.

. When the covers are properly aligned they will lock automatically with a gentle downward pressure on the top cover.

NOTE

A disc cartridge should be installed at all times, whether operating or not, to insure proper sealing of the shroud area from environmental contaminents.

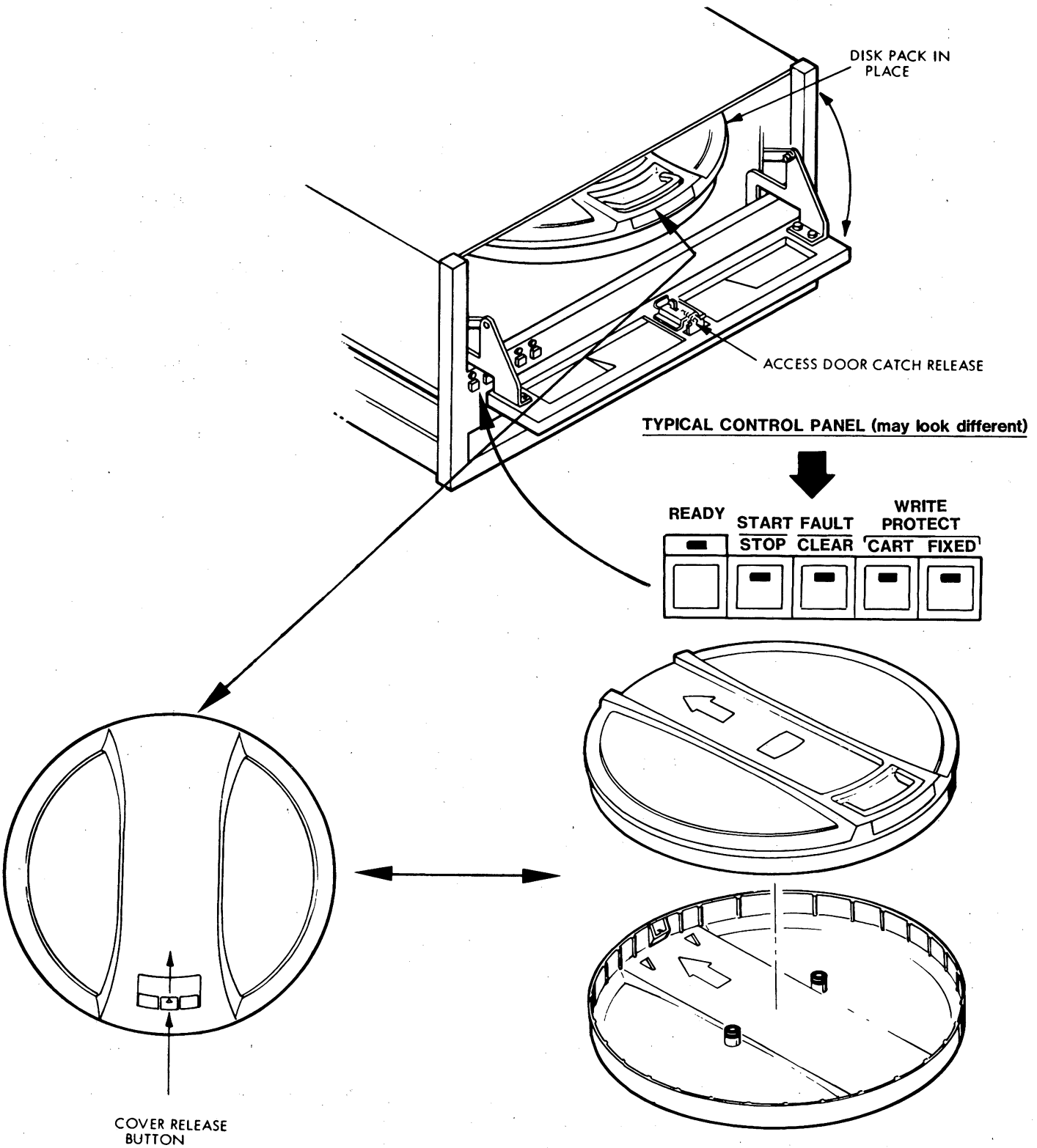


Figure 2.3.1 OPERATING CARTRIDGE DISC UNITS P825-011/012

2.3.3 INSTALLATION DISC UNIT

1. Pack unit conform figure below.
2. Put def track list in space for documentation.
3. Close packing and secure cardboard to pallet with two packaging strips or ropes.

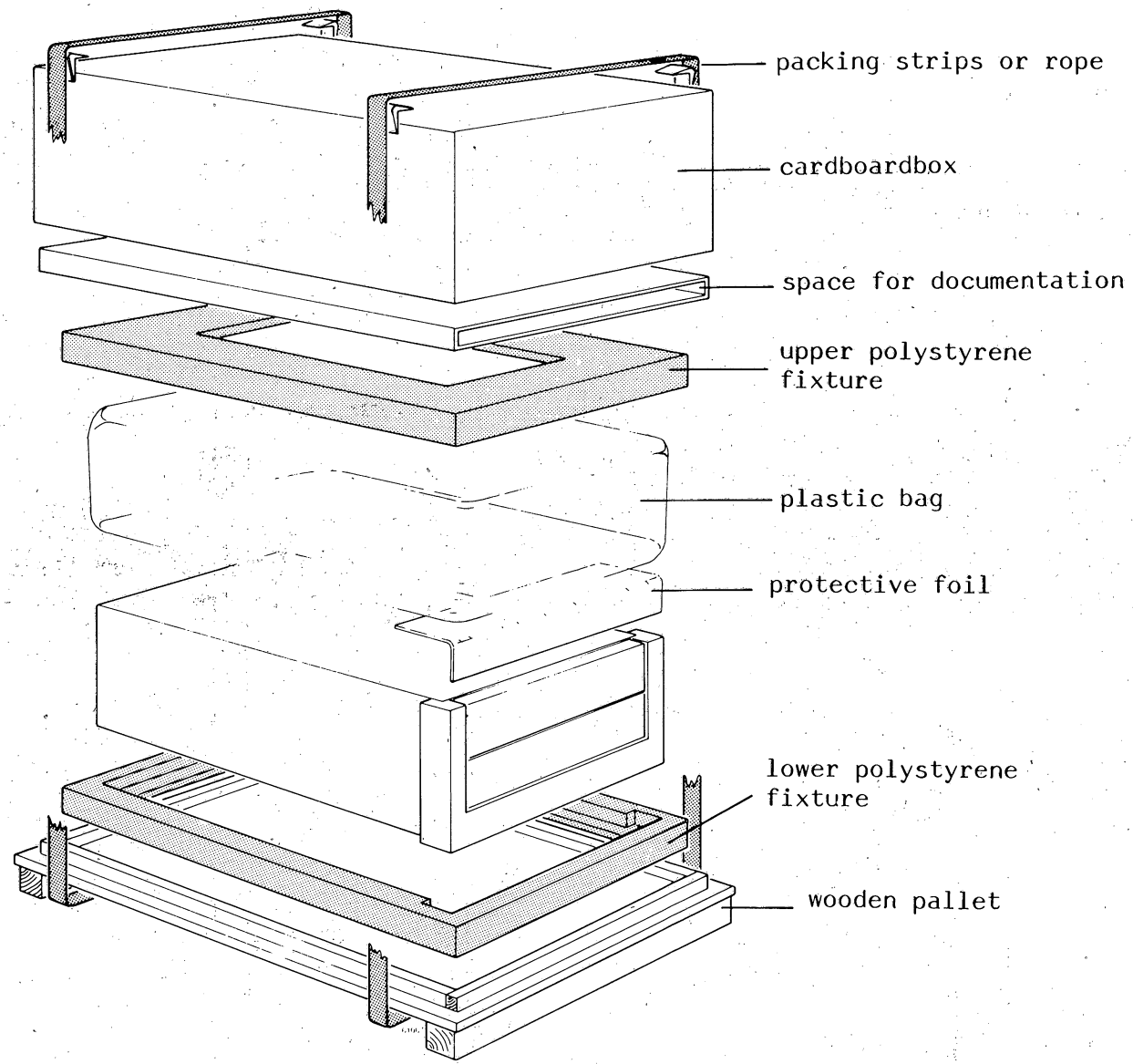


Figure 2.3.2 PACKING/UNPACKING

During unpacking exercise care, so that any tools being used do not cause damage to the unit. As the unit is unpacked inspect it for possible shipping damage. All claims of this type should be filed promptly with the transporter involved. If a claim is filed for damages, save the original packing materials.

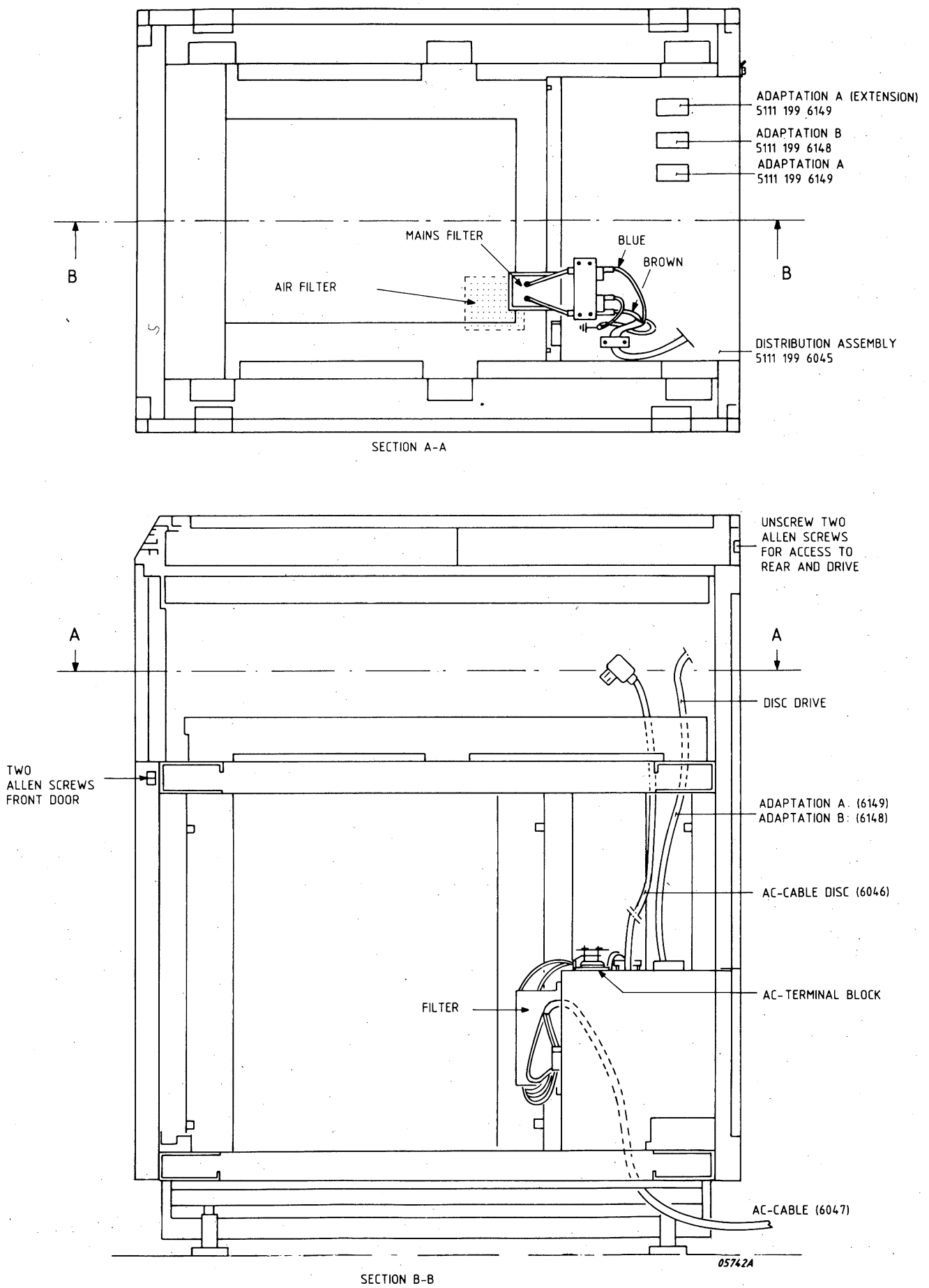


Figure 2.3.3 CABINET P825-011/12

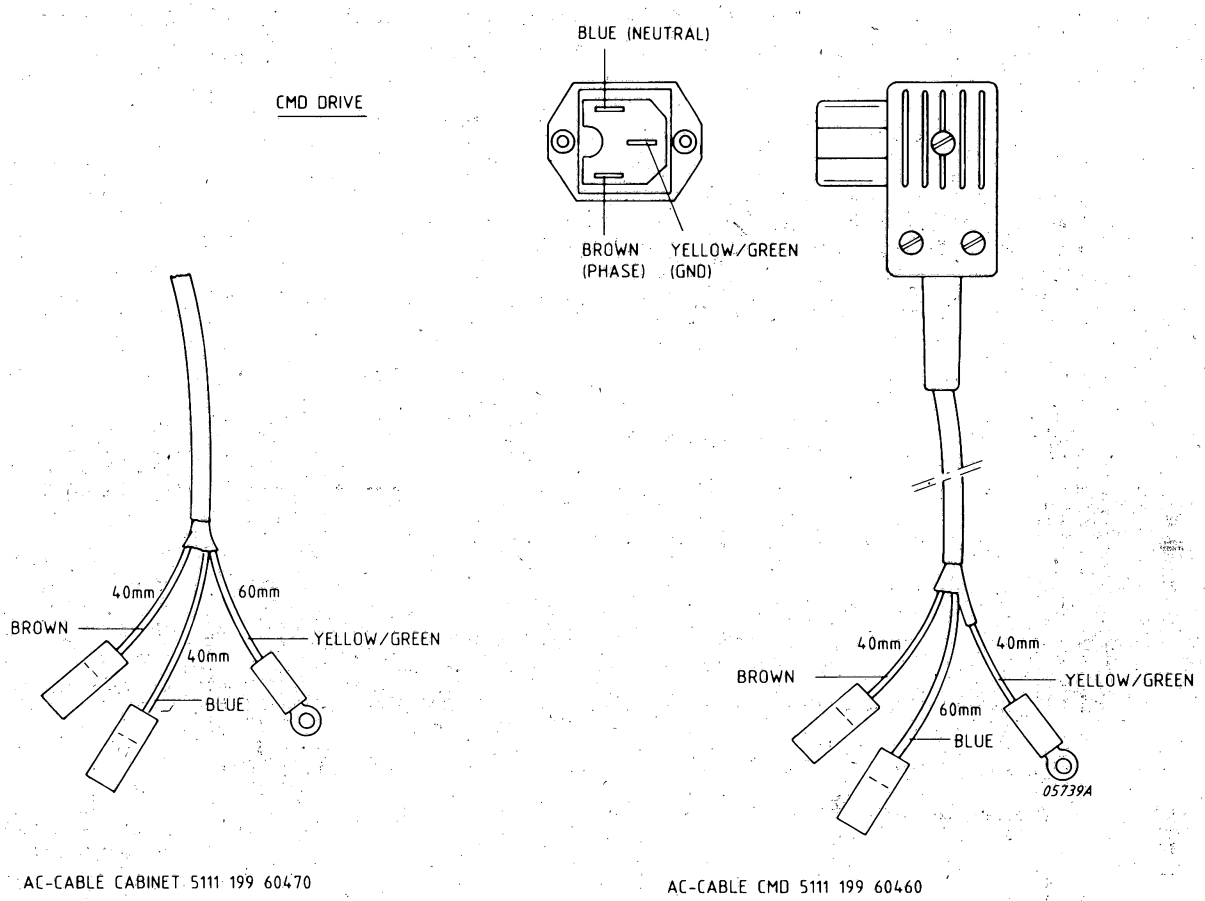


Figure 2.3.4 AC-CABLES CABINET/DRIVE

Before installing the drive some panels must be removed from cabinet.
To remove the panels proceed as follows (see figures of cabinet):

Unscrew the two ALLAN screws at the rear top (c).
Take off the horizontal bar and lift of the rear panel.
Disconnect the ground wire from chassis.
Unscrew the two screws fixing the top cover at the rear (d) of the cabinet, slide the top cover backwards and lift it off the cabinet.

If necessary, the two side panels can be lifted off after unscrewing two bolts inside the cabinet. The two bolts are accessible via two holes in the power and interface assembly, or after removal of this assembly (4 screws at rear and 2 screws at the cabinet-bottom).

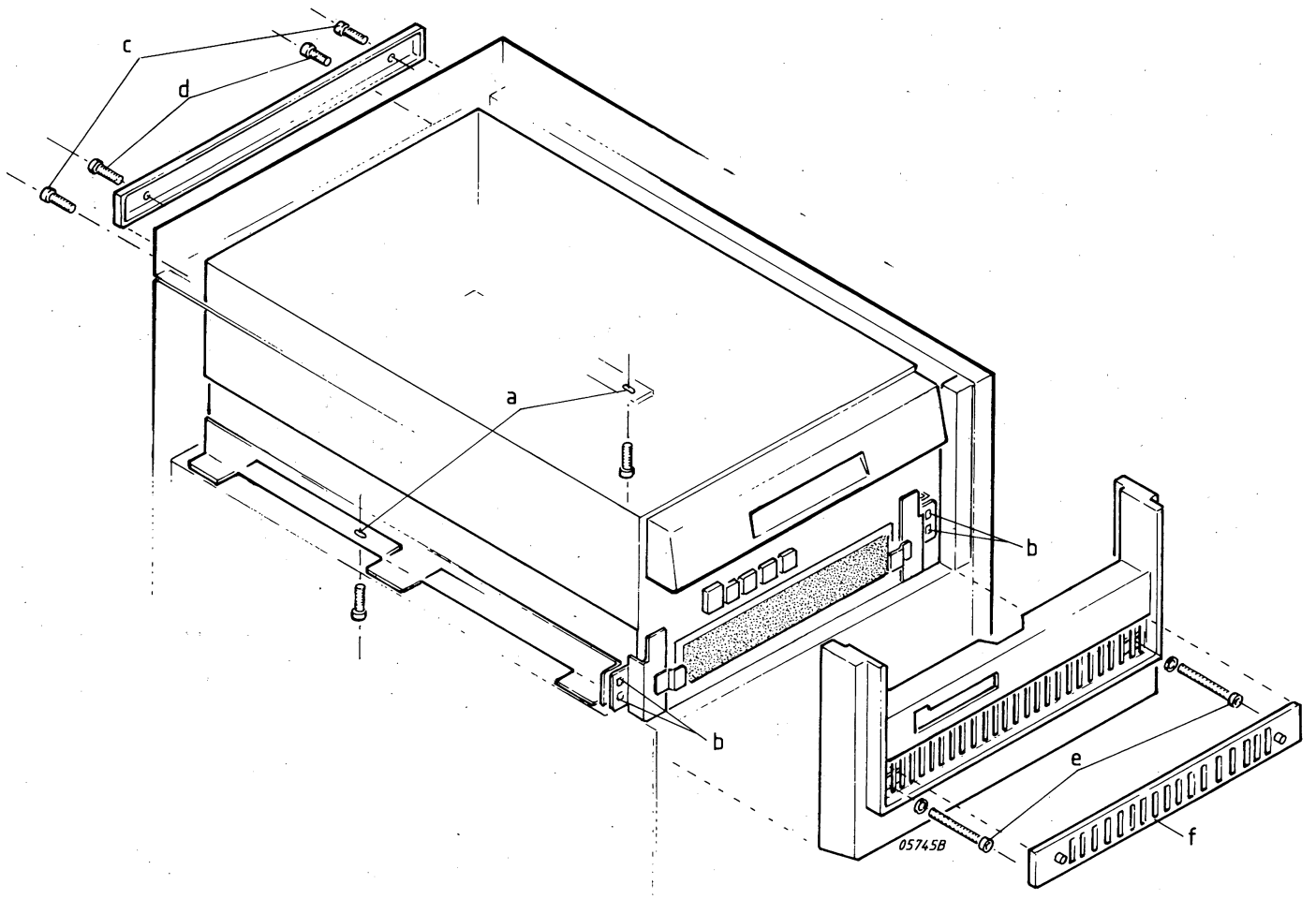


Figure 2.3.5 INSTALLATION OF CMD DRIVE

1. Place CMD at the top of the cabinet
2. Fix screws a (2) and b (4)
3. Mount front cover plate and fix it by means of Allen Screws (e)
4. Place airfilter (f)

Remark: To direct the Allen screws correctly in the holes top cover of the CMD can be shifted backwards after loosening two fixing screws at the back.

Dismantle the unit as follows:

A Remove the top cover and inspect various items such as circuit boards, carriage assembly and read/write heads for shipping damage.

B Check that all packing material pieces are removed and that the unit is clean inside.

C Remove the screw (4) which secures the carriage locking tool (1). Lift the Locking tool to remove the pin (2) from the hole in the carriage (6). Swing the locking tool around to the operating position on (B). Reinstall the screw to secure the locking tool to the magnet in the operating position.

CAUTION:
Do not position the carriage manually. Such action could cause the read/write heads to load and to cause damage to the heads and disks. The unit should never be shipped or even be moved any significant distance without the carriage lock pin in place in prevent the heads from loading and damaging the discs and/or heads.

D Remove rear shipping bolt (C), using a 3/16 inch hex driver.
Stop the shipping bolt in the hold provided to the left of magnet as shown at (D) in the figure. Before shipping this bolt must be installed in the centre hole again.

E Remove and discard the screws (F) that secure the Electronics Module to the base pan for shipping. Screws (E) also secure the Electronics Module but these should not be removed until it is necessary to access the bottom of the Electronics Module. The screws (E) should not be discarded but replaced when accessing of the bottom of the Electronics module is completed.

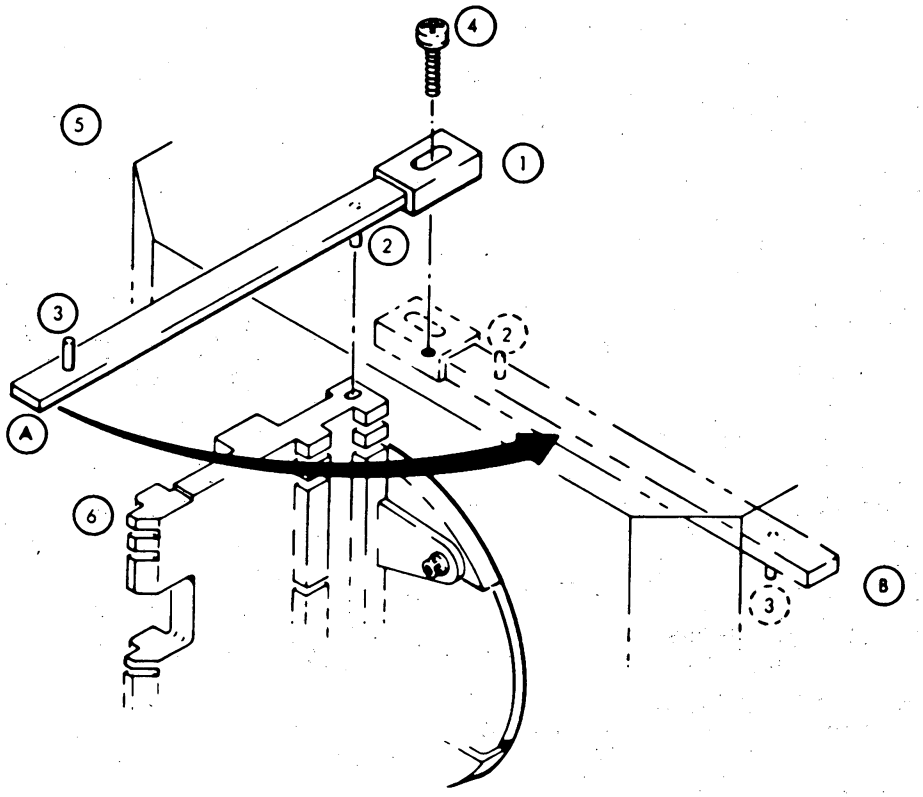
F Remove deck hold down bolts and stow them below the deck in the base pan together with all the hardware as shown.
Before re-shipping the unit, re-install the bolts in the position as shown.

G If deck hold down bolts (A) were removed to raise deck these should be replaced before placing the unit in operating. Before re-shipping the unit it should be inspected to make certain that the "A" bolts and the "B" bolts have been securely installed (See Note:).

H Replace the unit cover. The cover should remain installed even if the unit is to be operated within a rack.

I A plastic cover is shipped in place of a cartridge. Remove the plastic cover and install a cartridge before operating.

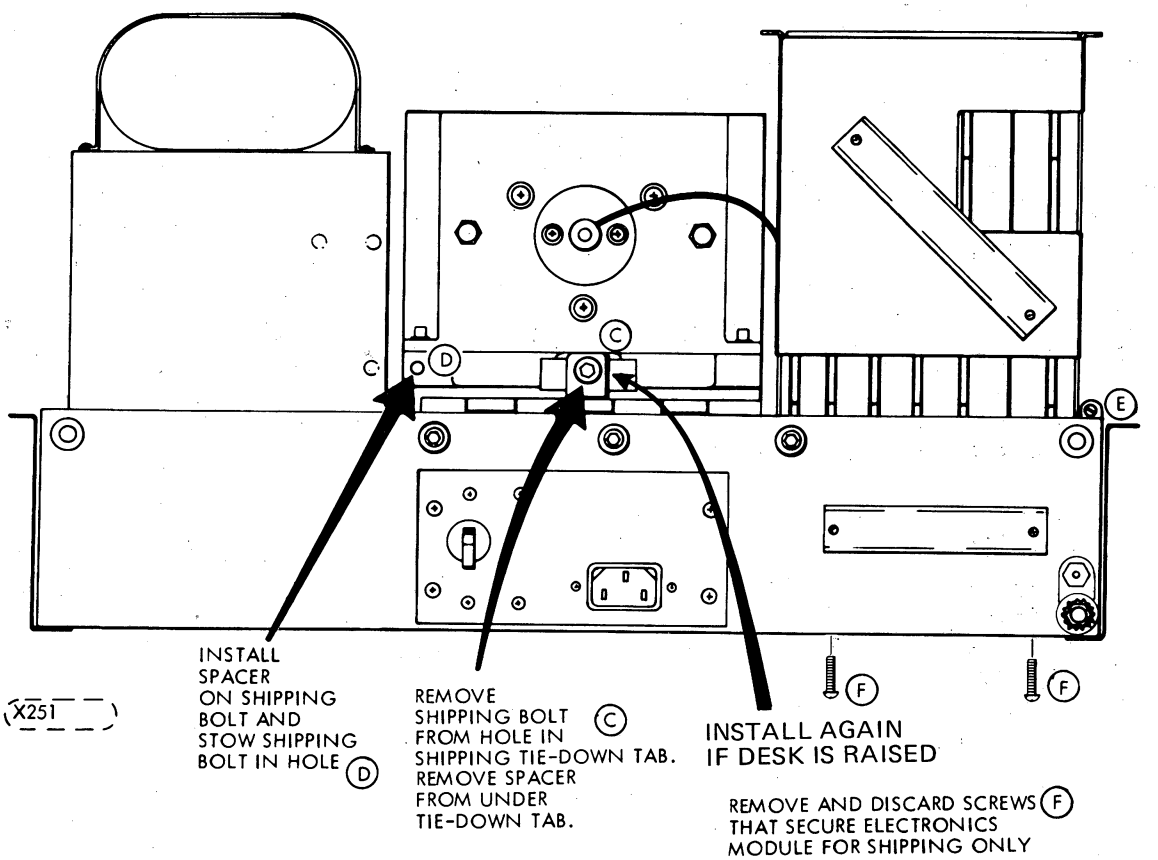
Note: Disconnect the voice coil leads and switch on power. Let the disc run for approx. 20 minutes with the voice coil leads disconnected to blow away dust particles without the risk of head crash.
The best is to do this with raised deck.
Stop the drive and repeat this with the deck in normal position for about 5 minutes.
Switch off the drive and power and connect the voice coil again.
This procedure is also useful after any change of air filters.



X231a

(A) CARRIAGE LOCK PIN (1) IN SHIPPING POSITION
(B) CARRIAGE LOCK PIN (1) IN OPERATING POSITION

Figure 2.3.6 CARRIAGE LOCKING TOOL - SHIPPING POSITON



X251

Figure 2.3.7 REAR SHIPPING BOLT LOCATION

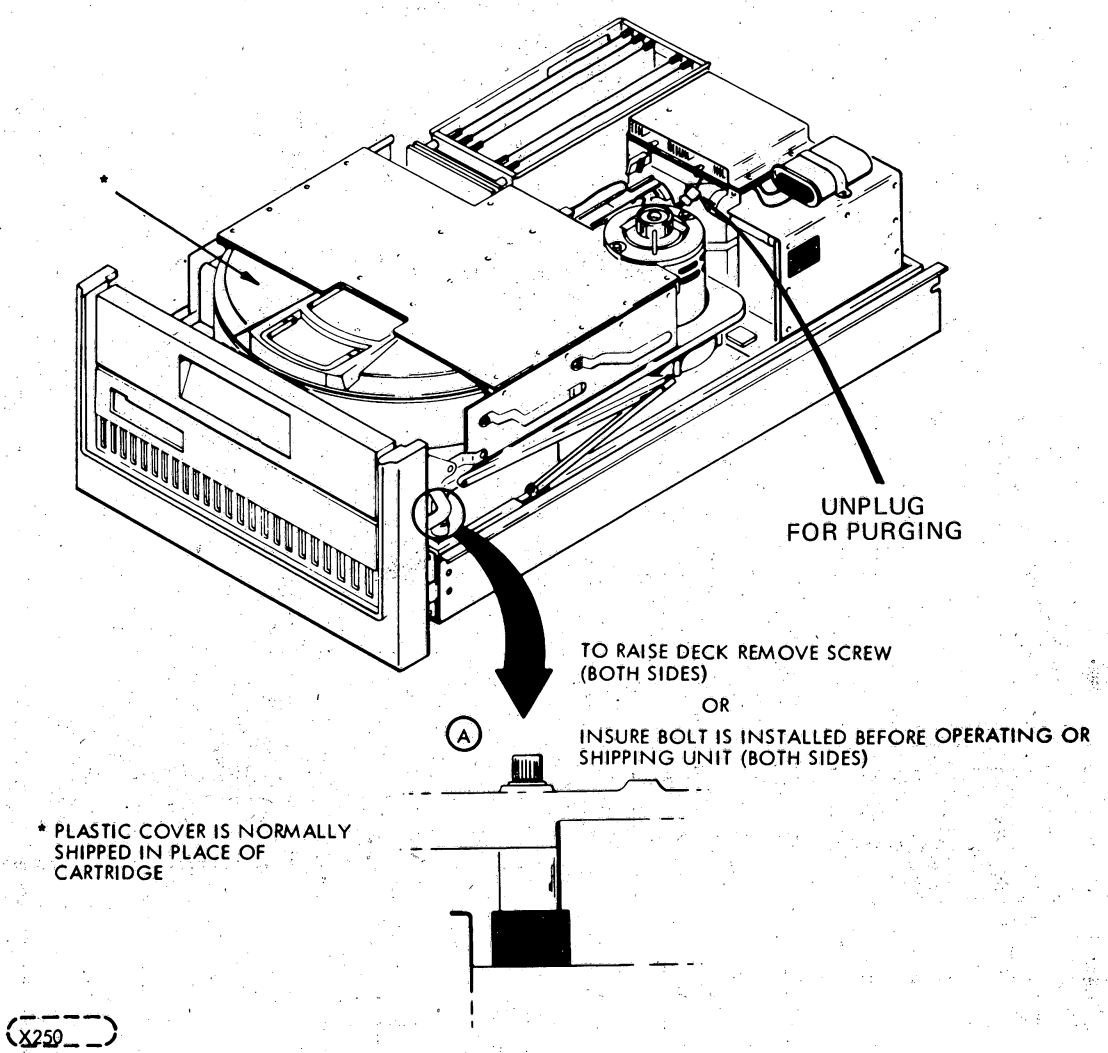
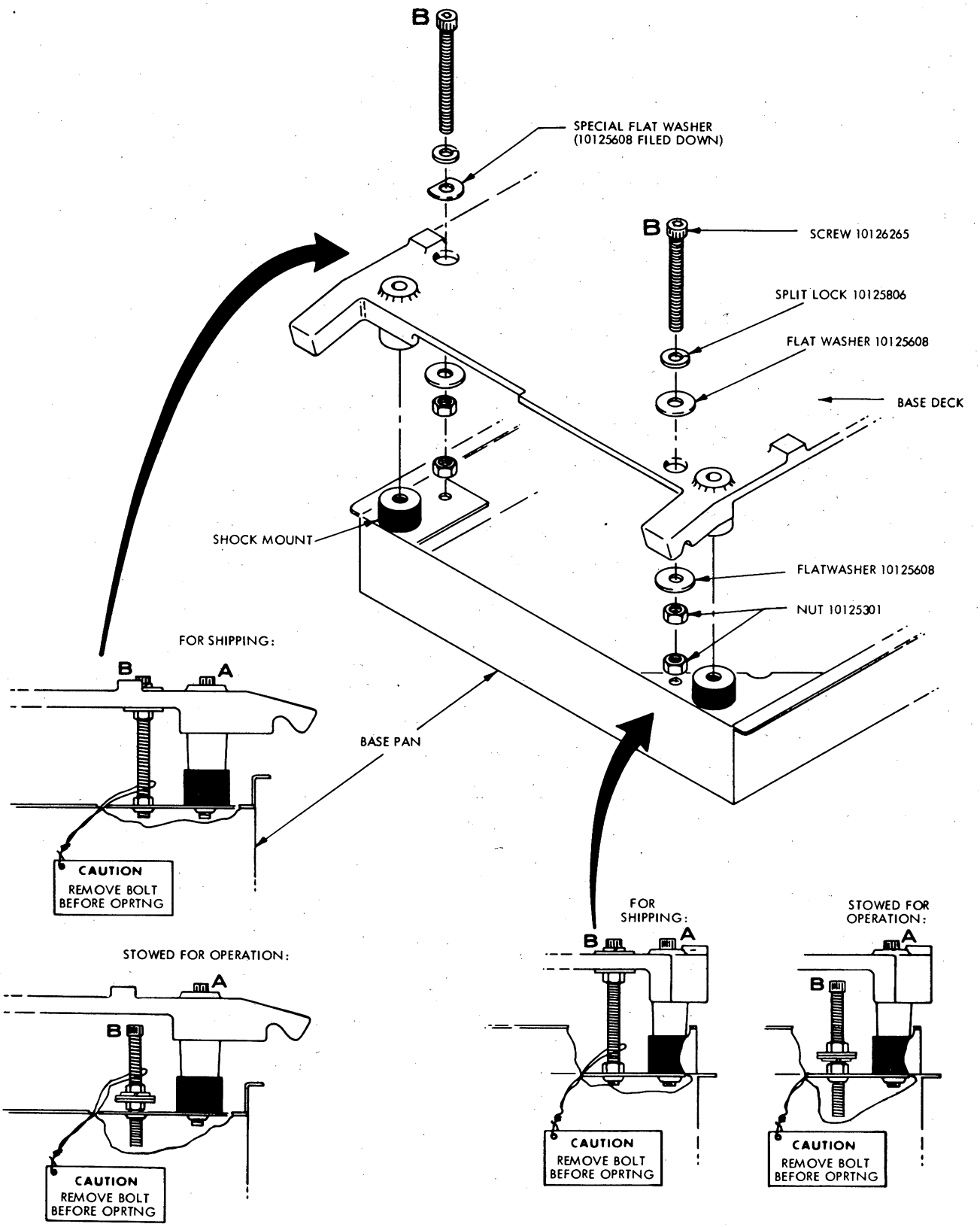


Figure 2.3.8 DECK HOLD DOWN BOLTS (1)



NOTE: RETAIN CAUTION TAG FOR POSSIBLE FUTURE SHIPPING

Z107

Figure 2.3.9 DECK HOLD DOWN BOLTS (2)

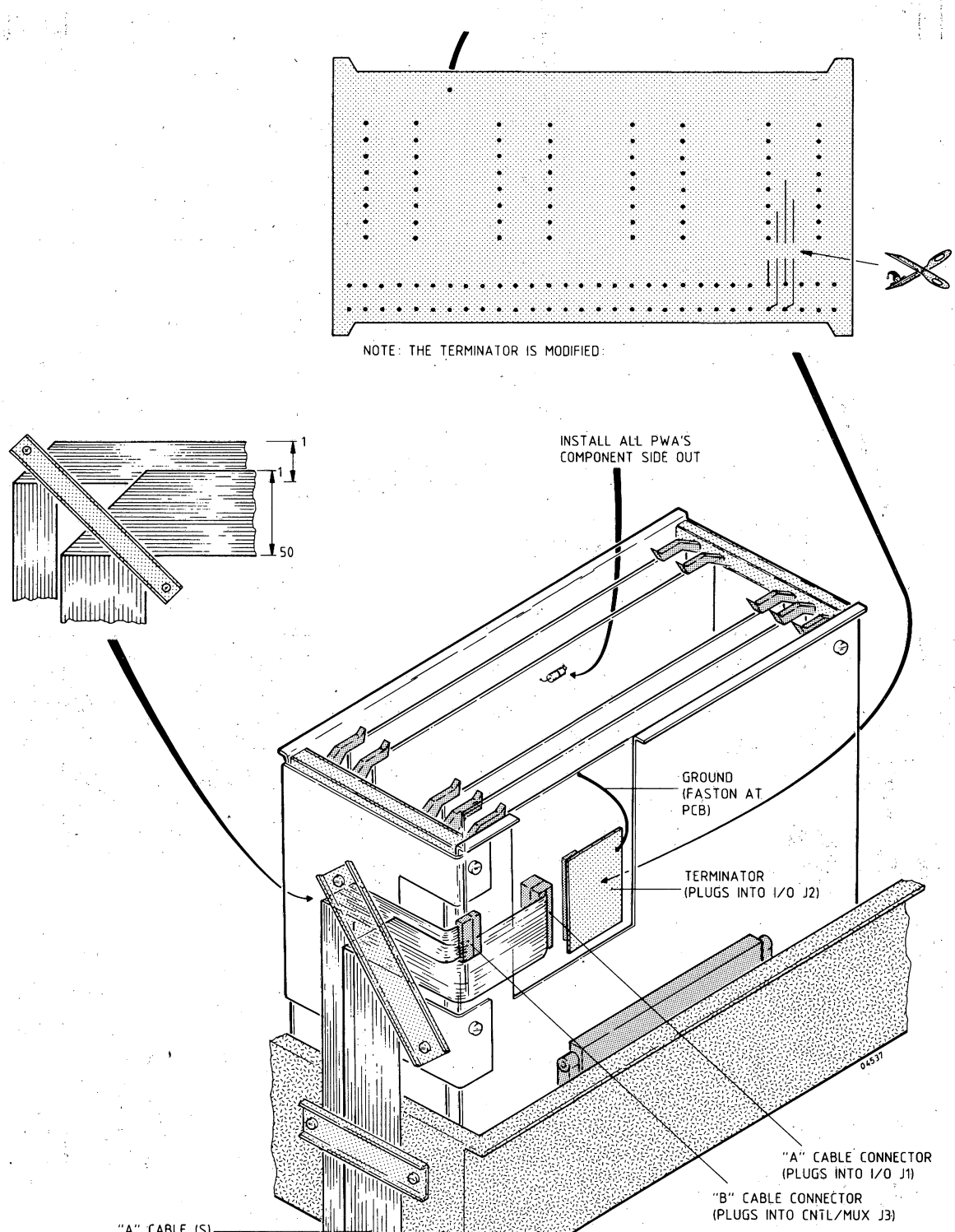


Figure 2.3.10 I/O CABLE INSTALLATION AND PCB NAMES/LOCATIONS

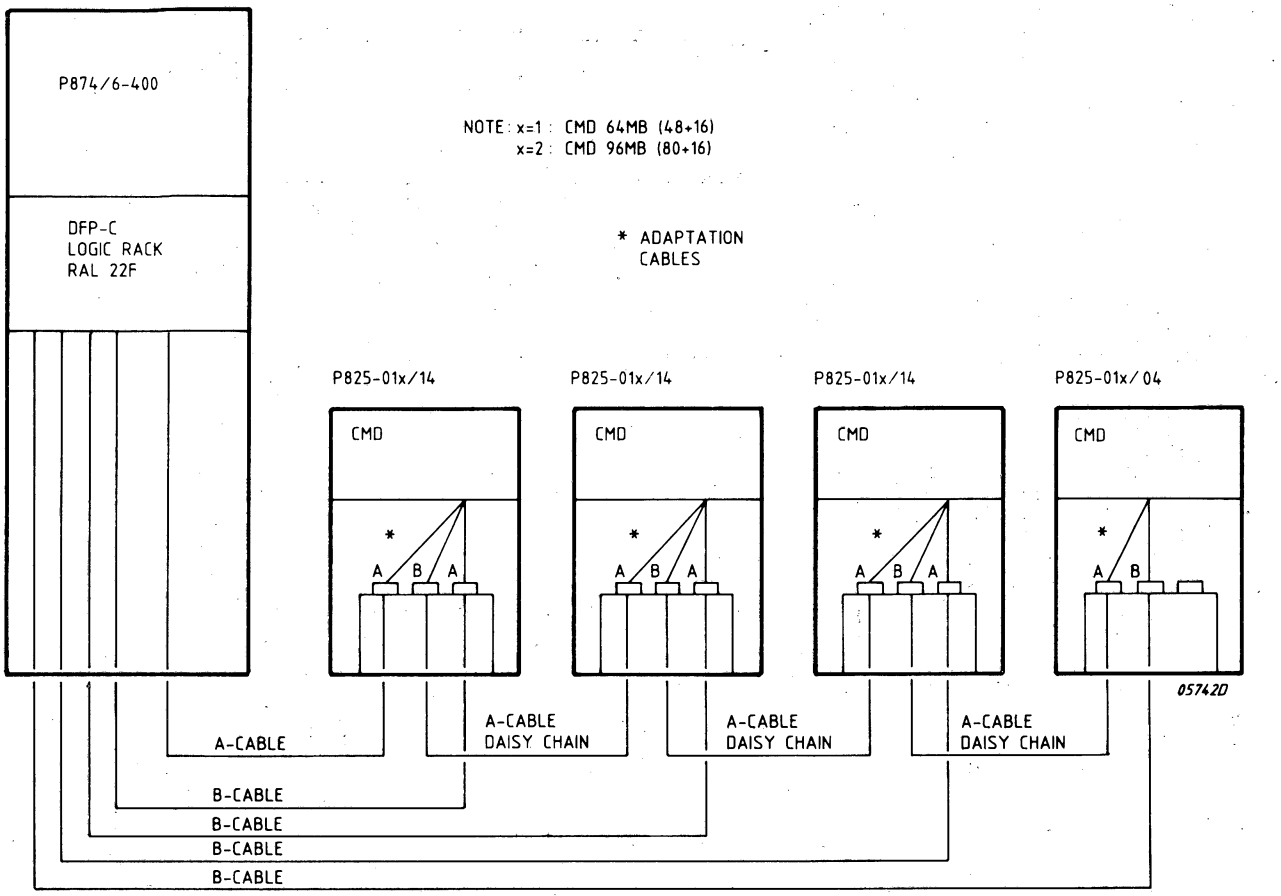


Figure 2.3.11 P874/6-400 CONFIGURATION WITH P825-011/12

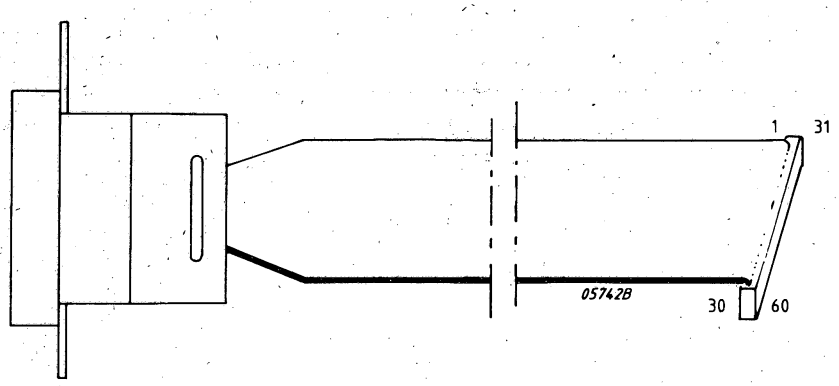


Figure 2.3.12 ADAPTATION A-CABLE (CMD), 5111 199 61490

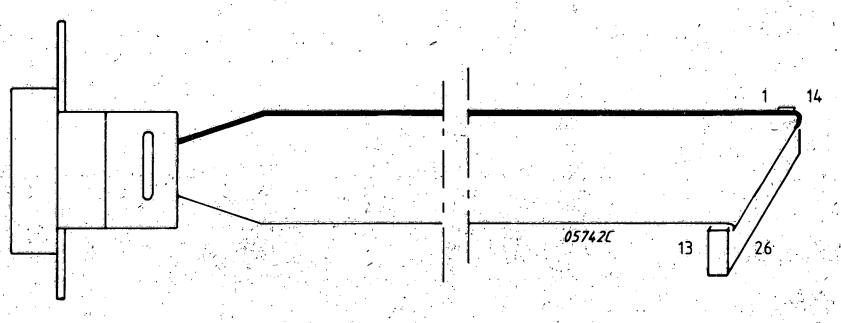


Figure 2.3.13 ADAPTATION B-CABLE (CMD), 5111 199 61480

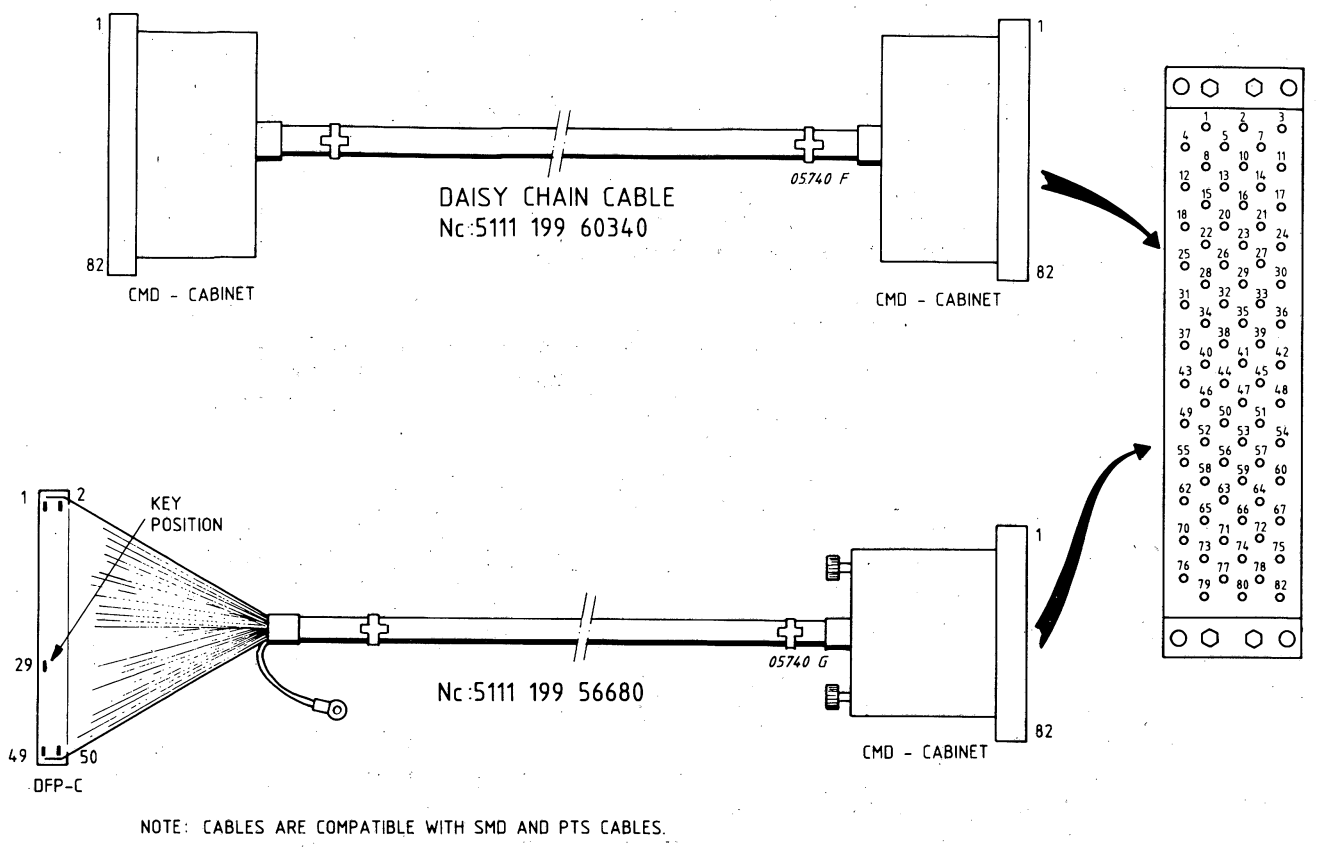


Figure 2.3.14 A-CABLES CMD (P800)

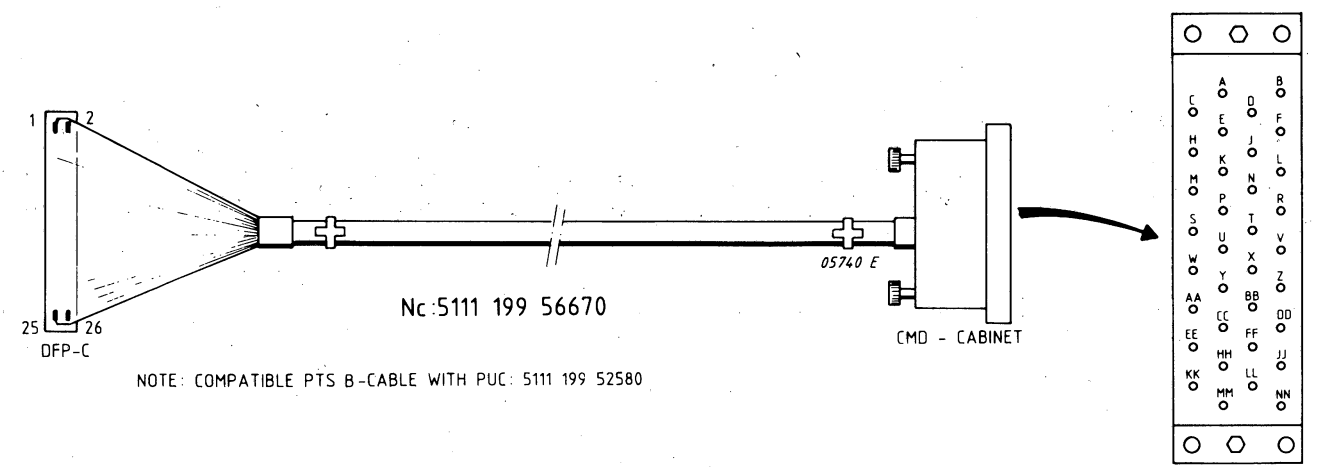


Figure 2.3.15 B-CABLE SMD/CMD (P800)

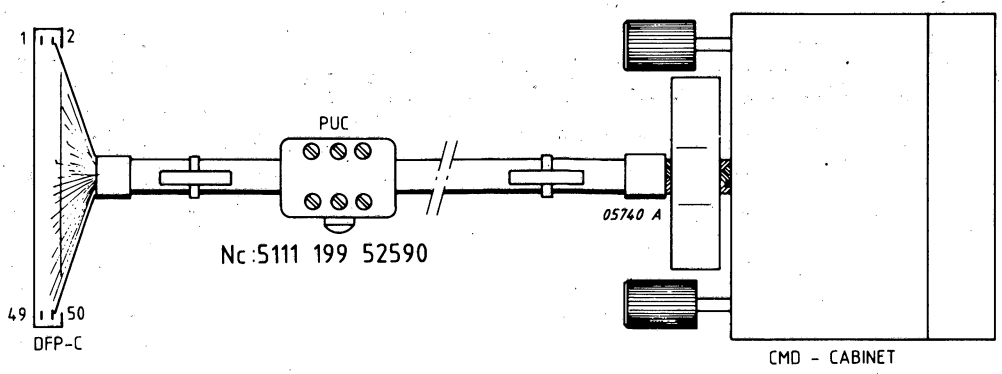


Figure 2.3.16 A-CABLE (PTS) COMPATIBLE WITH P800 (PUC SYSTEM)

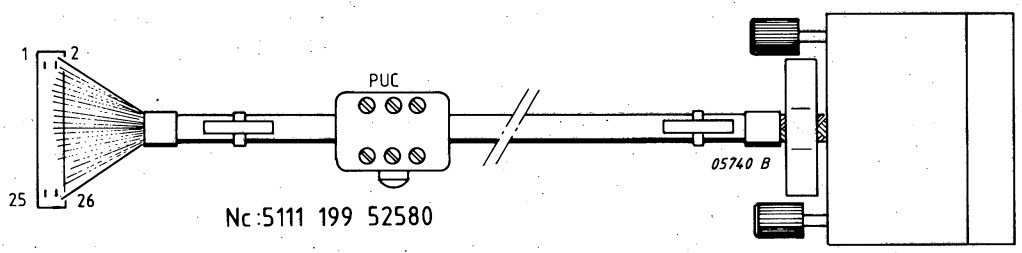


Figure 2.3.17 B-CABLE (PTS) COMPATIBLE WITH P800 (PUC SYSTEM)

CDC-TERMINATOR

The A-Cable terminator, 12NC: 5112 291 64841, must be used in CMD-files. Four tracks, unit select 2 (pin 26 and 56) and unit select 3 (pin 27 and 57), are out.

SIGNAL	BERG(CU) CONN.PIN	AMP(SMD) CONN.PIN	SIGNAL NAMES, REMARKS	CMD DRIVE CONN.PIN
A CABLE OUTPUT SIGNALS				
USL, N	45, 46	25, 22	UNIT SELECT	52, 22
SC, N	1, 2	49, 46	TAG1, Cylinder Selection	31, 1
HS, N	3, 4	51, 48	TAG2, Head Selection	32, 2
CTS, N	5, 6	55, 52	TAG3, Control Selection	33, 3
AL0, N	7, 8	26, 23		34, 4
AL1, N	9, 10	27, 24		35, 5
AL2, N	11, 12	31, 28		36, 6
AL3, N	13, 14	32, 29		37, 7
AL4 N	15, 16	33, 30	,Bit 0-9 Data Lines	38, 8
AL5 N	17, 18	37, 34		39, 9
AL6 N	19, 20	38, 35		40, 10
AL7 N	21, 22	39, 36		41, 11
AL8, N	23, 24	43, 40		42, 12
AL9, N	25, 26	44, 41		43, 13
AL10, N	43, 44	- -	,Bit 10 not used	- -
USB0, N	47, 48	4, 1	UNIT SELECT 0, Disc Adr.	53, 23
USB1, N	49, 50	5, 2	UNIT SELECT 1, Disc Adr.	54, 24
OCD, N	27, 28	20, 16 3, 7 8, 12	OPEN CABLE DETECTOR ,UNIT SELECT 2 and 3 are connected invertedly to OCD signal (not active)	44, 14 26, 56 27, 57
A CABLE INPUT SIGNAL				
IX, N	39, 40	13, 10	INDEX PULSE	48, 18
SEC, N	37, 38	77, 74	SECTOR PULSE	55, 25
SER, N	35, 36	78, 75	SEEK ERROR	46, 16
RDY, N	31, 32	21, 17	UNIT READY	49, 19
WP, N	41, 42	56, 53	WRITE PROTECTED	58, 28
FAULT, N	33, 34	14, 11	FAULT, Fault detected	45, 15
- - - - -	(29), 30	(18), 15	,29 is dummy pin	(47), 17
B CABLE OUTPUT SIGNALS (1 set for each disc)				
WD, N	14, 15	B, A	WRITE DATA, Bit Ser.	20, 8
Ground	13	D		7
WC, N	12, 11	J, H	WRITE CLOCK	19, 6
Ground	10	E		18
B CABLE INPUT SIGNALS (1 set for each disc)				
RC, N	8, 9	X, W	READ CLOCK	17, 5
Ground	7	Y		4
RD, N	6, 5	V, U	READ DATA, Bit Serial	16, 3
Ground	4	T		15
SC, N	2, 3	N, M	SERVO CLOCK,Write Cl.Pulse	14, 2
Ground	1	K		1
SEN, N	19, 20	CC, AA	SEEK END	23, 10
US, N	17, 18	BB, DD	UNIT SELECTED	9, 22
Ground	16	C		21
Ground	21	EE — HH, L	,Not used (grounded)	12, 24 11
Ground	24	FF — JJ, F	,Not used (grounded)	13, 26 25

Table 2.3.1 DFP-C INTERFACE SMD/CMD

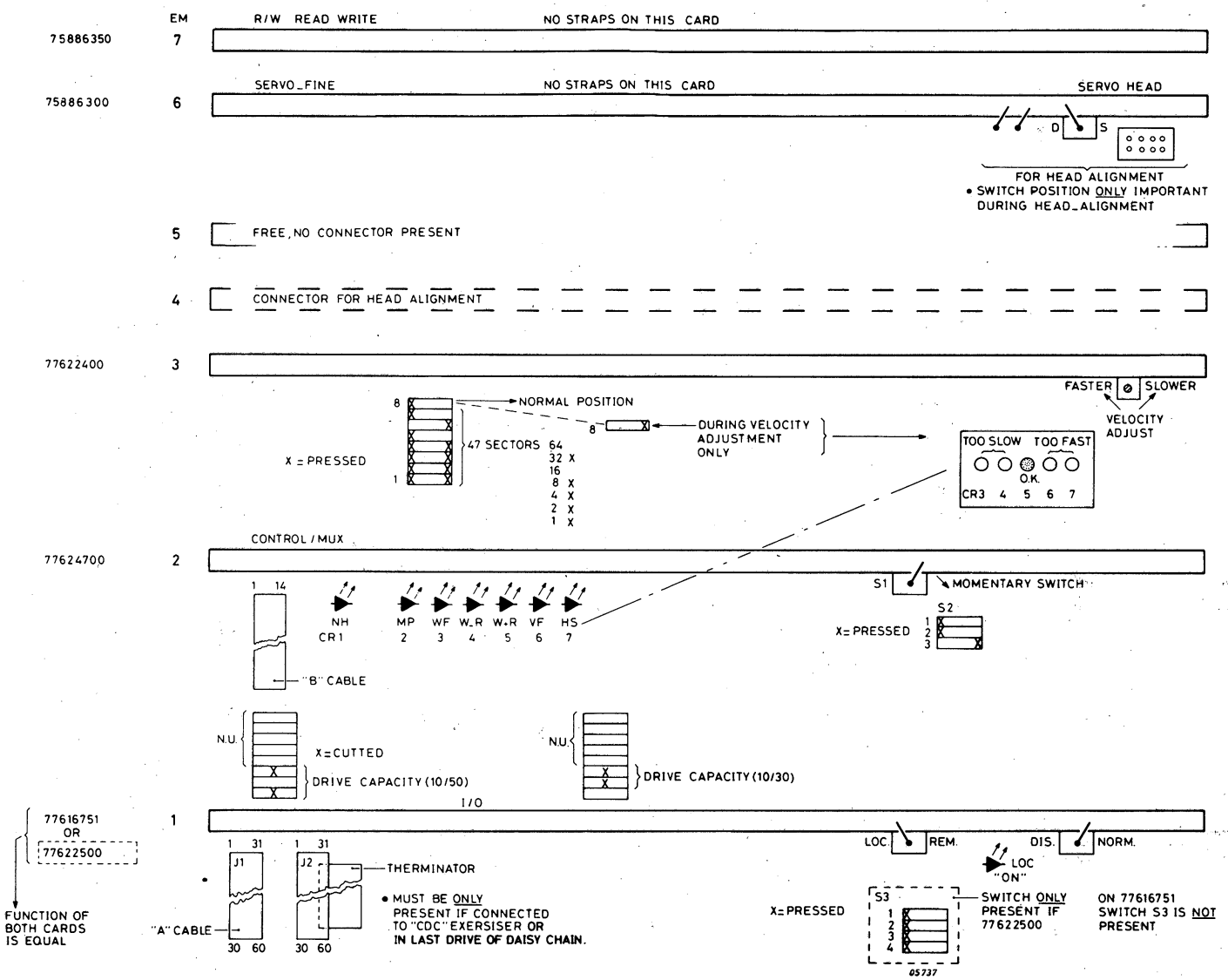


Figure 2.3.18 SWITCH SETTING CMD PCB'S

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3.1 RA12F- RACK P871/P874-300

3.1.1 IDENTIFICATIONS

P871-300/01 BASIC SYSTEM WITH 11 FREE SLOTS:

Part numbers P871-300:

5111 010 04060	IPL ROM 4064
5111 100 52250	Identification Strip P871
5111 199 53250	Card PSU 8105R (5322 218 80092)
5111 199 53980	Mounting Kit
5111 199 54160	Support PUC
5111 199 54290	Power Distribution Assembly (RA12F)
5111 199 54570	Kit 120V/7A
5111 199 55000	Rack RA12F
5111 199 56840	Card PSU 8124 (5322 218 80036)
5111 199 59390	Card CP1BF

P874-300/01 BASIC SYSTEM WITH 9 FREE SLOTS:

Part numbers P874-300:

5111 010 04060	IPL ROM 4064
5111 100 52220	Identification Strip P874-300
5111 199 53250	Card PSU 8105R (5322 218 80092)
5111 199 53980	Mounting Kit
5111 199 53990	Adapt Kit 115V 7A
5111 199 54160	Support PUC
5111 199 54290	Power Distribution Assembly (RA12F)
5111 199 55000	Rack RA12F
5111 199 56840	Card PSU 8124 (5322 218 80036)
5111 199 60060	Backpanel P857E-B
5111 199 61980	Card C7E1-B
5111 199 61990	Card C7E2-B
5111 199 62000	Card MIOP-B

P851-050/01 CABLE SUPPORT

5111 199 71690	Cable Support 1U, with Front Panel

P843-015/01 KIT WITH 10 PUC I SETS

5111 199 52460	Kit 10 PUC I

P843-016/01 KIT WITH 5 PUC II SETS

5111 199 52450	Kit 5 PUC II

P843-200/01 VENTILATION UNIT

5111 199 61260	Ventilation Unit Logic Rack

3.1.2 GENERAL DESCRIPTION

The RA12F rack is a 19" rack that comprises:

- Two Power Supply modules
- Mains Distribution Assembly
- Twelve slot back-panel (UPL-Bus)
- Operator Key Switch

On option the RA12F rack can be extended with:

- A 4U Ventilation Unit (P843-200)
- A 1U Cable Support (P851-050)

Remark: On the RA12F Rack-System can be connected up to 2 Winchester Disc Racks. The necessary voltages are distributed to the first Winchester Disc Rack for the optional Floppy disc Drive and/or the optional Streamer Tape Drive.
The remote power control is also distributed, in parallel, to the first and second disc rack.

3.1.3 MECHANICAL DATA

The RA12F has the following dimensions:

- Height: 266mm (6U)
- Depth : 283mm
- Width : 483mm (19")

3.1.4 POWER SUPPLY RA12F

3.1.4.1 MAINS CONNECTION

The RA12F is powered through a mains cord with:

- Upper range: 200-240V
- Lower range: 100-127V

The optional ventilation unit P843-200 must be adapted for the correct mains voltage range (see RAL22F rack).
As standard a "110V adaption" Kit is delivered with every rack (Fuse and Label).
The mains input is fused by a 3.2A (220V), or a 7A (110V) fuse on the mains filter assy.

3.1.4.2 PERFORMANCE DATA

VENTILATION CAPACITY (Ventilation unit is optional)

Extraction for 12 cards and power supply: 450W
Inter card air flow speed : 1m/sec.
Air flow temperature increase : 5°C
(at card rack level)

POWER SUPPLY RATING

The power supply provides the following outputs to the Bus back panel:

Voltages	PSU 8105	PSU 8124	Remark
+ 5VL	30.0A	-	
+12VL	1.0A	-	LOGIC VOLTAGES
-12VL	0.5A	-	
+24VL	-	3.5A	
+ 5VM	-	3.0A	MEM. VOLTAGE

Table 3.1.1 LOGIC- AND MEMORY VOLTAGES RA12F

BATTERY BACK-UP

The Battery Back-up time (for a fully, charged battery) is about 1 hour for 1 WMD, 256Kb memory.
A fully discharged battery takes 48 hours to be charged again.

3.1.4.3 TESTING THE BATTERY

The battery voltage can be measured on the cable connected to J3 of the 8124 PSU:

Pin 3 = 0V
Pin 1 = 12V (without mains connected)
Pin 1 = 35V (with mains connected)

To measure the charge discharge current, the battery must be connected to the STBY card via an AMP-meter.

3.1.5 PHYSICAL DESCRIPTION RA12F

The RA12F rack is mounted in a 19" cabinet as shown below.
The cable support, fan-unit and front-panels are to be ordered separately.

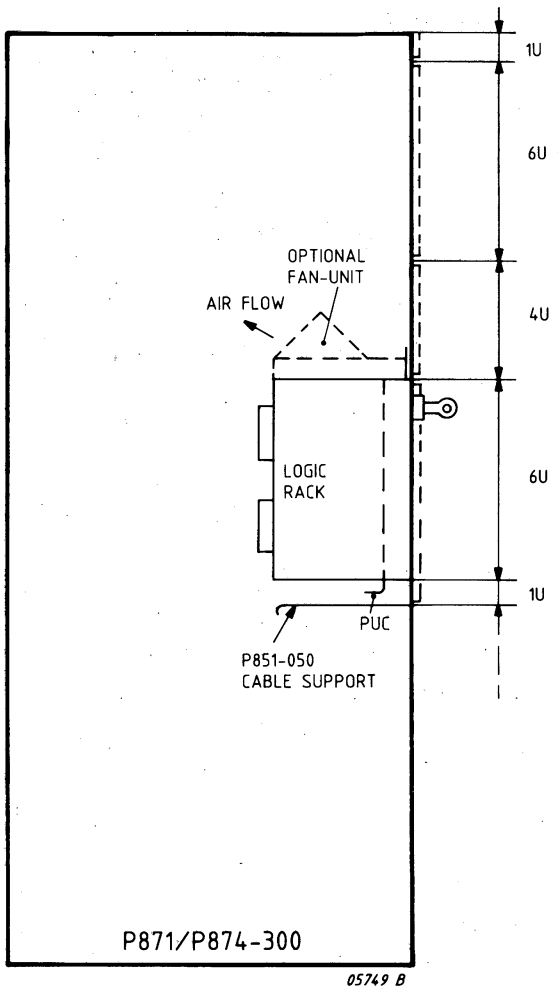


Figure 3.1.1 PHYSICAL CONFIGURATION RA12F IN 19" CABINET

For the details about the ventilation assembly and PUC refer to the description of rack RAL22F.

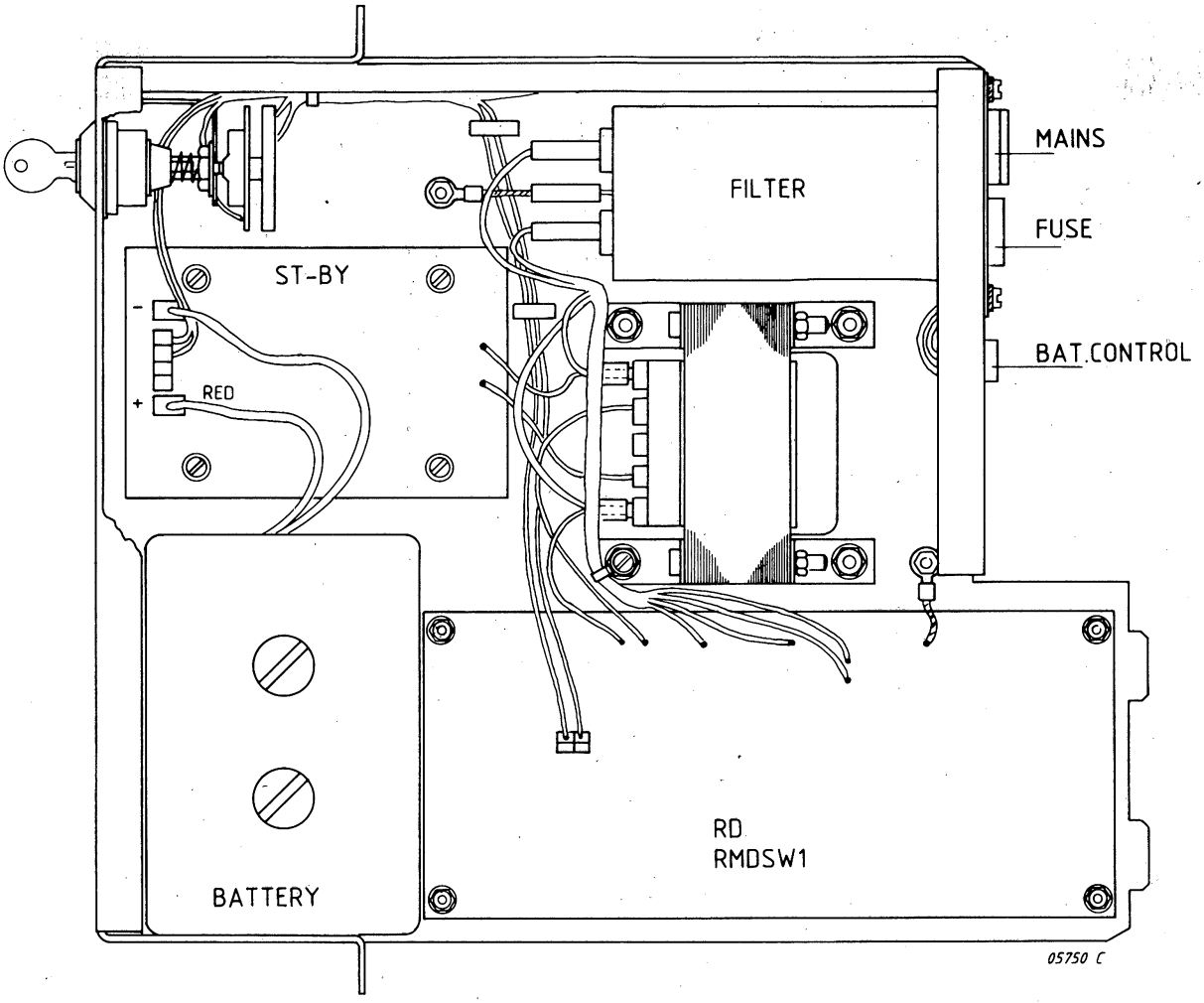


Figure 3.1.2 POWER DISTRIBUTION ASSEMBLY RA12F (5111 199 54290)

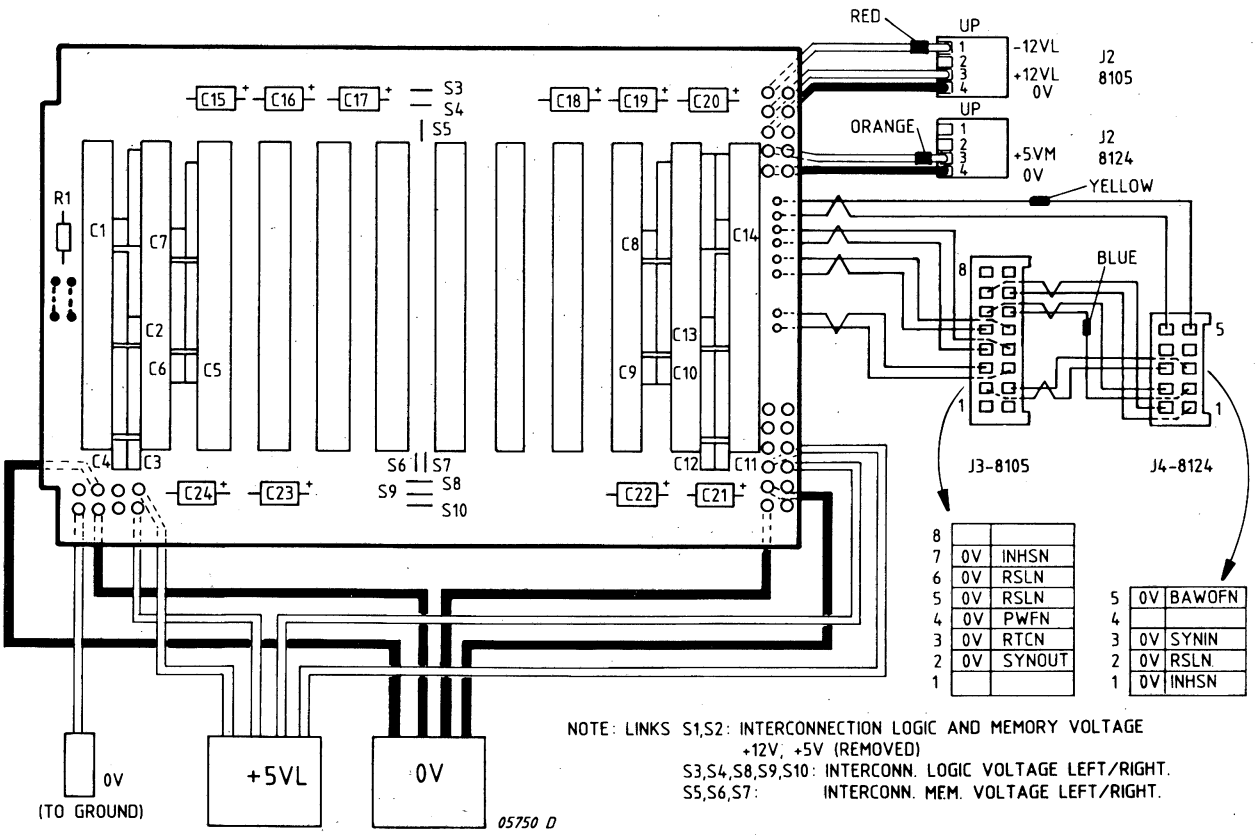


Figure 3.1.3 12-SLOT BACKPANEL RA12F (FRONT VIEW) (5111 199 54250)

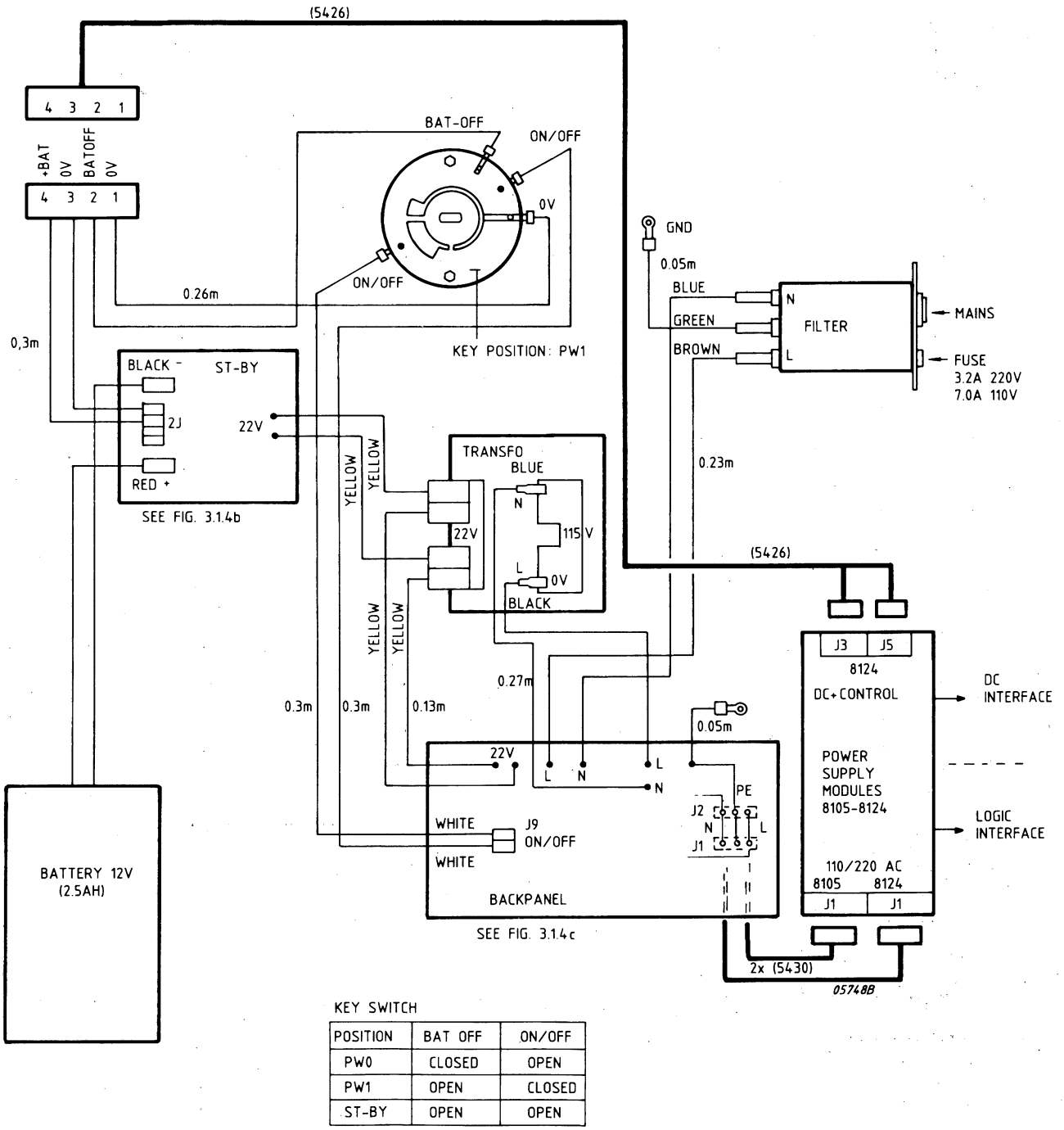
3.1.6 FUNCTIONAL DESCRIPTION RA12F

LOGIC SIGNALS (FROM 8105 AND 8124, SEE: INTERCONNECTIONS).

The power supply rack generates the following signals to the CPU and UPL Bus:

- Power failure protection (PWFN)
- Reset logic (RSLN)
- Battery was off (BAWOFN)
- Real time clock (RTCN)

For further details refer to RAL22F rack description and to the timing diagram.



KEY SWITCH

POSITION	BAT OFF	ON/OFF
PW0	CLOSED	OPEN
PW1	OPEN	CLOSED
ST-BY	OPEN	OPEN

Figure 3.1.4a POWER DISTRIBUTION RA12F

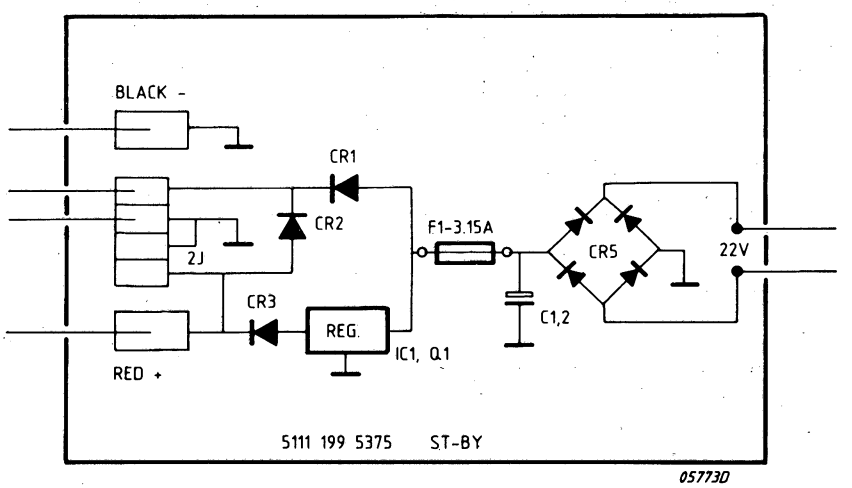


Figure 3.1.4b ST-BY CARD

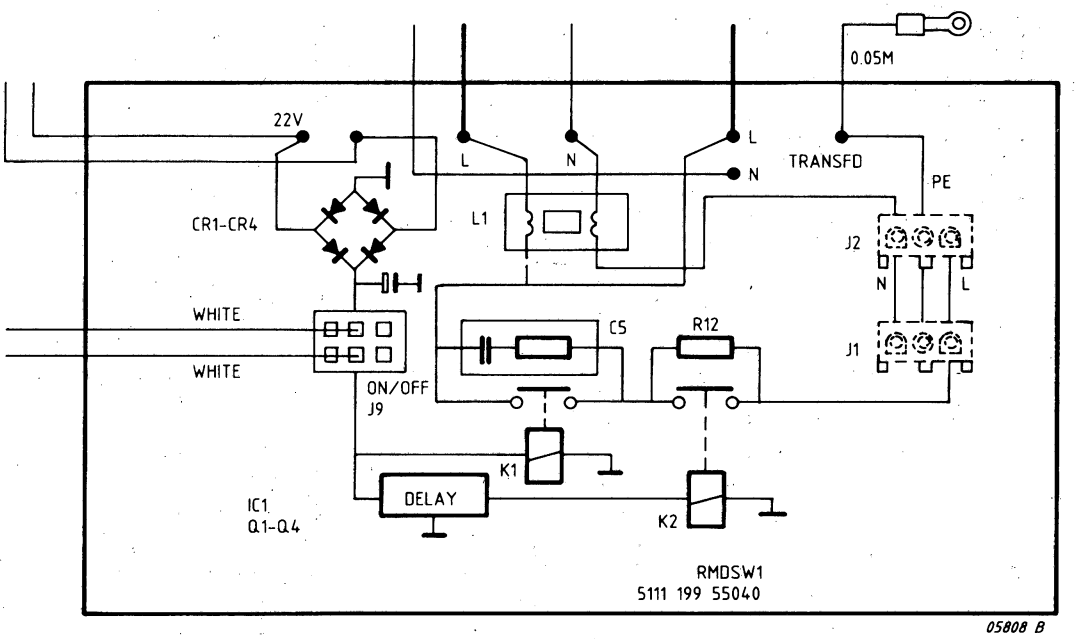


Figure 3.1.4c RMDSW1 CARD

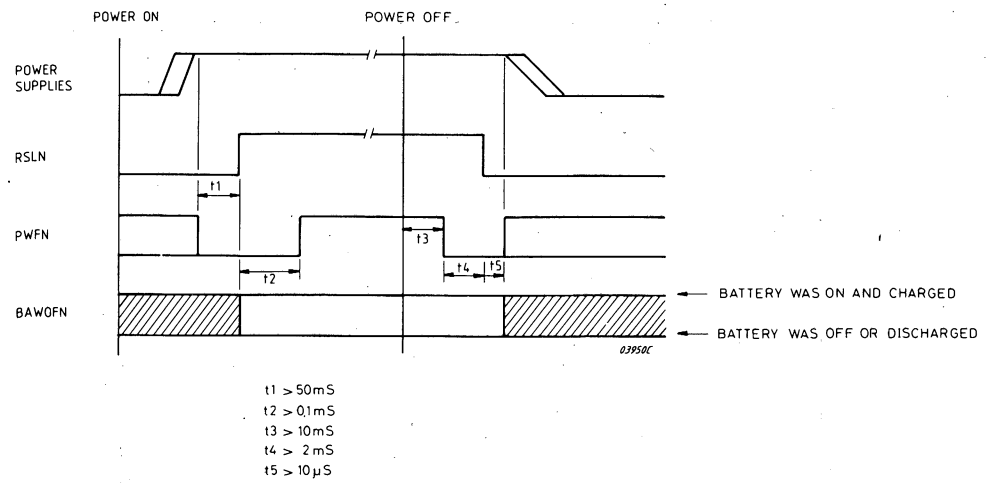


Figure 3.1.5 POWER SUPPLY LOGIC SIGNALS

3.1.7 OPERATOR KEY FUNCTIONS

The Operator's Key is used to control the combined switching of:

The mains supply to the Power Supply Rack;

The Logic voltages.

The Standby Memory Voltages;

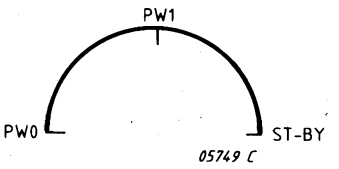


Figure 3.1.6 KEY SWITCH POSITIONS

The following table shows the combinations of the functions performed.

POSITION	MAINS SUPPLY	LOGIC VOLTAGES	MEMORY VOLTAGES	BATTERY CONNECTION	BATTERY FUNCTION
PW0	Switched OFF	OFF	OFF	DISCONNECTED	
PW1	Switched ON	ON	ON *	CONNECTED	CHARGE
ST BY	Switched ON	OFF	ON *	CONNECTED	CHARGE

* In case of mains failure the memory voltages are maintained by the battery.

Table 3.1.2 OPERATOR KEY FUNCTIONS

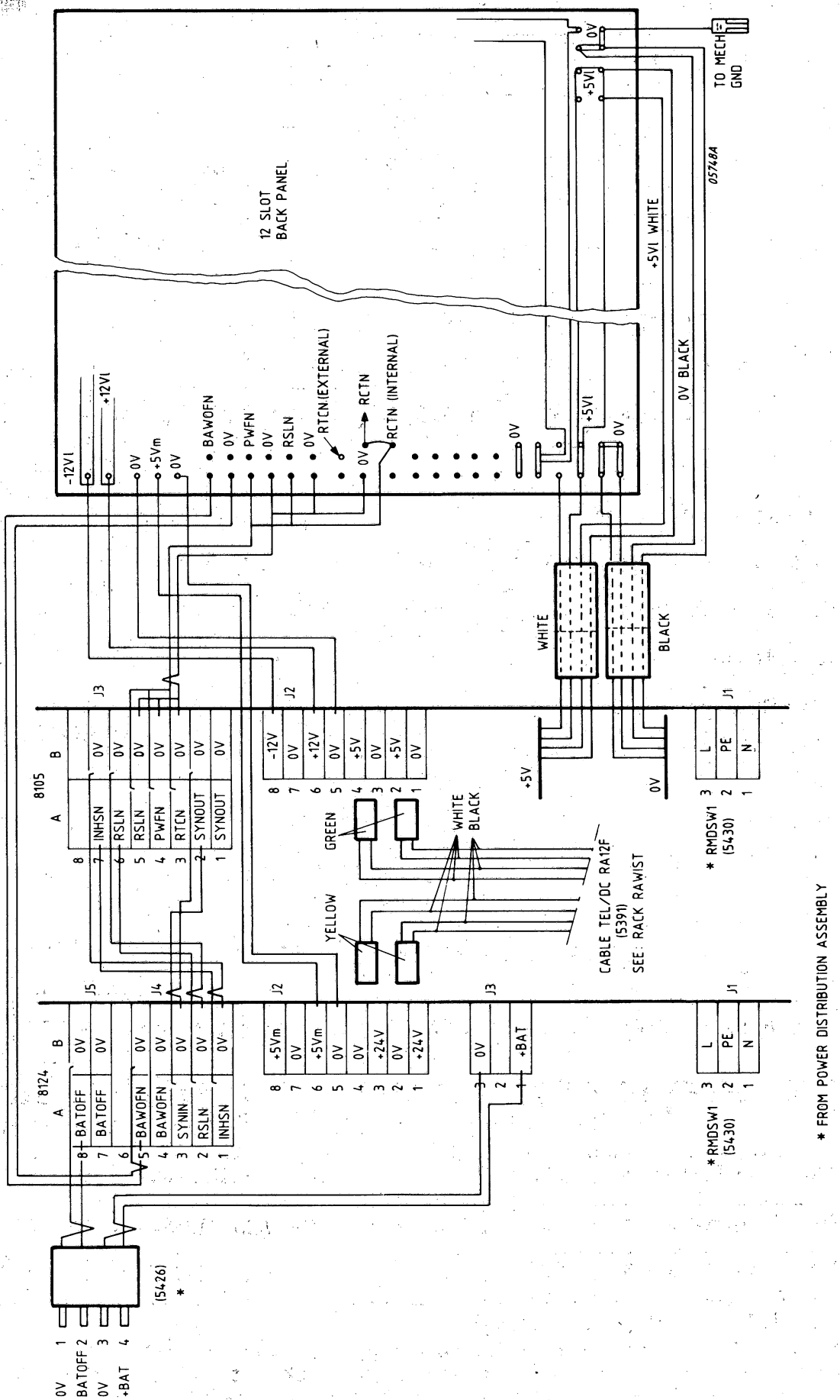


Figure 3.1.7 DC-WIRING AND LOGIC SIGNALS RA12F (REAR VIEW)

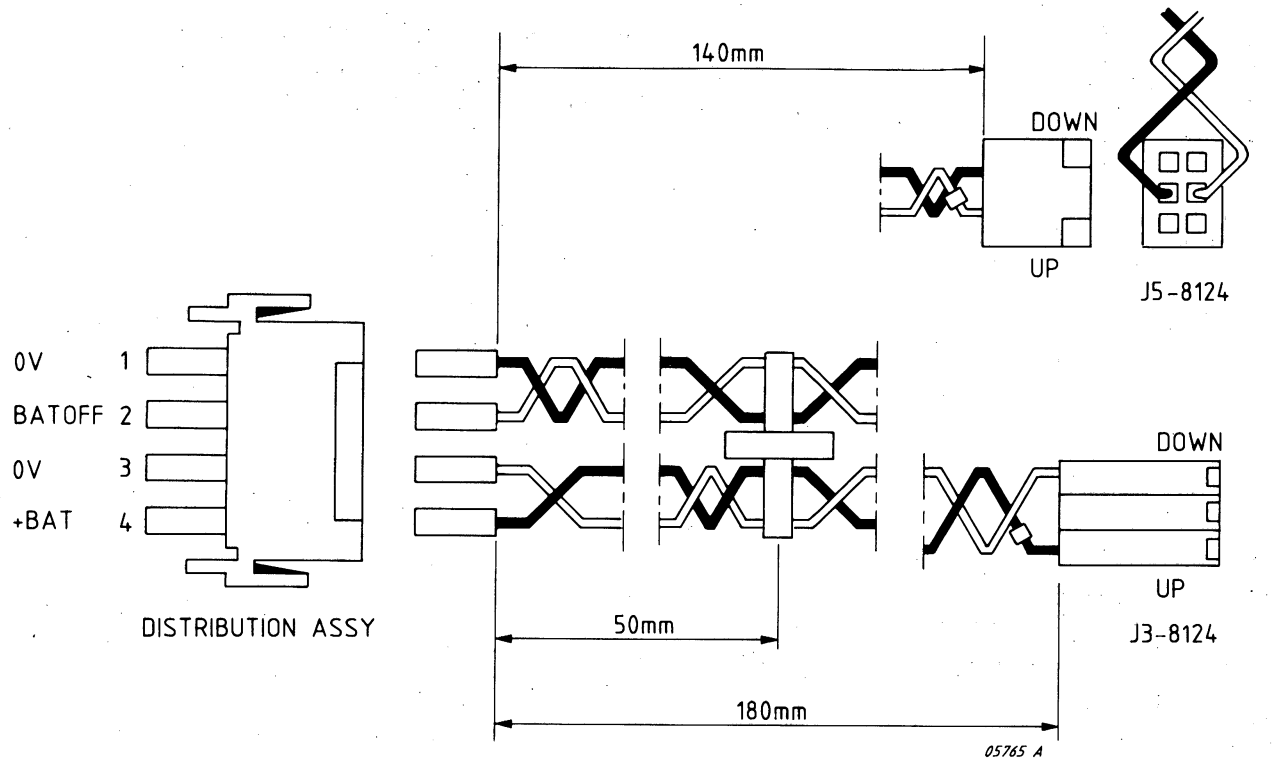


Figure 3.1.8a CABLE BATTERY SUPPLY AND CONTROL (5111 199 54260)

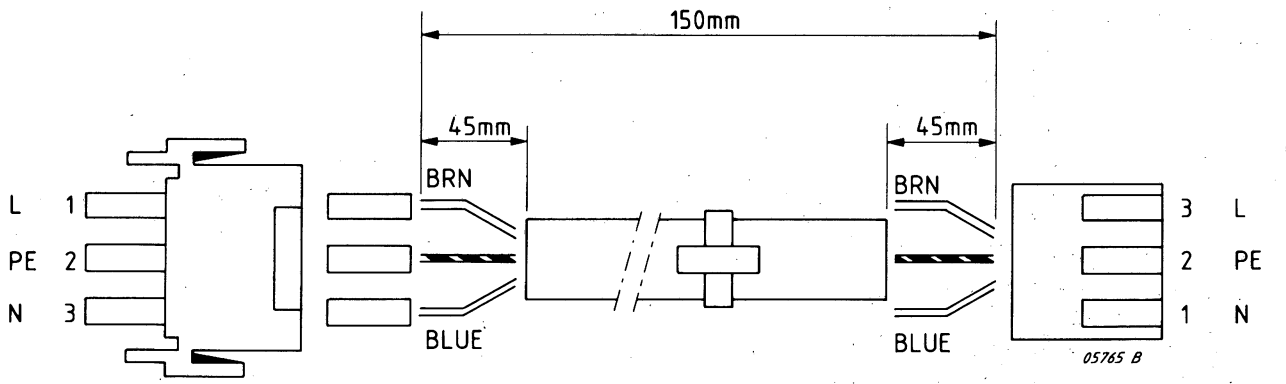


Figure 3.1.8b CABLE AC-220/110V FOR PSU'S 8105 AND 8124 (5111 199 54300)

3.1.10 VENTILATION UNIT LOGIC RACK RA12F

If a ventilation unit is used for the Logic Rack, it must be adapted to the correct mains voltage as shown in the description for rack RAL22F.

3.1.11 POWER SUPPLY UNITS RA12F

POWER SUPPLY UNITS: 8105 AND 8124

In case of short circuit, test without load and test of PSU's one by one is permitted. Note that primary switched power supplies need a minimum load of about 15% of their max. output current and therefore voltages may be slightly out of specification without load.

POWER ON.

If the key switch is in position 'ON' or 'STBY', the STBY pcb and +5VM regulator of PSU 8124 are active.
If the key switch is in position 'ON', the PSU's 8105 and 8124 are powered with AC from RMDSW1 pcb.

- Working on these primary switched power supplies is dangerous, if they are powered.
- Repair or adjustment is only allowed in workshop equipped with dedicated tools for these types of PSU's, such as isolation transformer, dynamic load, etc.
- It is not allowed to adjust PSU's in the field!

BATTERY (BBU - 5111 010 08471)

Manufacturer	: General Electric
type	: lead, 6 elements of 2V type D ref.: 47B025FD19001
voltage	: 12V nominal
capacity	: 2.5Ah 250mA in 10 hours discharge at 25 °C until 10.2V 1 hour for 512kb WMD memory in standby from a fully charged battery. Received batteries must have a minimum charge of 60%. After a full charge, batteries can be stored at 25°C up to 3 years after manufacturing date (mentioned on battery).
environment	: 0 - 50 degrees Celcius
humidity	: 80% max.
weight	: 1.2kg
size	: 106.9 x 73.2 x 68.6 mm
connection	: positive - red negative - black

Note: The battery is no standard spare part. It must be ordered from a local dealer.
During power failure, battery power is used to supply +5VM (PSM 8124) to the memory pcb's.
The battery is charged as long as the key-switch is in the activated position (PW1 or ST-BY) and MAINS is on.

BATTERY SUPPLY AND CONTROL LINES

+BAT/0V

The +BAT and 0V lines form together the DC input to the 8124.
From this DC input the +5VM is derived under control of the two BATOFF inputs.

BATOFF/BATOFF

The two BATOFF lines (Battery OFF) enable the +5VM supply from 8124 when the key-switch makes contact between the two lines.
When the key-switch contacts are open, the +5VM is disabled and the battery voltage (+BAT) disconnected from 8124.

INTERNAL LOGIC SIGNALS POWER SUPPLY RA12F

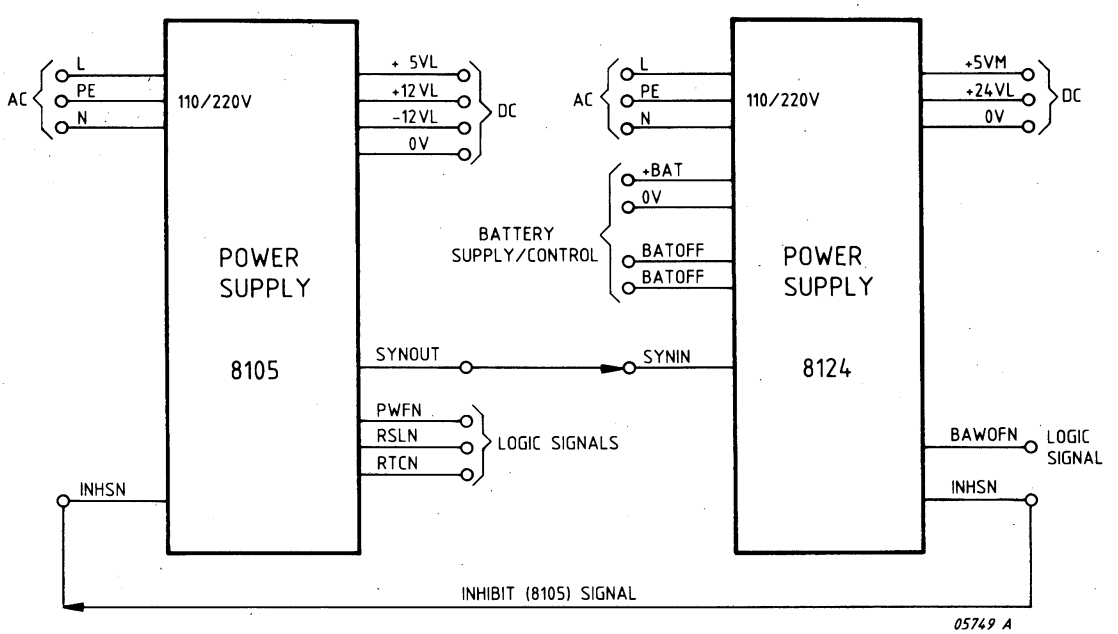


Figure 3.1.9 INTERFACES 8105 AND 8124 PSU'S

SEQUENCE INHIBIT OUTPUT SIGNAL (INHSN)

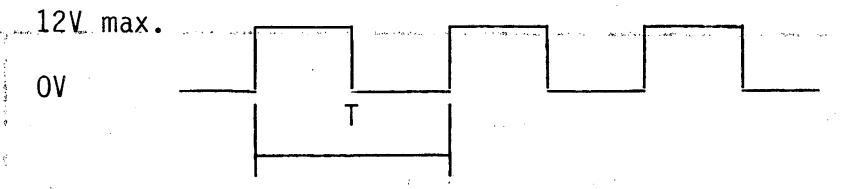
This signal is used by the PSU 8124 module in conjunction with a PSU 8105 module and must be connected to the INHSN input of the PSU 8105 module. When INHSN is at a low level, it indicates that the voltages of the PSU 8124 are not within their specified limits. This low level is used by the PSU 8105 module to keep the PWFN and RSLN signals at a low level.

SYNCHRONIZATION INPUT SIGNAL (SYNIN)

This signal is used by the PSU 8124 in conjunction with the PSU 8105 module. In this case, the PSU 8105 acts as a master by generating a synchronization signal for the switching oscillator of PSU 8124.

SYNCHRONIZATION OUTPUT SIGNAL (SYNOUT)

This signal is generated to synchronize the switching oscillator of other power supply modules when they are used in conjunction with the PSU 8105 moduel. The PSU 8105 acts as a master.



T = Master Oscillator period (about 25us)
Duty Cycle about 50%

Figure 3.1.10 SYNOUT/SYNIN

3.1.11.1 PSU 8105 (5322 218 80035)
PSU 8105R (5322 218 80092)

The Power Supply Unit 8105 provides the necessary DC voltage for ten double format EURO pcb's of a computer system. The DC voltage distribution will be provided by the back-panel bus of the rack.

MAINS INTERFACE

mains voltage	Lower range	99V to 132V rms
	Upper range	198V to 264V rms
main frequency	48 to 63Hz	

DC VOLTAGE

The PSU 8105 provides the following DC voltages:

+ 5VL max. current 30A
+12VL max. current 1A
-12VL max. current 0.5A

All DC-voltages are protected against overvoltage and overcurrent.

- static load variations	20 to 100% for +5VL 10 to 100% for +12VL and 112VL
- dynamic load variations	between +10% and -10%
- ambient temperature range	0 to 50 degrees Celcius

VENTILATION

When the PSU 8105 is operating within the specified operating range, no forced ventilation is needed.

Note: A new version of PSU 8105 is made (PSU 8105R). The difference is that the +5VL and 0V connectors are no longer attached via cables, but screwed on the printed circuit board. The old type 8105 however can still be used.

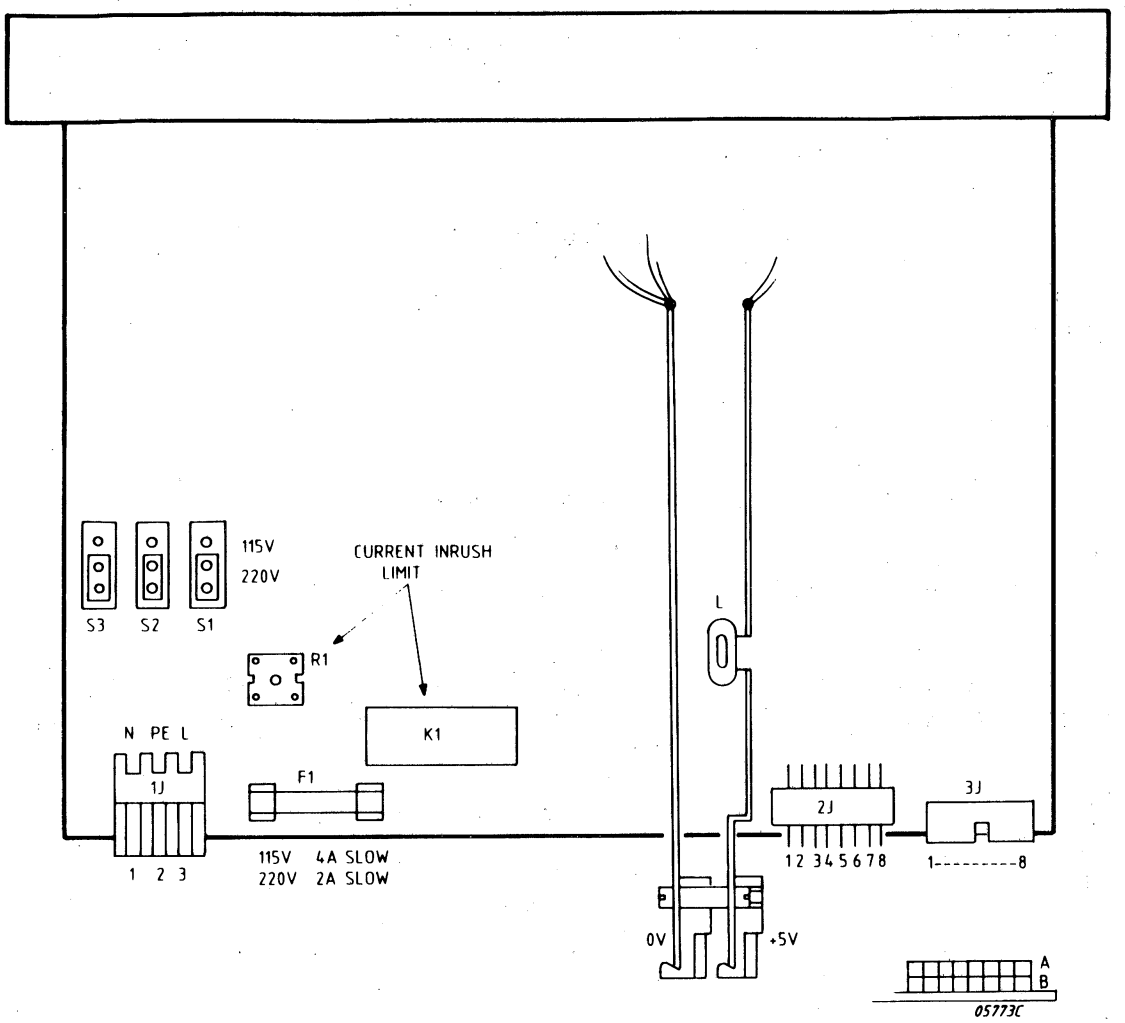


Figure 3.1.11 PSU 8105R

AC	
1J 1	N
2	PE
3	L

DC	
2J 2	+5VL
4	+5VL
6	+12VL
8	-12VL
1	0V
3	0V
5	0V
7	0V

LOGIC			
3J A1	SYN OUT	B1	0V
A2	SYN OUT	B2	0V
A3	RTCN	B3	0V
A4	PWFN	B4	0V
A5	RSLN	B5	0V
A6	RSLN	B6	0V
A7	INHSN	B7	0V

Table 3.1.3 INTERFACE PSU 8105

3.1.11.2 PSU 8124

The Power Supply Unit 8214 provides the necessary DC voltages for two WMD memory pcb's of a computer system and a +24V supply for FLOPPY and STREAMER. The DC voltage distribution for the memories is provided by the backpanel bus of the rack.

MAINS INTERFACE

mains voltage	Lower range	99V to 132V rms
	Upper range	198V to 264V rms
mains frequency	48 to 63Hz	

DC VOLTAGE INTERFACE

The PSU 8124 provides the following DC voltages:

+ 5VM max. current 3A
+24VL max. current 3.5A

The +5VM voltage is maintained by a Battery Backup system in case of power failure. Both DC output voltages are protected against overcurrent. Only +5VM is protected against overvoltage.

Note: +24VL : - no overvoltage protection -

- status load variations	20 to 100% for +5VM
	10 to 100% for +24VL
- dynamic load variations	between +10% and -10%
- ambient temperature range	0 to 50 degrees Celcius

VENTILATION

When the PSU 8124 is operating within the specified operating temperature range, no forced ventilation is needed.

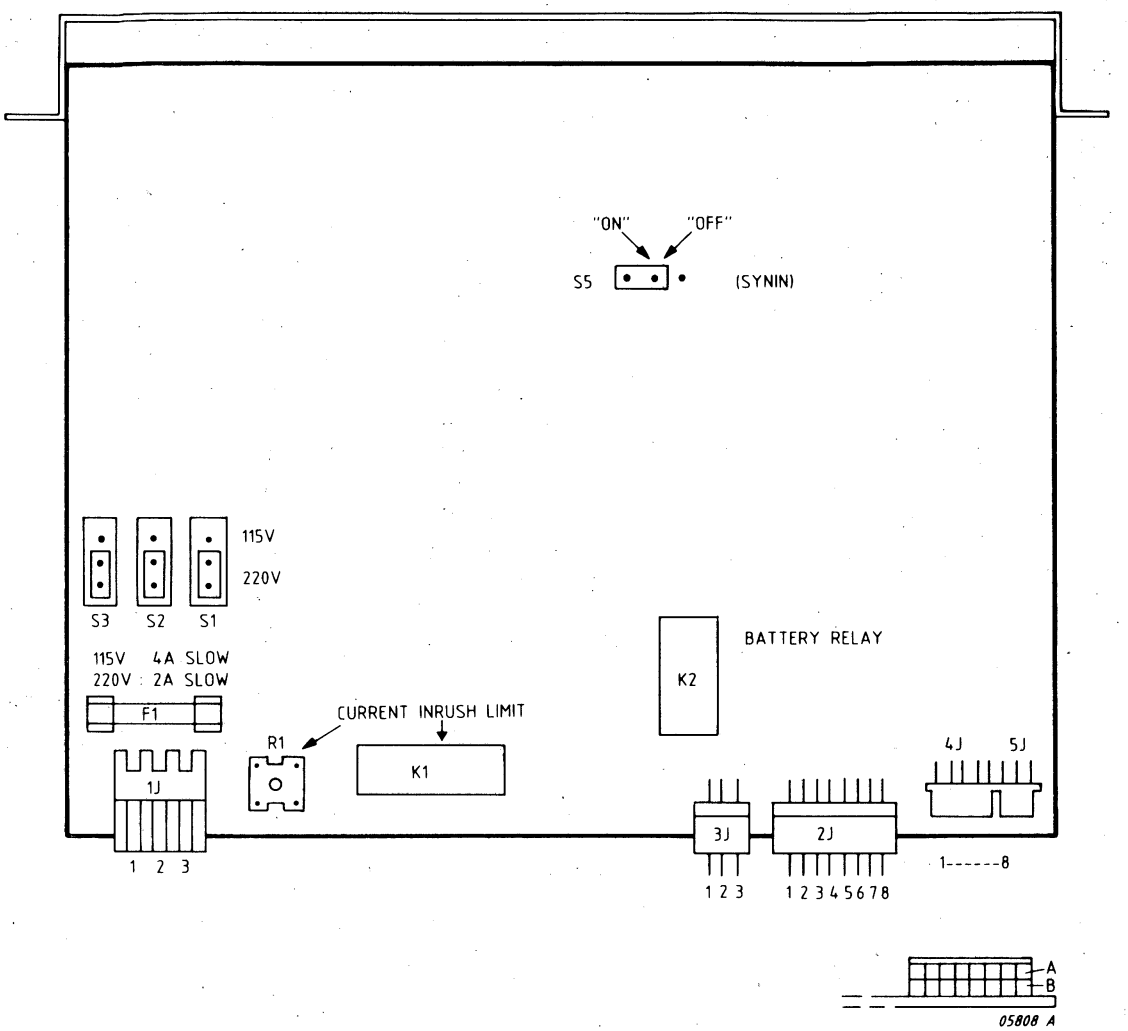


Figure 3.1.12 PSU 8124

AC		
1J	1	N
	2	PE
	3	L

BAT		
3J	1	+BAT
	2	(nc)
	3	0V

DC		
2J	1	+24VL
	2	0V
	3	+24VL
	4	0V
	5	0V
	6	+5VM
	7	0V
	8	+5VM

LOGIC				
4J	A1	INHSN	B1	0V
	A2	RSLN	B2	0V
	A3	SYNIN	B3	0V
	A4	BAWOFN	B4	0V
	A5	BAWOFN	B5	0V
5J	A6		B6	
	A7	BATOFF	B7	0V
	A8	BATOFF	B8	0V

Table 3.1.4 INTERFACE PSU 8124

3.1.11.3 STAND-BY BATTERY SUPPLY

The STBY pcb charges the battery in ST/BY and PW1 position of the key switch and supllies 30V or 12V DC to the PSU 8124.
If mains power fails, the battery instead supplies current to the +12VM regulator of the PSU 8124.

AC INTERFACE

input voltage	22V rms at 1.5A rms
frequency	48 to 63Hz

DC INTERFACE (VBAT)

30V DC ± 20% (unregulated), output VBAT = 12V if mains is "off".
30V DC, charge voltage +14.1V ± 0.1V at 25°C, input/output +BAT/,-BAT
charge current 250mA max.
charge voltage compensation for temperature change.

3.2 RAL22F-RACK P874-400/P876-400

3.2.1 IDENTIFICATIONS

P874-400/01 BASIC SYSTEM WITH 20 FREE SLOTS:

Part numbers P874-400:

5111 010 04060	IPL ROM 4064
5111 100 49060	Lock Bar Power Supply
5111 100 52210	Identification Strip P874-400
5111 199 54160	(2x) Support PUC
5111 199 54570	Kit 120V 7A
5111 199 54800	Mounting Kit RAL22F
5111 199 55120	Logic Rack RAL22F
5111 199 55140	Power Supply Rack RAL22F
5111 199 59080	Card PSU8B (5322 216 21287)
5111 199 60060	Backpanel P857E-B
5111 199 61260	Ventilation Unit Logic Rack
5111 199 61980	Card C7E1-B
5111 199 61990	Card C7E2-B
5111 199 62000	Card MIOP-B
5111 199 62220	Ventilation Unit RU22
5112 291 80780	Card PSU M1 (5322 214 40219)
5112 291 80880	Power Supply PSUB1E (5322 216 21434)

P851-050/01 CABLE SUPPORT

5111 199 71690	Cable Support 1U, with Front Panel

P876-400 BASIC SYSTEM WITH 18 FREE SLOTS

There are 2 different versions available:
- P876-400/01 : Cable-support FAN 220V (2U)
- P876-400/11 : Cable-support FAN 110V (2U)

Part numbers P876-400:

5111 010 04060	IPL ROM 4064
5111 100 49060	Lock Bar Power Supply
5111 100 52200	Identification Strip P876-400
5111 199 54160	Support PUC (2X)
5111 199 54800	Mounting Kit RAL22F
5111 199 54970	Cable Support Assembly (P876-400/11)
5111 199 55120	Logic Rack RAL22F
5111 199 55140	Power Supply Rack RAL22F
5111 199 55150	Cable Support Assembly (P876-400/01)
5111 199 56350	Interconnection Cable CP2B (5322 321 20884) (6X)
5111 199 57530	Card CIPF
5111 199 57570	Back Panel CP2B
5111 199 58050	Card CTPG
5111 199 58340	Card CIPC
5111 199 58350	Card CIPB
5111 199 58390	Card CIPA
5111 199 59080	Card PSU8B (5322 216 21287)
5111 199 61260	Ventilation Unit Logic Rack
5111 199 62220	Ventilation Unit RU22
5112 291 80780	Card PSU M1 (5322 214 40219)
5112 291 80880	Power Supply PSUB1E (5322 216 21434)

P843-400/01 BASIC POWER SUPPLY MODULE PSUB1E (5111 291 80880)

P843-402/01 MEMORY POWER SUPPLY MODULE PSUM1 (5111 291 80780)

3.2.2 GENERAL DESCRIPTION

The standard RAL22F is a set of 19 inch racks that comprises:

- A 23 slot Card Rack, with UPL backpanel.
- Operator's Key-Switch.
- A Power Supply Rack equipped with at least 1 PSUB1E module (for the Logic voltages) and 1 PSUM1 module (for the Memory voltages).
- A ventilation system with two 4U ventilator Units to be installed one above the Logic Card Rack and one above the Power Supply Rack.
- Additionally, the P876 Minicomputer System is installed always with an I/O cable and Ventilator Shelf for the cooling requirements of the 5 card CIP (CP2B).

On option the RAL22F can be supplied with:

- One extra PSUB1E slave and one extra PSUM1 added to the basic Power Supply Rack for large configurations.
- An I/O Cable Shelf P851-050 (1U) for the P874.

Remark: On the RAL22F Basic Rack System can be connected up to 2 Winchester Disc Racks (RAWIST).
The necessary voltages are distributed to the first winchester disc rack for the optional floppy disc drive and/or the optional streamer. The remote power control is also distributed, in parallel, to the first and second winchester disc racks.

3.2.3 MECHANICAL DATA

The weights and maximum dimensions of the basic mechanical units as shown below:

	LOGIC RACK	POWER SUPPLY RACK	VENTILATION UNITS
Height	266mm (6U)	266 mm (6U)	133 mm (3U)
Width	483 mm (19")	483 mm (19")	483 mm (19")
Length	300 mm (with cable shelf)	320 mm	300 mm
Weight	5 kilograms	9.3 kilograms	1.5 kilograms

Table 3.2.1 WEIGHT AND MAXIMUM DIMENSIONS RAL22F

3.2.4 POWER SUPPLY RAL22F

3.2.4.1 MAINS CONNECTION

The RAL22F is powered through a mains cord with:

- Upper range: 200 to 240V
- Lower range: 100 to 127V

The ranges are switchable on the 2 ventilation units and on the power modules. The fan on the 2U cable shelf, for the P876, can not be adjusted and must be the correct version for either 220V or 110V.

As standard a "110V adaption" kit (fuse and lable) is delivered with every rack.

The mains input is protected by a 6.25A (220V), or a 10A (120V) fuse.

3.2.4.2 PERFORMANCE DATA

VENTILATION CAPACITY

Extraction for 23 card slots : 450W.
Inter-card air flow speed : 1m/sec.
Air flow temperature increase : 5°C.
(at card rack level)

POWER SUPPLY RATING

The Power Supply Rack can supply different current values depending on the configuration, the examples of maximum permitted current are given in the table. If only 1 PSUB1E, it must be installed in the position marked on the PSU-back-panel with "MASTER".

LOGIC VOLTAGES (WITH VENTILATION UNIT OPERATING)

Voltages	PSU8B	1 PSUB1E	2 PSUB1E
+ 5VL	-	40.0A	70.0A
+12VL	-	3.5A	3.5A
-12VL	-	1.0A	1.0A
+24VL	-	3.5A	3.5A
- 5VL	3.5A	-	-
+24VE	1.6A	-	-

Note: The +24VL and +12VL can each supply a 6A instantaneous peak current.

Table 3.2.2 LOGIC VOLTAGES RAL22F

MEMORY VOLTAGES (WITH VENTILATION UNIT OPERATING)

VOLTAGES	1 PSUM1 MODULE	2 PSUM1 MODULES
+ 5VM	3.0A	6.0A
+12VM	1.5A	3.0A

Table 3.2.3 MEMORY VOLTAGES RAL22F

IN STAND-BY MODE (VENTILATION BY NATURAL CONVECTION ONLY)

VOLTAGES	1 PSUM1 MODULE	2 PSUM1 MODULES
+ 5VM	3.0A	6.0A
+12VM	1.0A	2.0A

Table 3.2.4 MEMORY VOLTAGES STAND-BY RAL22F

BATTERY BACK-UP

The Battery-Back-up time (for a fully charged battery) is about 3 hours for 1 WMD, 256Kb memory. A fully discharged battery takes 48 hours to be charged again.

3.2.4.2 TESTING THE BATTERY

A test socket is mounted on the rear of the battery support assembly for testing the battery without removing it from the power supply. To gain access to the socket, the rack must be swung down out of the cabinet.

For normal operation a plug is inserted with a link between pins 1 and 2. This connects the battery to the system via the contact of a small relay mounted on the battery support.

1. To totally isolate the battery in case of faults, simply remove the plug.
2. To measure the charge/discharge current connect an ammeter across pins 1 and 2 in place of the line (pin 1 positive wrt pin 2 when the battery is discharging).
3. To measure the battery voltage connect a voltmeter across pins 1 and 3 (pin 1 positive).
   After testing the battery always replace the link.

SLOT	CARD	+5VL	+24VL	+12VL	-12VL	+5VM	+12VM
1 2 3 4 5	CIPC CIPA CIPB CIPG CIPF	25.0		0.06	0.035		
6 7	FPPE2 FPPE1	4.45					
8	IOPZR	3.2					
9	IOPZR	3.2					
10 11 12 13 14 15	WMD1 WMD1 WMD1 WMD1 WMD1 WMD1	8.16				4.24	
16	WDC	4.35					
17	WJA	4.1					
18	SLCUZ	1.9		0.1	0.1		
19	AMA4Z	2.8		0.15	0.15		
20	F1MZA	1.8					
21	CRLPZ	1.0					
22	SCUZ	0.5		0.025	0.045		
23	FRCP	0.9		0.17	0.025		
TOTAL		61.36		0.505	0.355	4.24	
AVAILABLE		70	3.5	3.5	1.0	6.0	3.0

TABLE 3.2.5 EXAMPLE OF A P876-400 MINICOMPUTER SYSTEM WITH 6X WMD1 (1.5MB) MEMORIES, 2 PSUB1E AND PSUM

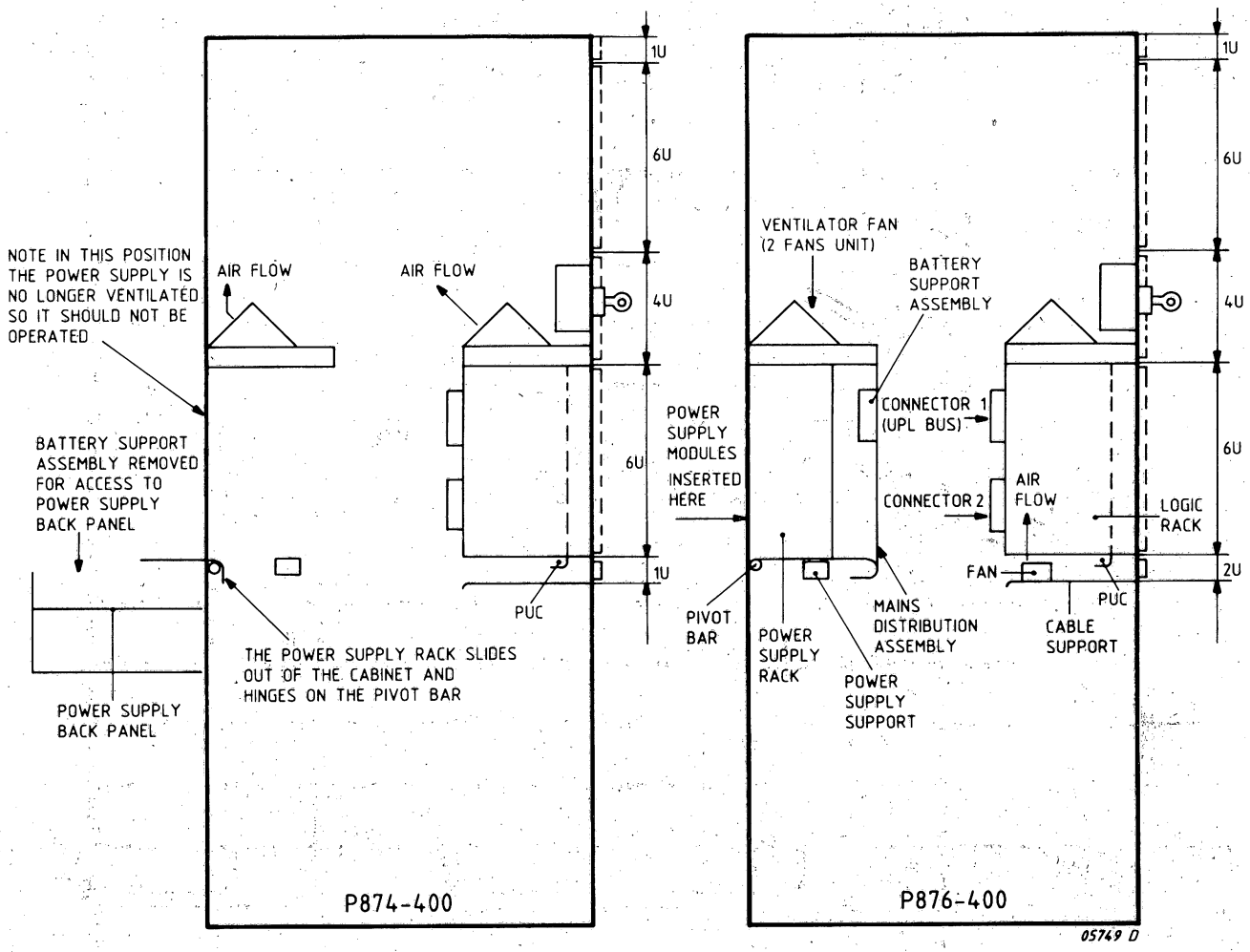


Figure 3.2.1 PHYSICAL CONFIGURATION RAL22F IN 19" CABINET

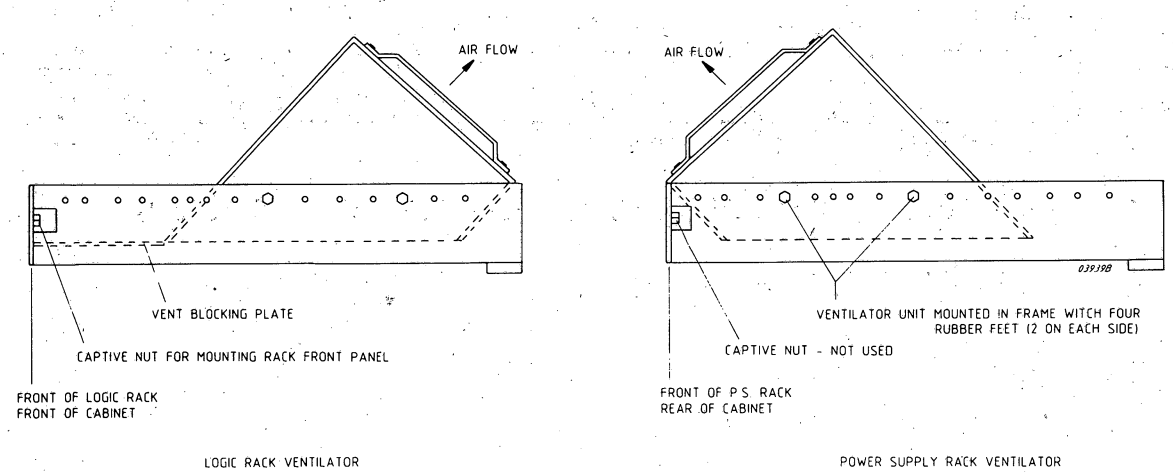


Figure 3.2.2 VENTILATION ASSEMBLIES

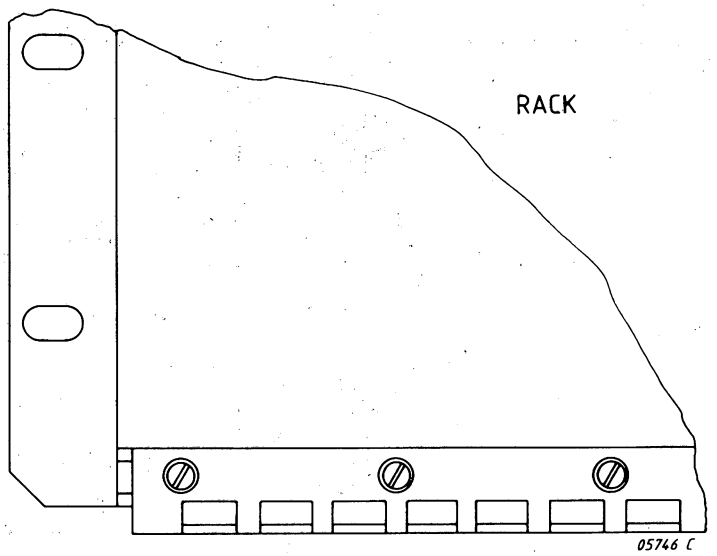


Figure 3.2.3 SUPPORT PUC (LOGIC RACK)

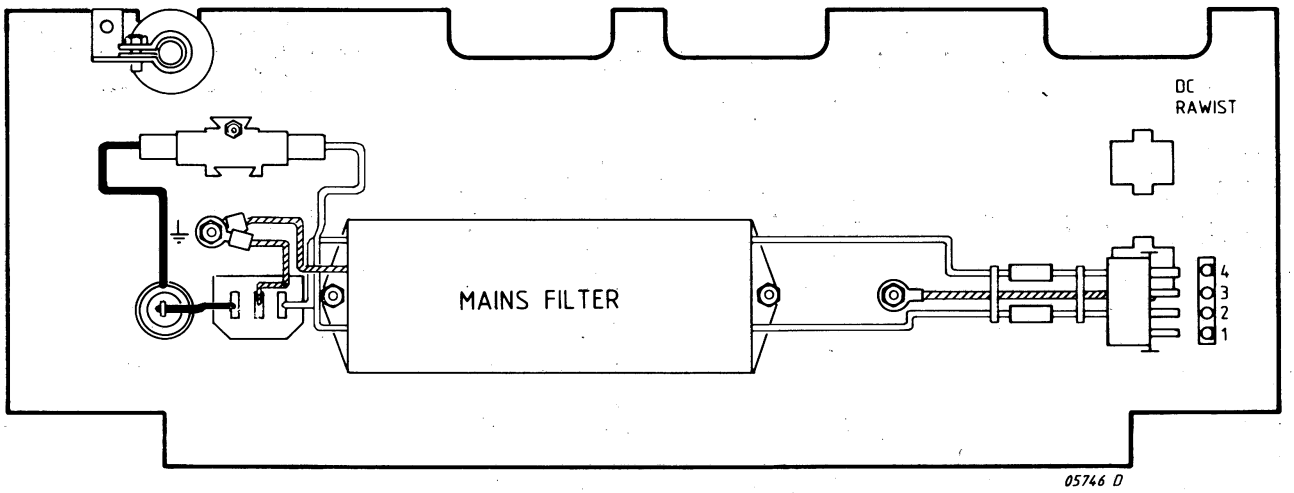


Figure 3.2.4 MAINS DISTRIBUTION ASSEMBLY (5111 199 54820)

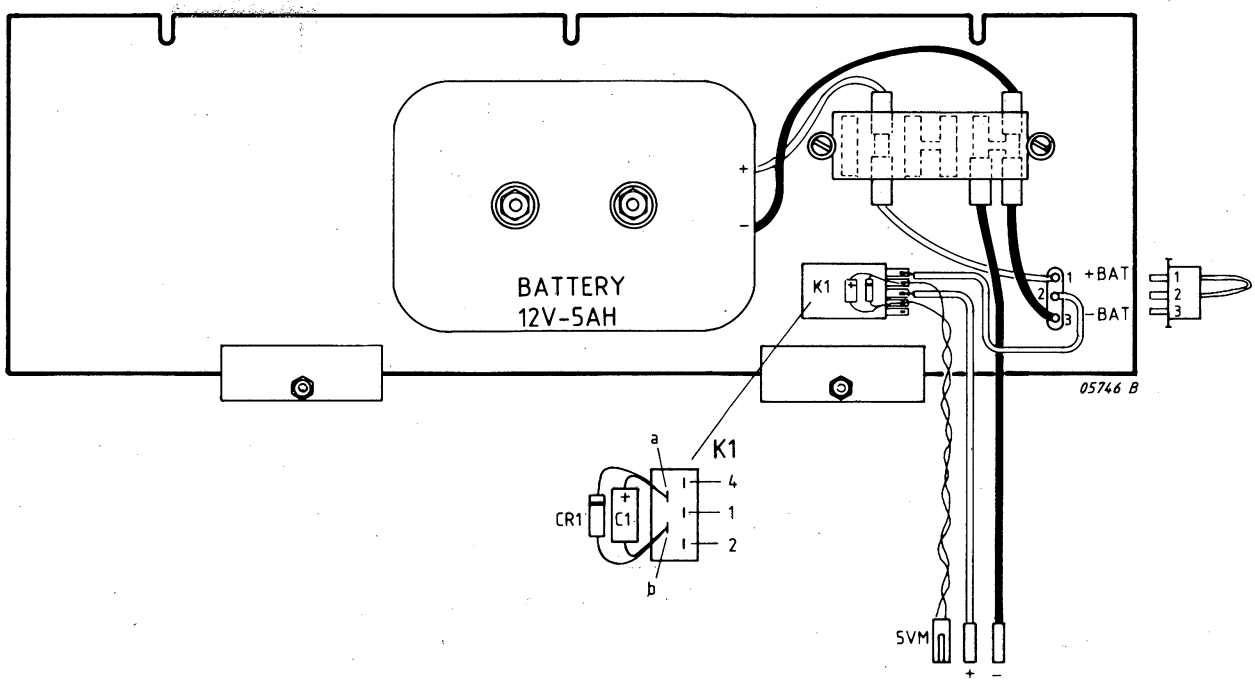


Figure 3.2.5 BATTERY SUPPORT ASSEMBLY (5111 199 59770)

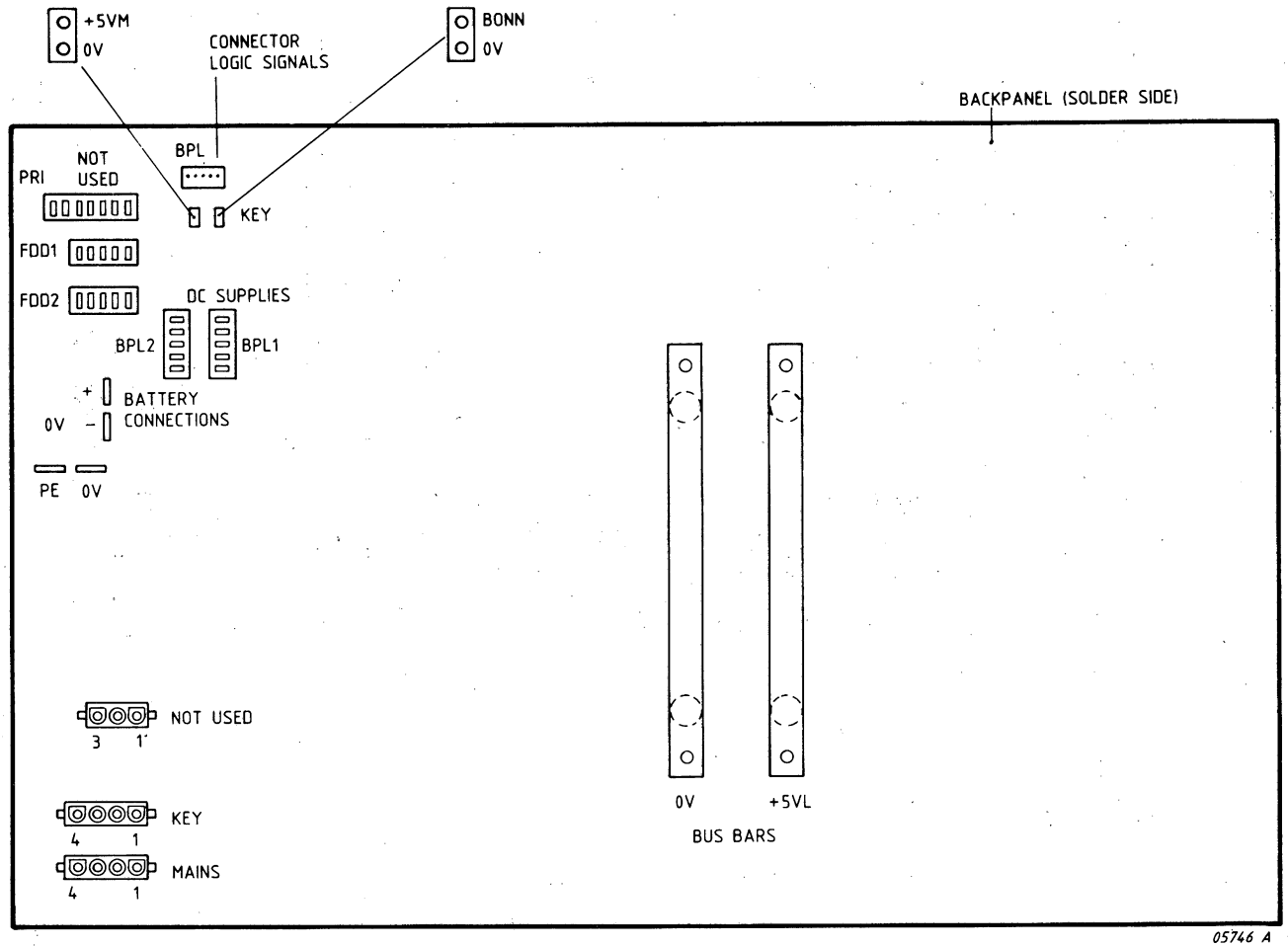


Figure 3.2.6 POWER SUPPLY BACK PANEL PBP86 (5111 199 55250)

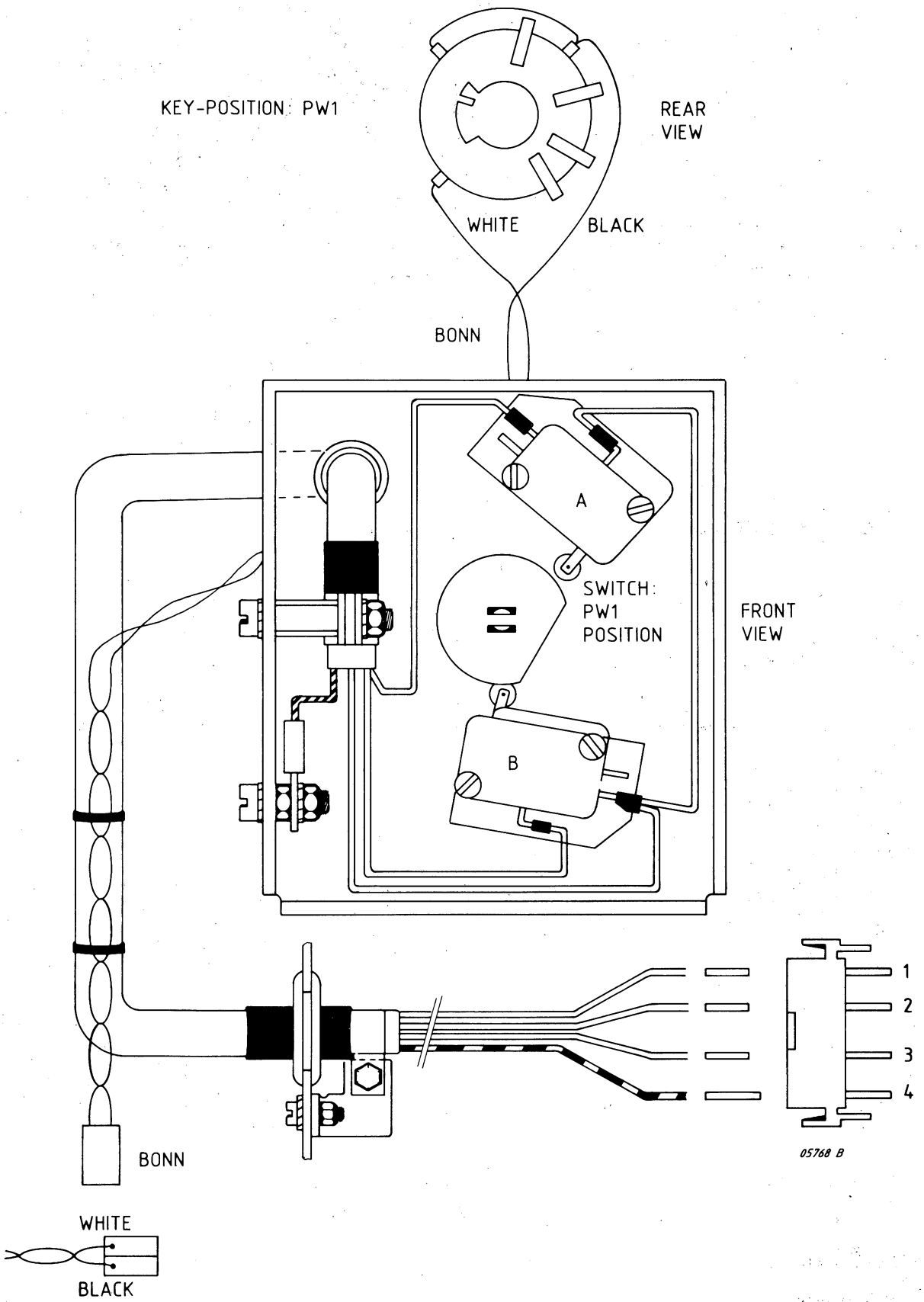
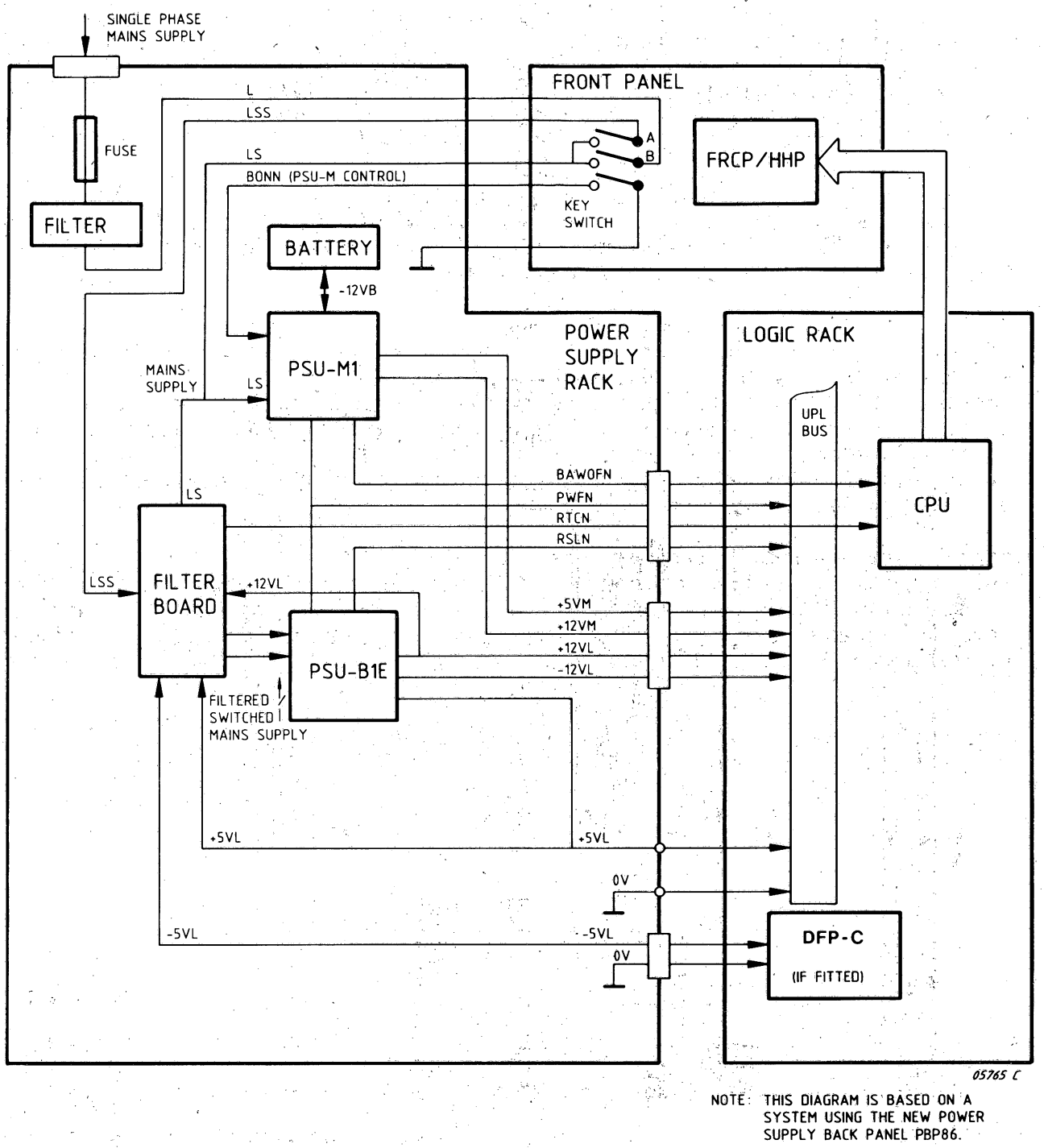


Figure 3.2.7 KEY ASSEMBLY (5111 199 55090)



NOTE: THIS DIAGRAM IS BASED ON A SYSTEM USING THE NEW POWER SUPPLY BACK PANEL PBP86.

Figure 3.2.8 RAL22F FUNCTIONS

LOGIC SIGNALS (FROM PSUB1E AND PSU M1)

The power supply rack generates the following signals to the CPU and UPL Bus:

- Power failure protection (PWFN)
- Reset logic (RSLN)
- Battery was off (BAWOFN)
- Real time clock (RTCN)

- Signal Line "PWFN" (Power Failure Not)
  During power-on the line should have the logical status "1", if all output voltages operate in their correct levels and if the RSLN is "1". When the mains voltage will drop below the -10% tolerance level, due to a failure, the PWFN line status will change to logical "Ø".

- Signal Line "RSLN" (Reset Line Not)
  The Reset Line should prevent misoperating of any logic circuits and mechanical devices during power-on and power-off.
  The Reset Line shall stay at a true ØV when the mains is not present.
  In case of a mains interrupt, indicated by the defined PWFN signal, the Reset Line will remain "1" at least 2 msec.
  After this time the Reset signal changes from "1" to "Ø" and all devices will be reset to avoid misoperating.

- Signal Line BAWOFN (Battery Was Off Not)
  This signal line reflects the status whether the back-up power voltage(s) was at its nominal level at the moment normal power was switched off, and has remained so ever since. The variable needs to be maintained and is used when system power is switched on (RSLN=1).

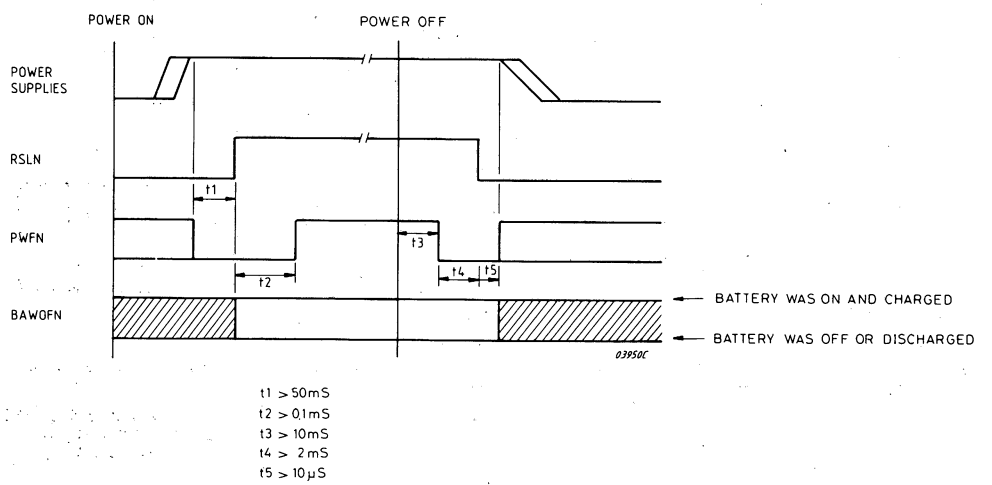
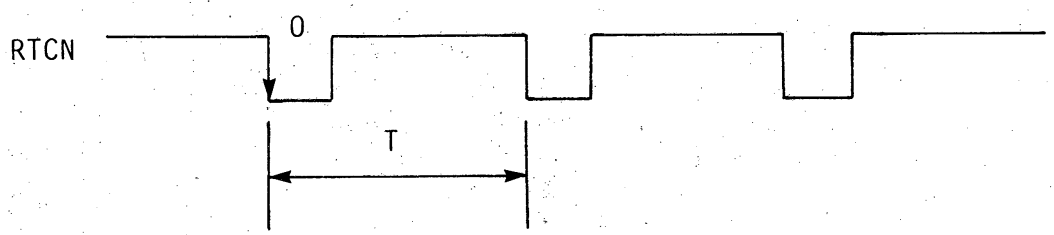


Figure 3.2.9a POWER SUPPLY LOGIC SIGNALS

- Signal Line RTCN (Real Time Clock Not)
  The RTCN signal is used by the system to provide the Real Time clock interrupt at each leading edge.



Where: 0 = 1us + 20% to -30%
T = mains period

Figure 3.2.9b POWER SUPPLY SIGNAL RTCN

3.2.7 OPERATOR KEY FUNCTIONS

The Operator's key is used to control the combined switching of:

- The mains supply to the Power Supply Rack
- The Logic voltages
- The Stand-by Memory Voltages

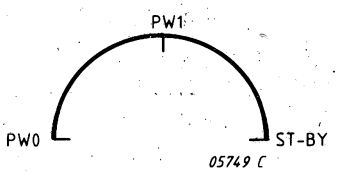


Figure 3.2.10 KEY SWITCH POSITIONS

The following table shows the combinations of the functions performed.

POSITION	MAINS SUPPLY	LOGIC VOLTAGES	MEMORY VOLTAGES	BATTERY CONNECTION	BATTERY FUNCTION
PWO	Switched OFF	OFF	OFF	DISCONNECTED	
PW1	Switched ON	ON	ON *	CONNECTED	CHARGE
STBY	Switched ON	OFF	ON *	CONNECTED	CHARGE

* In case of mains failure the memory voltages are maintained by the battery.

Table 3.2.6 OPERATOR KEY FUNCTIONS

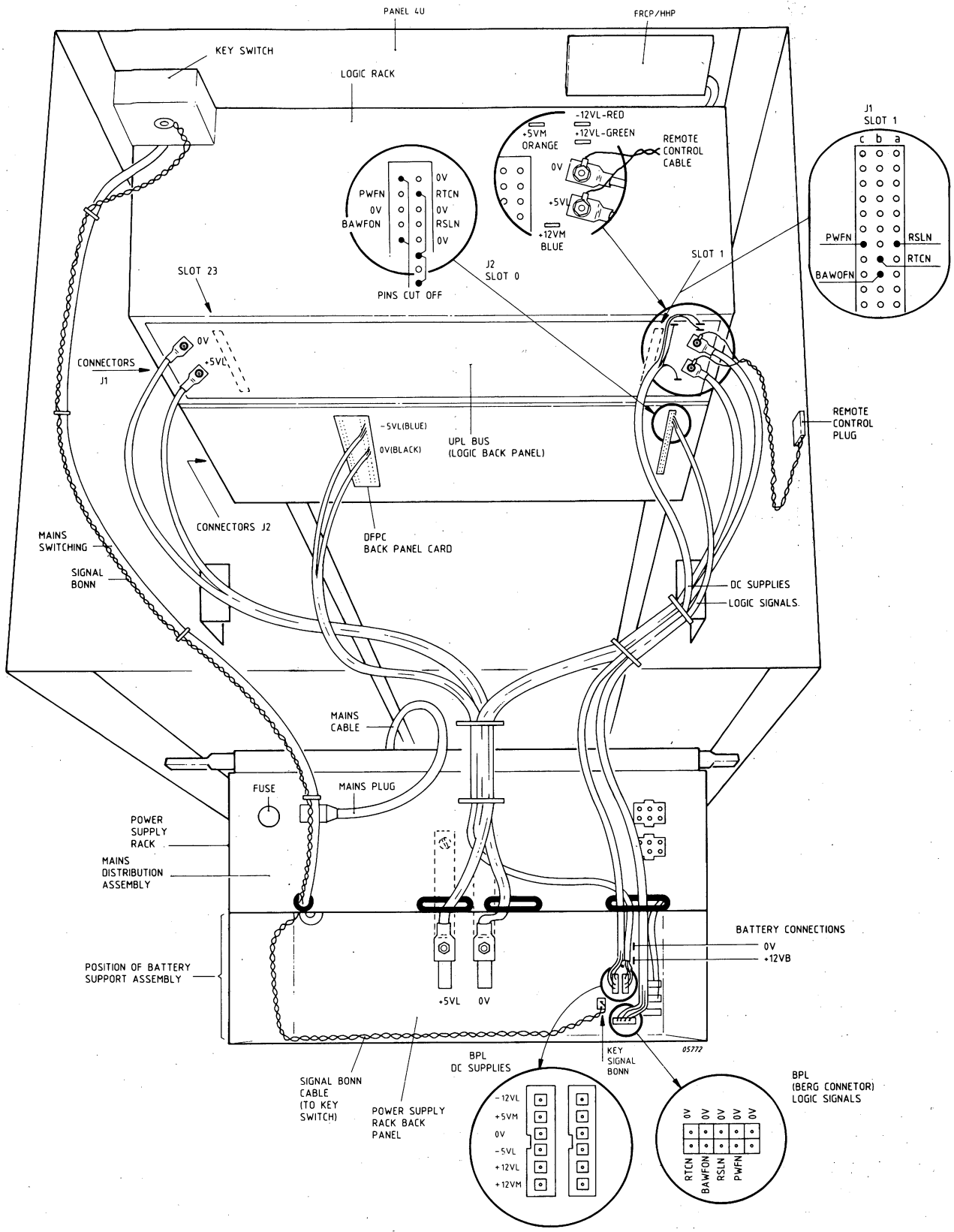


Figure 3.2.11 CABLING RAL22F

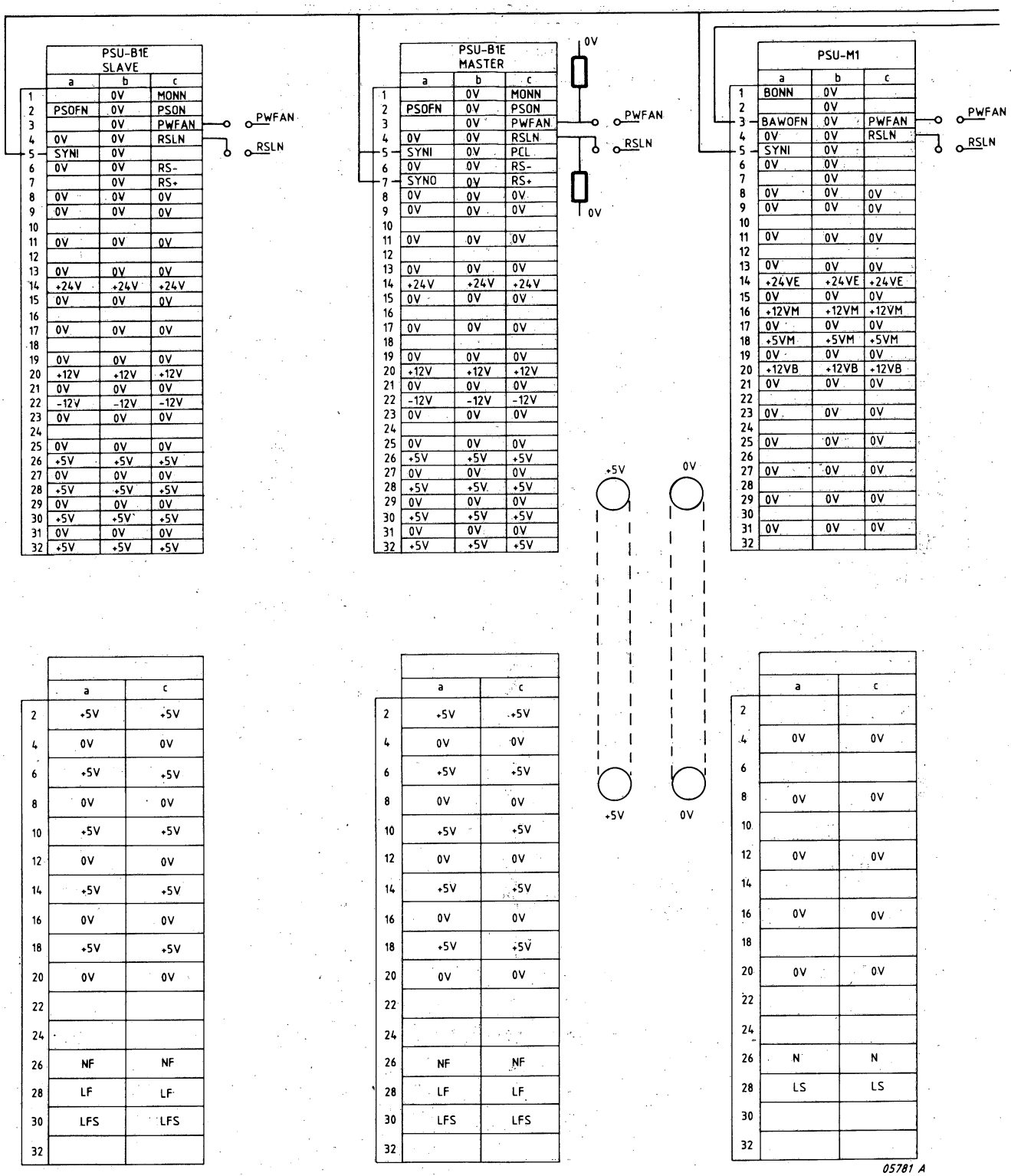


Figure 3.2.12 PSU BACK PANEL (LEFT HAND SIDE)

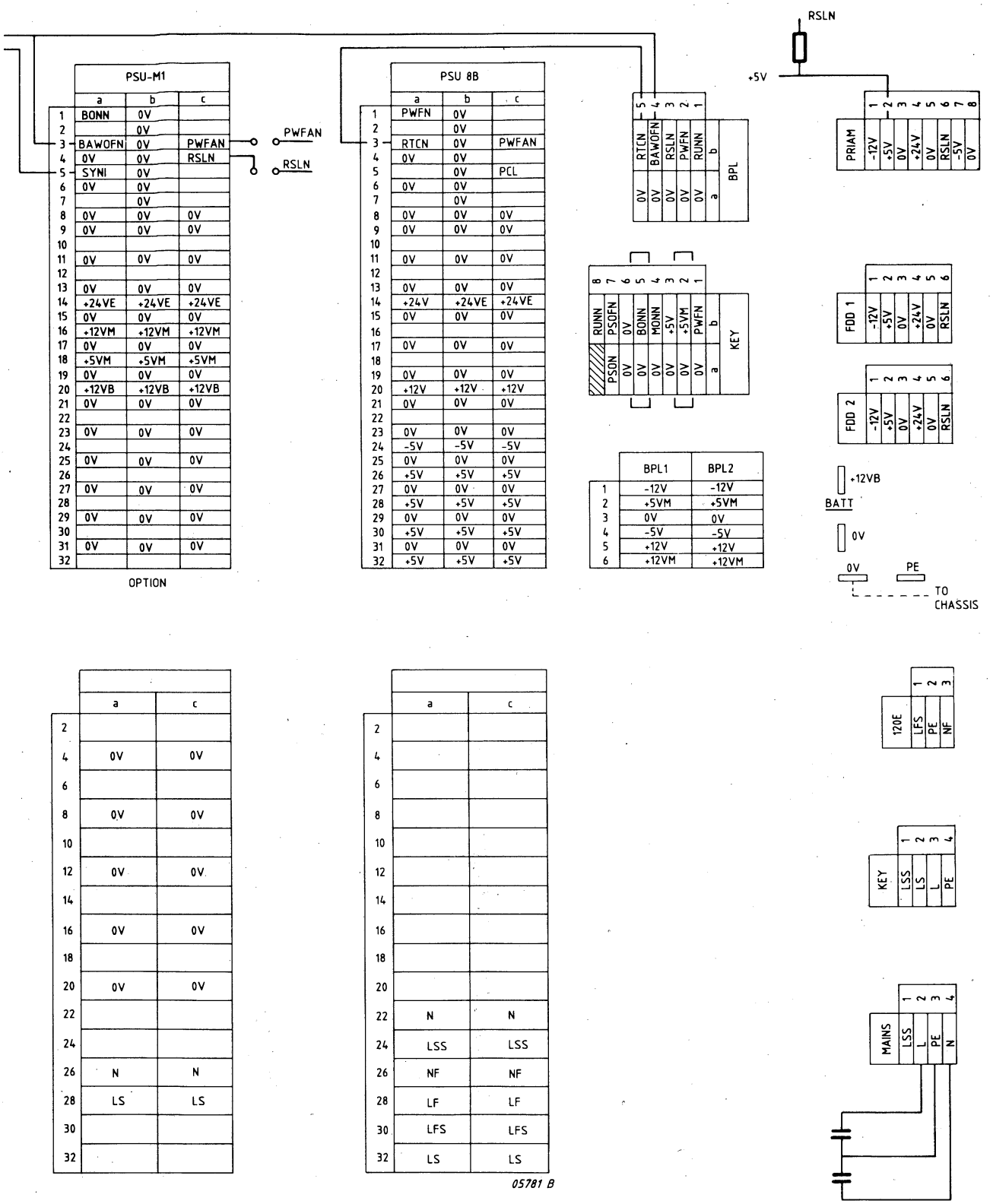


Figure 3.2.12 PSU BACK PANEL (RIGHT HAND SIDE) (CONT'D)

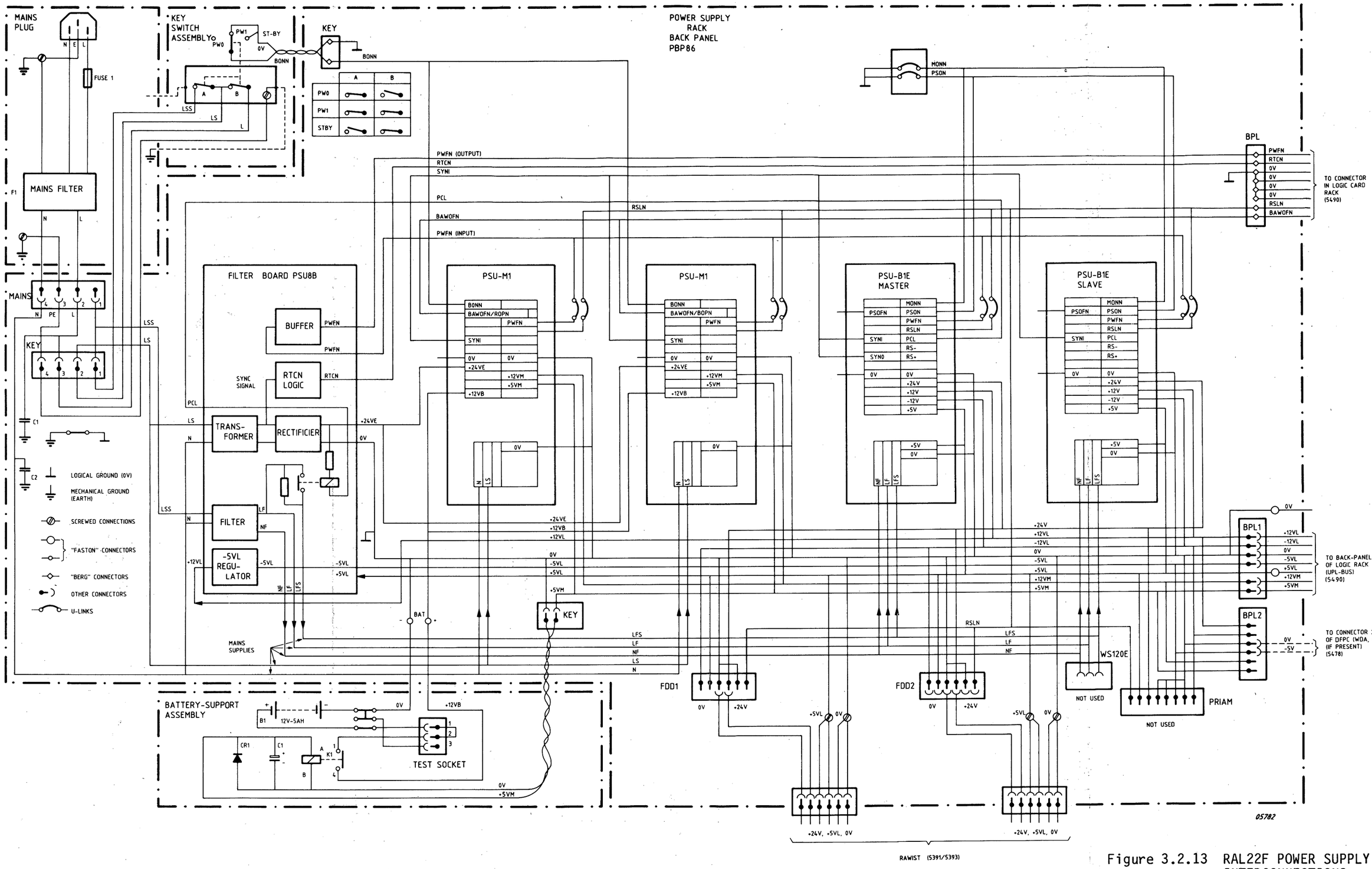
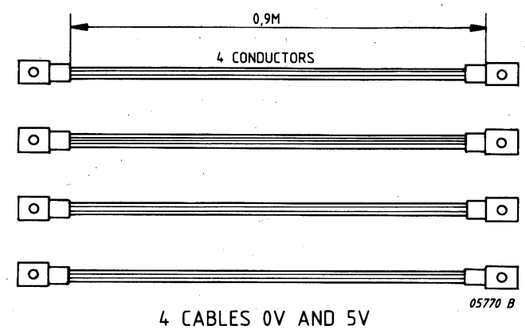
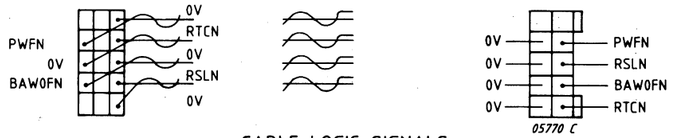


Figure 3.2.13 RAL22F POWER SUPPLY INTERCONNECTIONS

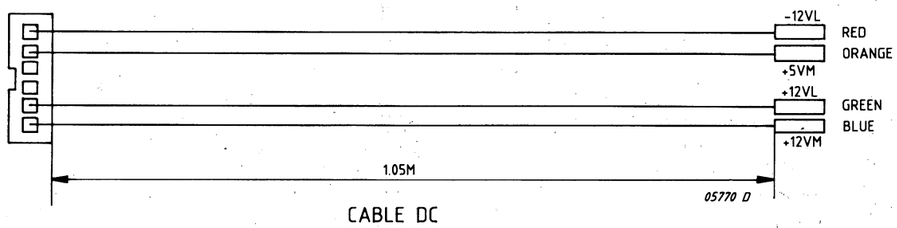
3.2.9 CABLES RAL22F



4 CABLES 0V AND 5V



CABLE LOGIC-SIGNALS



CABLE DC

Figure 3.2.14 CABLE ASSEMBLY RAL22F (5111 199 54900)

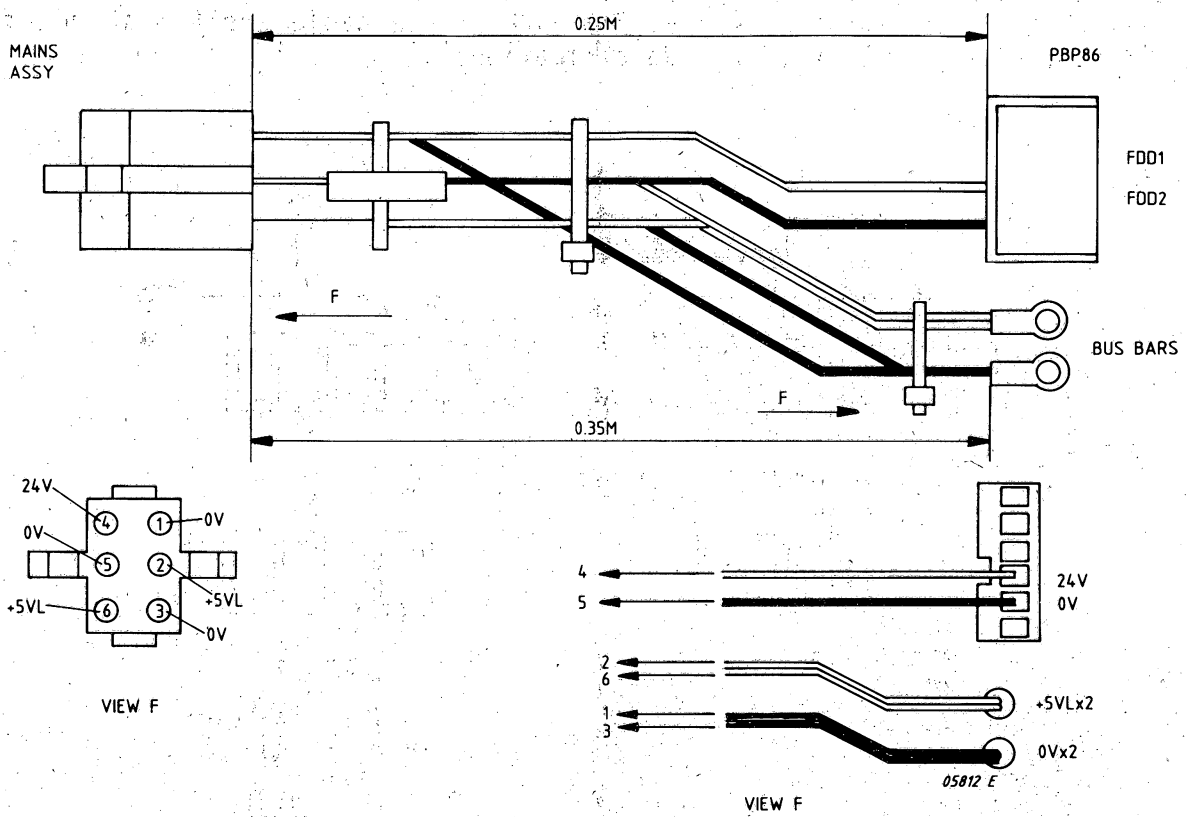


Figure 3.2.15 CABLE DC-FDD/STREAMER (5111 199 55130)

3.2.10 VENTILATION UNITS RAL22F

The 2 ventilation units of the RAL22F must be adapted to the correct mains voltage. (See: Mains Connection).

The 2U cable shelf which is used with P876 also is equipped with a FAN.
The FAN is necessary for cooling the 5 CP2B cards in co-operation with the ventilation unit of the logic rack. The FAN on the cable shelf must be of the correct type: 220V or 110V (See: Identifications).

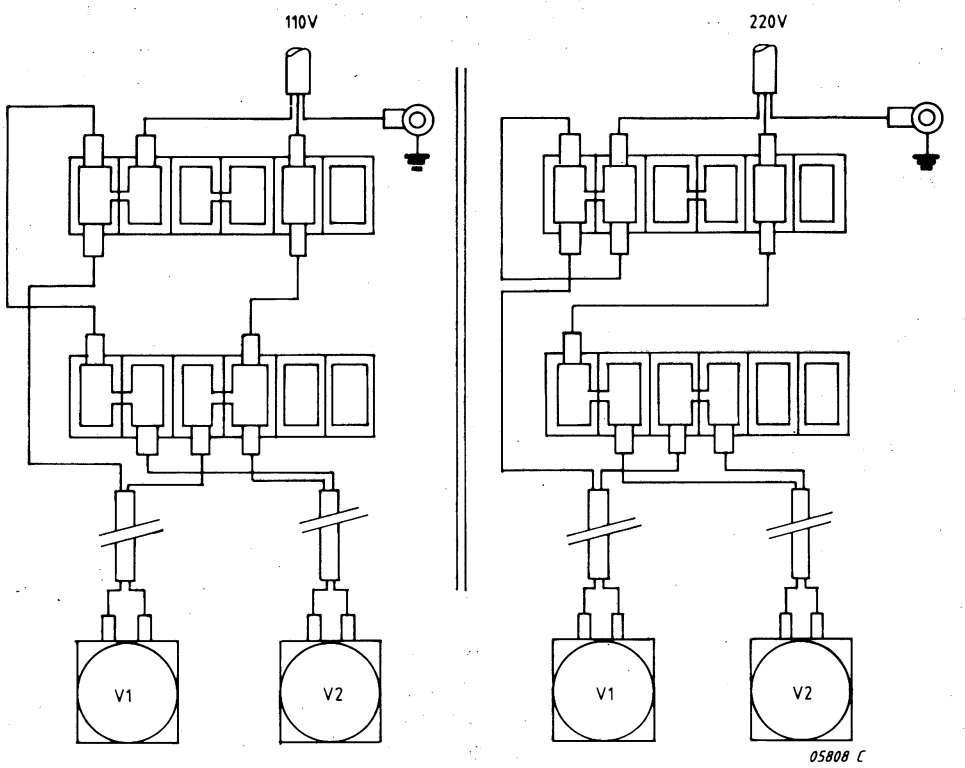


Figure 3.2.16 VENTILATION-UNITS VOLTAGE-ADAPTION

3.2.11 POWER SUPPLY UNITS RAL22F

The power supply is of modular design.
The power supply units operate with switching technique.

Note: Power Supply Units are independant, but:
In case of short circuit, test without load and test of PSU's one by one is not permitted. Note that primary switched power supplies need a minimum load of about 15% of their max. output current (PSU B1E and WS120E).

> WARNING:
> . Working on these primary switched power supplies is dangerous, if they are powered.
> . Repair or adjustment is only allowed in workshops equipped with dedicated tools for these types of PSU's such as isolation transformer, dynamic load, etc.
> . It is not allowed to adjust PSU's in the field

BASIC POWER SUPPLY (P843-400/01, PSUB1E)

Supporting flexible disc drives and Streamer Tape together with approximately 20 electronic boards. PSUB1E input is switchable, for high and low voltages (90-140 or 180-280V, 50 or 60Hz).

POWER SUPPLY UNIT FOR MEMORY (P843-402/01, PSU-M1)

This module supplies power to the memory even when the mains voltage to the basic power supply is switched off (stand-by or power failure).
PSUM1 input is switchable for high and low voltages (90-140 or 180-280V, 50 or 60Hz). However, this unit is also supplied with +24V from PSU8B. See also Technical Data PSU-M1.

FILTERBOARD (PSU8B)

The filterboard contains a mainsfilter through which the mains is passed to the power supply units B1E.
On the filterboard is also available a 24V supply used to supply the M1-module. PSU8B input is switchable for high and low voltages (99-132 or 198-264V, 48-63Hz).

The CPU is provided with power failure and restart signals from the power supply modules, as well as a Real Time clock timing signal, which are controlled via the filterboard.

BATTERY (BBU - 5111 010 06222)

- Standby for 256kb for a period of 3 hours from fully charged.
- After discharge, charging takes 48 hours.
- Capacity 5 Ah, 12V.

Power on/off

Note: The battery is no standard spare part. It must be ordered from a local dealer.
The battery is charged as long as the key-switch is in the activated position and MAINS is on. PSU-M1 is connected to supply +5VM (and +12VM).

POWER SUPPLY CONTROL LINES RAL22F

Signal Line "PSON" (Power Supply On Not)
The Power Supply System will start if MONN and PSON are both in logical "Ø".
Two U-links at the card side must be connected for this purpose.

Signal Line "PSOFN" (Power Supply Off Not)
The signal line directs the PSU to switch off the normal power. During power on (RSLN and PWFN = logical "1") the PSOFN-line is kept high (log. "1") by the system processing hardware (not connected in RAL22F).

Signal Line MONN (Master On Not)
This signal can be connected to the master-on/off switch (not present on P800) on the operator panel and should allow the mains power supply to be connected/ disconnected by means of a key switch. In the RAL22F this signal is grounded with an U-link. a "master-off" will completely disconnect all power except battery power, if available.

Signal Line "BONN" (Battery On Not)
This signal line is connected to a key switch at the operator panel. This switch allows the battery to be switched off, i.e. in case the system is left with mains power disconnected for a longer period of time (in order to avoid discharging).
The battery is disconnected if the BONN-line will have the logical status "1".

INTERNAL LOGIC SIGNALS RAL22F

PCL (Power Control Line)
This line controls the primary power distribution line on PSU8B, relay k1.

SYNO (Synchronization Out)
This signal is used for synchronization of switched mode power supply units in order to avoid undesired oscillations when several units (max. 6 units) are operating in parallel. The frequency is higher than 20 KHz. Only one SYNO line (master) of a basic unit should be connected to other Power Supply Units (slaves) by means of external wiring (PSU-B1E is the master).

SYNI (Synchronization In)
This input is synchronized by an external clock (reason: see definition of SYNO).

RS +; RS - (Remote Sensing +; Remote Sensing -)
When remote sensing is required the connection of the lines RS + and RS - should be made at the centre of loads.

3.2.11.1 PSU-B1E

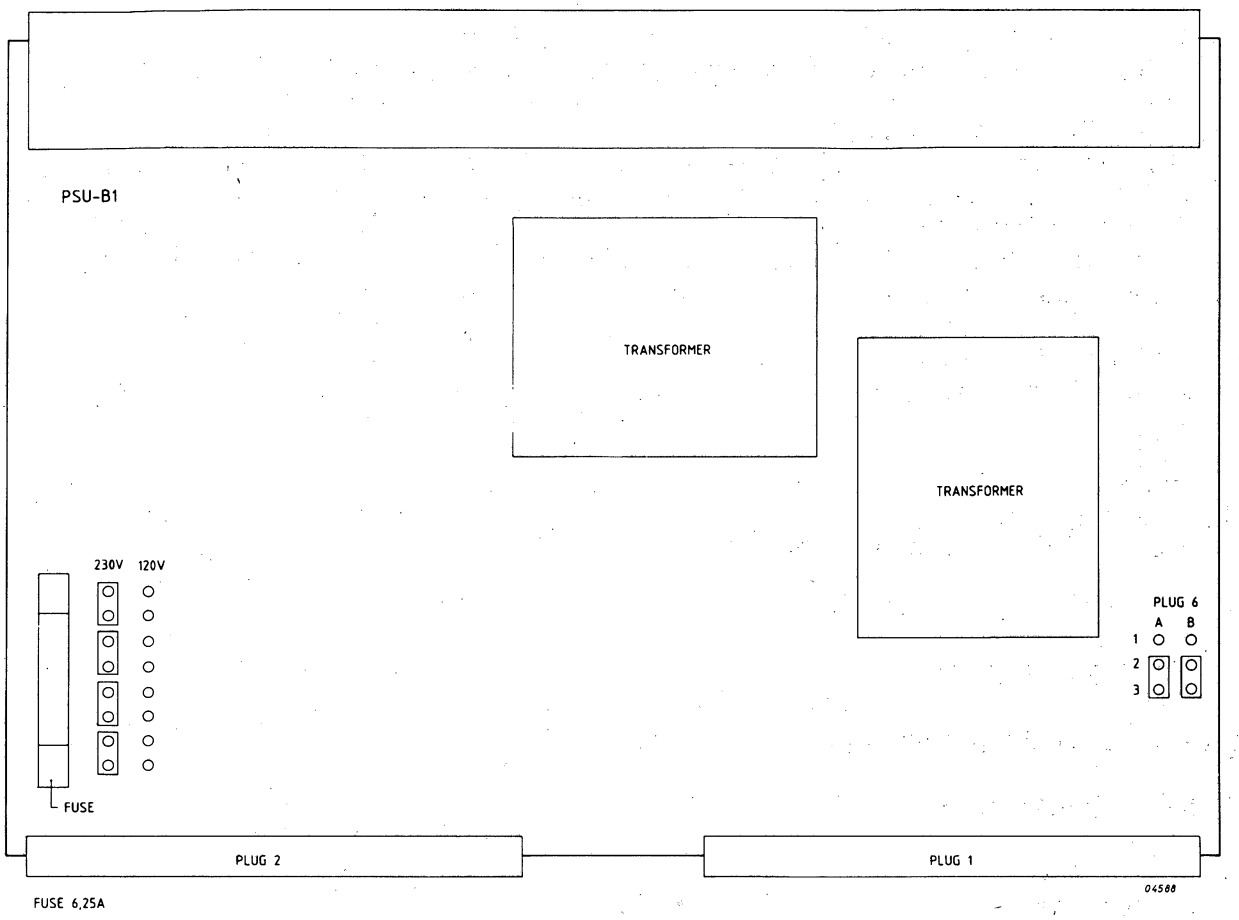
Note: PSU B1 is pin comatible, but has a lower performance.

Technical Data PSU-B1E (P843-400/01)

Input Voltage	- Single phase alternating current
Rated Voltate	- 115V eff ± 20% repluggable 230V eff ± "=% repluggable
Mains Frequency	- 50 Hz, 60 Hz ± "%
Efficiency	- better than 70%
Switching Frequency	- 30 KHz
Short Circuit Protection	- The outputs are protected by current limitation
Storage Time	- Mains losses of half cycle in intervals of more than 1 s will be surmounted.
Connection	- 96-pole female multipoint connector
Dimensions	- 233.4 x 160 x 90 mm
Weight	- 3.1 kg
Environment Conditions	- +5° up to ±55°C relative humidity 10-90%.

DC outputs U-rated	Tolerance	Forced cooling 1m/sec	Peak Current
+5V	± 3%	40 Amp.	
+12V	± 4%	3.5 Amp.	6 Amp.
+24V	± 10%	3.5 Amp.	6 Amp.
-12V	± 4%	1 Amp.	2 Amp.

Table 3.2.7 PERFORMANCE DATA PSU-B1E



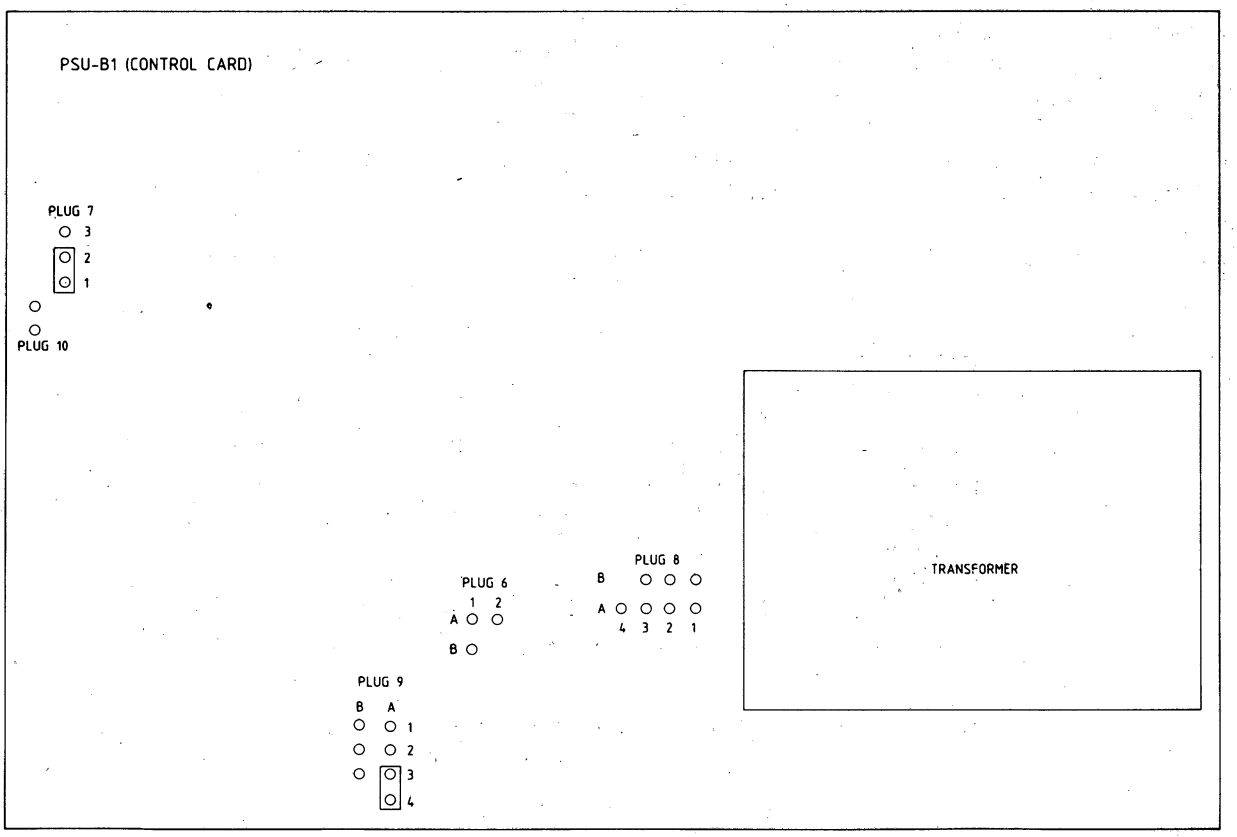


Figure 3.2.17 PSU-B1E

PSU-B1 Interface pinniry

	plug 1 c	b	a		plug 2 c	a
1	MONN	ØV	*			
2	PSON	ØV	PSOFN	2	+5V	+5V
3	PWFN	ØV	*			
4	RSLN	ØV	ØV	4	ØV	ØV
5	PCL	ØV	SYNI			
6	RS-	ØV	ØV	6	+5V	+5V
7	RS+	ØV	SYNO			
8	ØV	ØV	ØV	8	ØV	ØV
9	ØV	ØV	ØV			
10	*	*	*	10	+5V	+5V
11	ØV	ØV	ØV			
12	*	*	*	12	ØV	ØV
13	ØV	ØV	ØV			
14	+24V	+24V	+24V	14	+5V	+5V
15	ØV	ØV	ØV			
16	*	*	*	16	ØV	ØV
17	ØV	ØV	ØV			
18	*	*	*	18	+5V	+5V
19	ØV	ØV	ØV			
20	+12V	+12V	+12V	20	ØV	ØV
21	ØV	ØV	ØV			
22	-12V	-12V	-12V	22	*	*
23	ØV	ØV	ØV			
24	*	*	*	24	*	*
25	ØV	ØV	ØV			
26	+5V	+5V	+5V	26	N	N
27	ØV	ØV	ØV			
28	+5V	+5V	+5V	28	(L	L)
29	ØV	ØV	ØV			
30	+5V	+5V	+5V	30	L1	L1
31	ØV	ØV	ØV			
32	+5V	+5V	+5V	32	*	*

* = not connected

Table 3.2.8 INTERFACE PSU-B1E

3.2.11.2 PSU-M1

Note: PSU M is pin compatible, bus has a lower performance.

Technical Data PSU-M1 (P843-402/01)

Input Voltage	- Single phase alternating current or unregulated direct voltage 24V
Rated Voltage	- 110V ± 10% 220V
Mains Frequency	- 50 Hz, 60 Hz ± 2%
Switching Frequency	- 30 KHz
Short Circuit	- The outputs are protected by current limitation.
Connection	- 96 and 32 pole connector
Dimensions	- 233.4 x 160 x 46 mm

DC outputs U-rated	Voltage Tolerance	24V Supply I-rated	AC Supply I-rated
+5VM	± 3%	4 Amp.	1 Amp.
+12VM	± 4%	1.5 Amp.	0.8 Amp.
+12VB (*)		0.5 Amp.	0.5 Amp.

(*) = Battery charge at 13.8V max.

Table 3.2.9 PERFORMANCE DATA PSU-M1

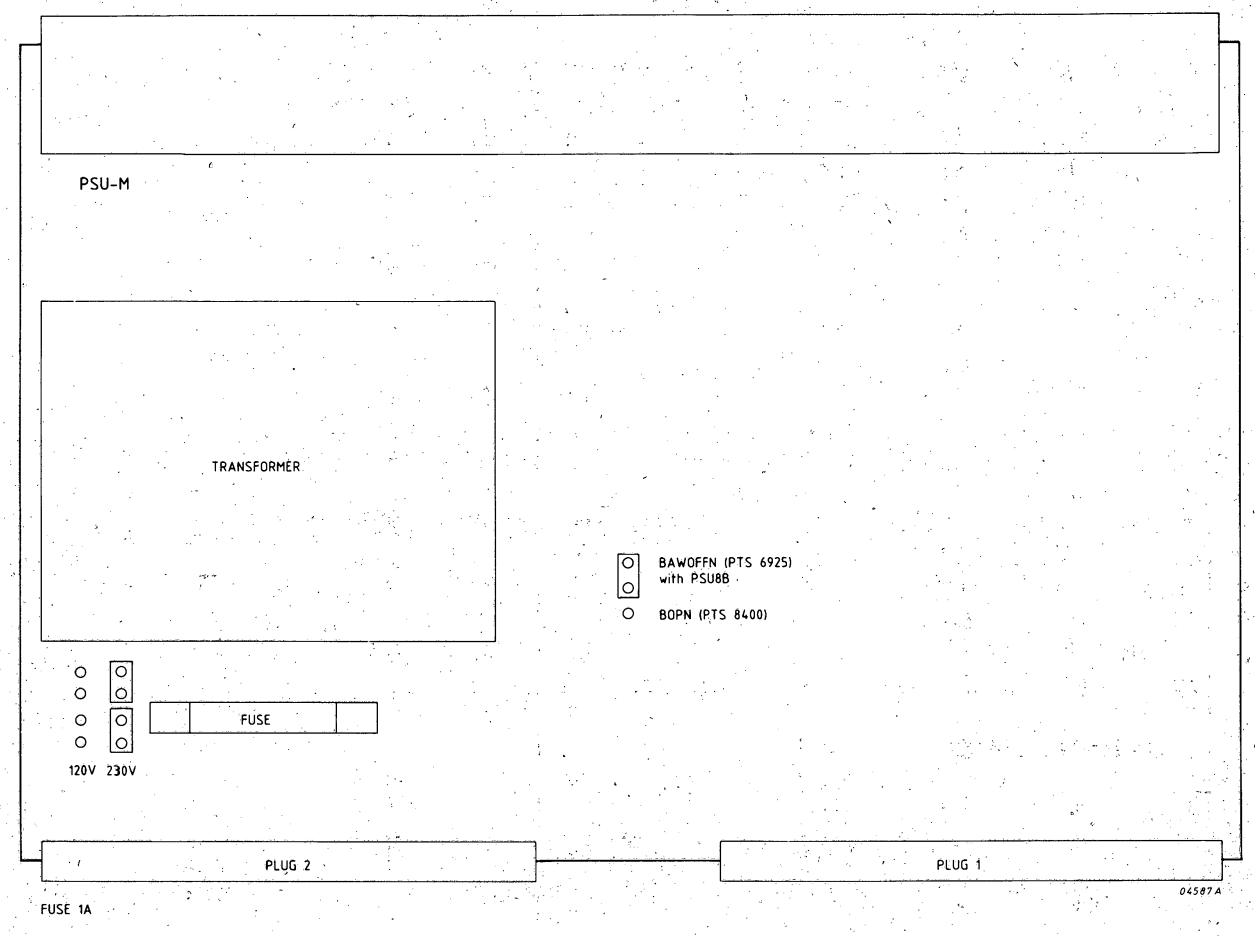


Figure 3.2.18 PSU-M1

PSU-M1 Interface pinning

	plug 1			plug 2	
	c	b	a	c	a
1	*	ØV	BONN		
2	*	ØV	ØV	*	*
3	PWFN	ØV	BOPN		
4	RSLN	ØV	ØV	ØV	ØV
5	*	ØV	SYNI		
6	*	ØV	ØV	*	*
7	*	ØV	*		
8	ØV	ØV	ØV	ØV	ØV
9	ØV	ØV	ØV		
10	*	*	*	*	*
11	ØV	ØV	ØV		
12	*	*	*	ØV	ØV
13	ØV	ØV	ØV		
14	+24V	+24V	+24V	*	*
15	ØV	ØV	ØV		
16	+12VM	+12VM	+12VM	ØV	ØV
17	ØV	ØV	ØV		
18	+5VM	+5VM	+5VM	*	*
19	ØV	ØV	ØV		
20	+12VB	+12VB	+12VB	ØV	ØV
21	ØV	ØV	ØV		
22	*	*	*	*	*
23	ØV	ØV	ØV		
24	*	*	*	*	*
25	ØV	ØV	ØV		
26	*	*	*	N	N
27	ØV	ØV	ØV		
28	*	*	*	L	L
29	ØV	ØV	ØV		
30	*	*	*	*	*
31	ØV	ØV	ØV		
32	*	*	*	*	*

* = not connected

Table 3.2.10 INTERFACE PSU-M1

3.2.11.3 FILTERBOARD PSU8B

Technical Data Filterboard

Input Voltage	- Single phase alternating current
Rated Voltage	- 99V - 132V low range ┐ plug 198V - 264V high range ┘ selectable
Mains Frequency	- 48 - 63 Hz
Connection	- 64-pole female multipoint connector
Dimensions	- 233.4 x 16Ø x 46 mm

plug 1

	c	b	a
1		0V	PWFN
2		0V	
3	PWFAN	0V	RTCN
4		0V	0V
5	PCL	0V	
6		0V	0V
7		0V	
8	0V	0V	0V
9	0V	0V	0V
10			
11	0V	0V	0V
12			
13	0V	0V	0V
14	+24VE	+24VE	+24VE
15	0V	0V	0V
16			
17	0V	0V	0V
18			
19	0V	0V	0V
20	+12V	+12V	+12V
21	0V	0V	0V
22			
23	0V	0V	0V
24	-5V	-5V	-5V
25	0	0	0
26	+5V	+5V	+5V
27	0	0	0
28	+5V	+5V	+5V
29	0	0	0
30	+5V	+5V	+5V
31	0	0	0
32	+5V	+ 5V	+5V

plug 2

	c	a
2		
4		
6		
8		
10		
12		
14		
16		
18		
20		
22	N	N
24	LSS	LSS
26	NF	NF
28	LF	LF
30	LFS	LFS
32	LS	LS

Table 3.2.11 INTERFACE PSU8B

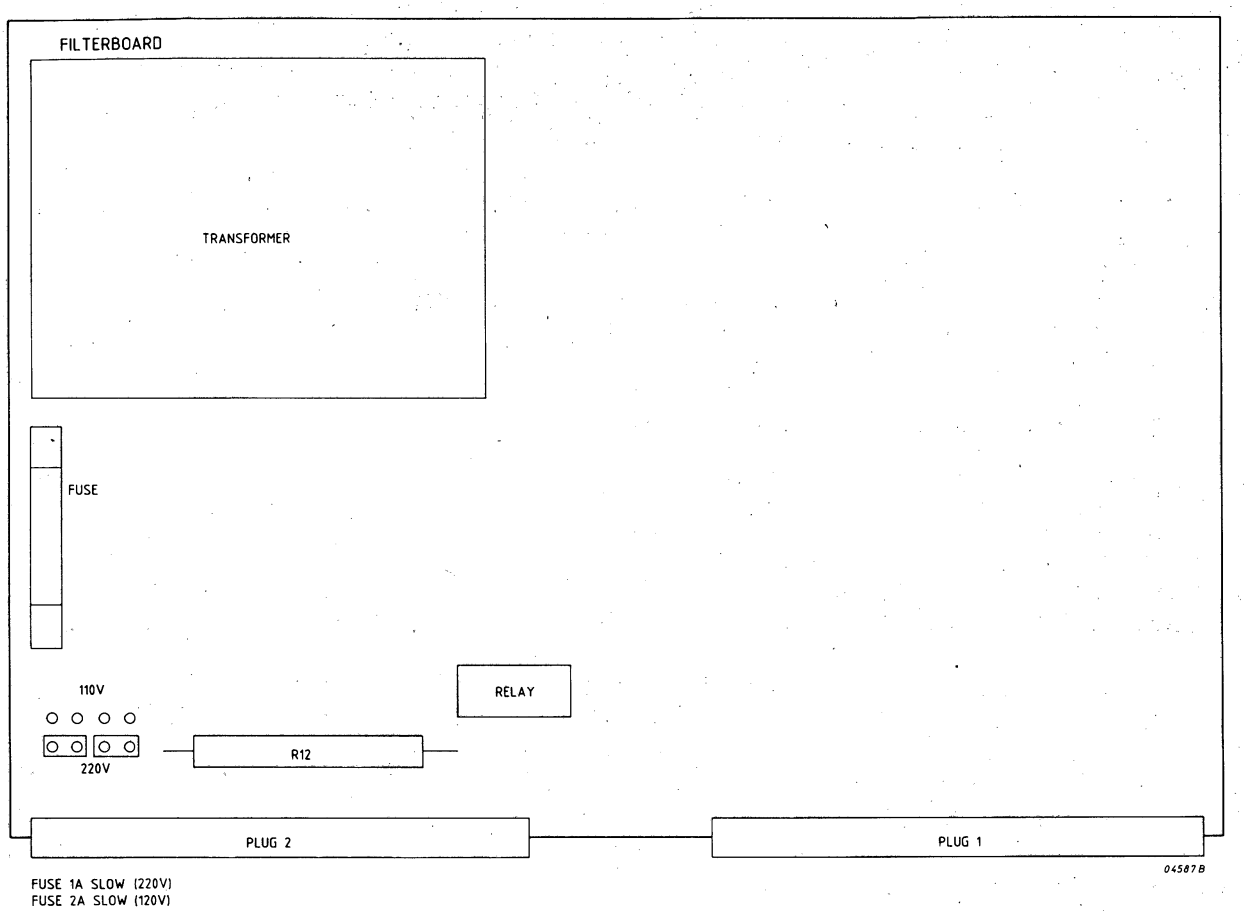


Figure 3.2.19 FILTERBOARD PSU8B

3.3 RACK RAWIST P829-001/005

3.3.1 IDENTIFICATIONS

P829-001 BASIC RACK 8"-DISK

For the purpose of secondary memory extension based on 8" winchester fixed disk, this rack is equipped with the PRIAM disk, 35M bytes model DISKOS 3450. The disk is vertically mounted with its proper mounting accessories, and the internal cabling (e.g. links between WS120E and disk) is pre-wired.

All the necessary external cables are delivered with the rack. The cables are depending of the 3 possible uses of the racks:

P829-001/01 : First 8" disk rack for P871 or P874-300.
P829-001/11 : First 8" disk rack for P874-400 or P876.
P829-001/02 : Second 8" disk rack.

Basic Rack Part numbers (P829-001/01/11/02):

5111 010 08850	PRIAM 3450-011 Disk-35MB	
5111 100 52230	Identification P829-001	
5111 199 53510	Ventilation Assembly RAWIST	
5111 199 53540	Cable Remote WS120E RAWIST	
5111 199 53560	Cable Current Limit RAWIST	
5111 199 53860	Cable Logic 4 PRIAM RAWIST	(P829-001/02)
5111 199 53870	Cable Logic 2 PRIAM RAWIST	(P829-001/01 or /11)
5111 199 53910	Cable Remote/DC RA12F-RAWIST	(P829-001/01)
5111 199 53930	Cable Remote/DC RAL22F-RAWIST	(P829-001/11)
5111 199 53950	Kit 120V 4A	
5111 199 53960	Mounting Kit RAWIST	
5111 199 53970	Panel Assy RAWIST	
5111 199 54270	Cable AC WS120E 6927 EXT	
5111 199 54310	Mounting Accessory PSU WS120E	
5111 199 54340	Mounting Accessory Disk PRIAM 6927	
5111 199 54380	Rack Basic RAWIST	
5111 199 54590	Cable DC Disk PRIAM 6927	
5111 199 55010	Back Panel WS120E	
5112 291 77780	PSU WS120E	

P829-002 ADDITIONAL 8"-DISK FOR P829-001

As an option a second 8" disk can be mounted as well in the first rack as in the second one. Therefore, up to 4 drives can be attached to the same system (same control unit).

P829-002/01: 8" PRIAM Disk with POWER SUPPLY and CABLES:

Part numbers:

5111 010 08850	PRIAM 3450-011 disk-35MB
5111 199 53550	Cable Inter BP WS120E
5111 199 54270	Cable AC WS120E 6927 Ext
5111 199 54310	Mounting Accessory PSU WS120E
5111 199 54340	Mounting Accessory Disk PRIAM 6927
5111 199 54590	Cable DC Disk PRIAM 6927
5111 199 55010	Back Panel WS120E
5112 291 77780	PSU WS120E

P829-005 BASIC RACK 5"¼ - DISK

For the purpose of secondary memory extension based on 5"¼ disk, this rack is equipped with the SEAGATE disk, 10M bytes, model ST412 and a XEBEC controller model ST410. They are mounted with their proper mounting accessories and the internal cabling is pre-wired.

All the external cables will be delivered with the rack. The cables are depending of the 3 possible used of the rack:

P829-005/01 : First 5"¼ disk rack for P871 or P874-300.
P829-005/11 : First 5"¼ disk rack for P874-400 or P876.
P829-005/02 : Second 5"¼ disk rack.

Basic Rack Part numbers (P829-005/01/11/02):

5111 100 52240	Identification P829-005
5111 199 52700	Cable DC XEBEC
5111 199 53480	Cable C.L. SEAGATE RAWIST
5111 199 53510	Ventilation Assembly RAWIST
5111 199 53540	Cable Remote WS120E RAWIST
5111 199 53590	Disk Assembly SEAGATE-10MB (See Note)
5111 199 53810	Cable DC Disk SEAGATE
5111 199 53880	Cable Logic SEAGATE (6M) (P829-005/01 or /11)
5111 199 53910	Cable TEL/DC RA12F-RAWIST (P829-005/01)
5111 199 53920	Cable Cont. Sign. SEAGATE RAWIST
5111 199 53930	Cable TEL/DC RAL22F-RAWIST (P829-005/11)
5111 199 53950	Kit 120V 4A
5111 199 53960	Mounting Kit RAWIST
5111 199 53970	Panel Assy RAWIST
5111 199 54270	Cable AC WS120E 6927 EXT
5111 199 54310	Mounting Accessory Disk SEAGATE
5111 199 54380	Basic Rack RAWIST
5111 199 55010	Back Panel WS120E
5111 199 56130	Cable Data Signal SEAGATE
5112 219 77780	PSU WS120E

Note: Assembly Disk SEAGATE - 10M includes:

5111 010 08450	Card XEBEC
5111 010 08460	Drive 5"¼ SEAGATE - 10MB

P829-006 ADDITIONAL 5"¼ - DISK FOR P829-005

As an option a second 5"¼ disk can be mounted as well in the first rack as in the second one. Therefore up to 4 drives can be attached to the same system (same control unit).

P829-006/01: 5"¼ SEAGATE disk with CABLES

Part numbers:

5111 010 08460	Drive 5"¼ SEAGATE - 10MB
5111 199 53810	Cable DC Disk SEAGATE
5111 199 53890	Cable Data EXT SEAGATE
5111 199 54330	Mounting Accessory SEAGATE

P830-035 FLEXIBLE DISK OPTION

A 8" flexible disk, model CDC 9406, can be installed, as an option, only in the first -either 8" disk or 5"¼ disk- extension rack, provided only one fixed disk is mounted.

P830-035/11: FLOPPY-1MB with CABLES

Part numbers:

5111 010 04770	Floppy 1MB 220V 50Hz with Door Lock
5111 199 53790	Cable DC FDD RAWIST
5111 199 53800	Cable AC FDD RAWIST
5111 199 54350	Mounting Accessory FDD (RAWIST)

P829-010 STREAMER CARTRIDGE - DRIVE OPTION

A 8" foot-print 20Mbytes ARCHIVE Streamer drive, type "Sidewinder" and a formatter can be installed, as an option in the first -either 8" disk or 5"¼ disk- extension rack, provided only one fixed disk is mounted.

P830-010/01: STREAMER (with FORMATTER) and CABLES

Part numbers:

5111 010 08801	Streamer 20MB St27 (with Formatter)
5111 199 52240	Adaption Assembly
5111 199 54030	Cable DC Streamer RAWIST
5111 199 54040	Cable Logic Disk ST RAWIST
5111 199 54320	Mounting Accessory Streamer (RAWIST)

3.3.2 GENERAL DESCRIPTION

The RAWIST (Rack Winchester Streamer) is an extension rack system, to be used for the P871, P874 and P876 minicomputers.

The RAWIST is a 19" rack intended to offer 8" or 5"¼ winchester disks extension to the P800 line.

Within the same rack, facilities are also provided to combine, in addition to a winchester drive, one 8" flexible disk and/or one 8" foot-print streamer drive or a second winchester drive.

Besides the drives, RAWIST houses the necessary power supply module(s), the mains distribution/filtering and ventilation units.

Up to two RAWIST racks can be connected to the same system.

	1st RAWIST										2nd RAWIST			
CONFIGURATION	1	2	3	4	5	6	7	8	9	10	1	2	3	4
8" PRIAM	1	1	1	1	2	0	0	0	0	0	1	2	0	0
5"¼ SEAGATE	0	0	0	0	0	1	1	1	1	2	0	0	1	2
8" Floppy	-	1	-	1	0	-	1	-	1	0	0	0	0	0
8" Streamer	-	-	1	1	0	-	-	1	1	0	0	0	0	0

Table 3.3.1 CONFIGURATIONS RAWIST

3.3.3 MAINS CONNECTION

RAWIST is powered through a mains cord to be connected in an independant way of the basic computer rack.

The mains power characteristics is:
. Upper range : 200 to 240 volts,
. Lower range : 100 to 127 volts,
The ranges are switchable on the ventilation unit (DISWST) and on the WS120E power module.
If a FLOPPY drive is mounted, it must be a version with the correct mains tension/frequency (220V/50Hz).

. Frequency : 48 to 63 Hertz.

As standard, a "110V adaptation" kit, (fuse and label) is delivered with every rack.
The mains input is protected by a 2 Amp (230V) or a 4 Amp (120V) fuse.

3.3.4 PHYSICAL DESCRIPTION

The common parts of RAWIST are:

. A metallic frame, 6U high, 19" rack mountable, housing the rest of the parts;
. A ventilation unit, built-in on the rear side of the rack with a mains filtering and distribution unit with provision for internal cables connections. Two FANS are built in with air outlets at the rear.
. A WS120E power module for supplying the disk D.C. voltages. Besides this module are provided its mounting accessories and a printed board for connections and DC distribution;
. A 6U front panel. With removable plates to provide openings for a FLOPPY drive and/or a STREAMER tape-drive.

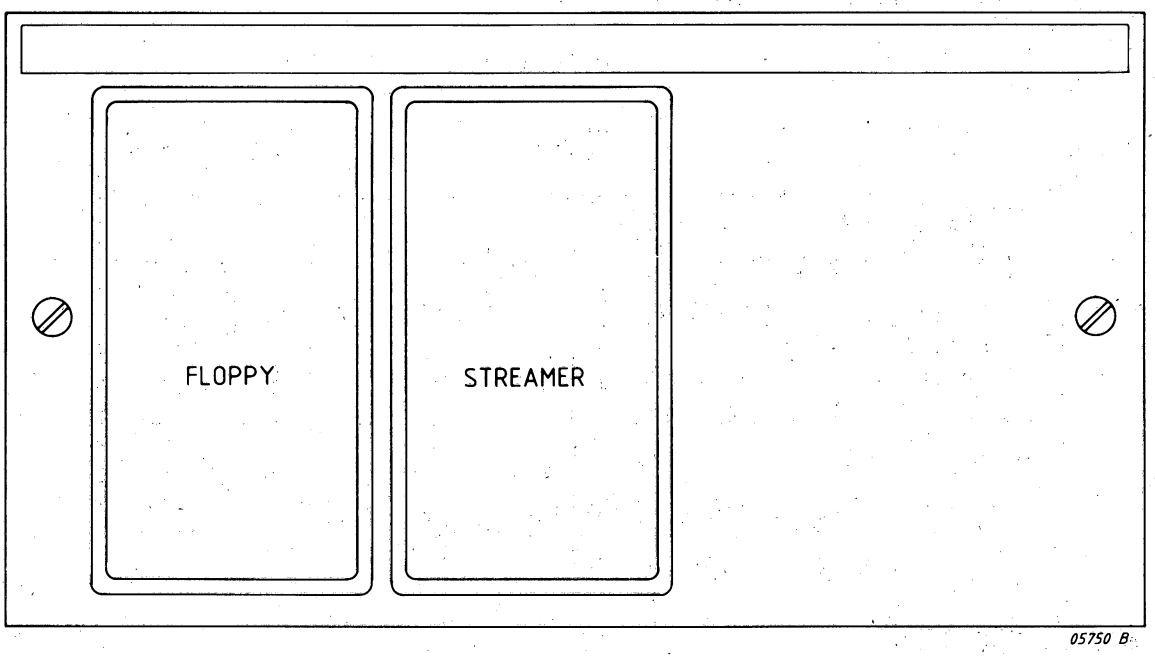


Figure 3.3.1 FRONT-PANEL RAWIST (5111 199 53970)

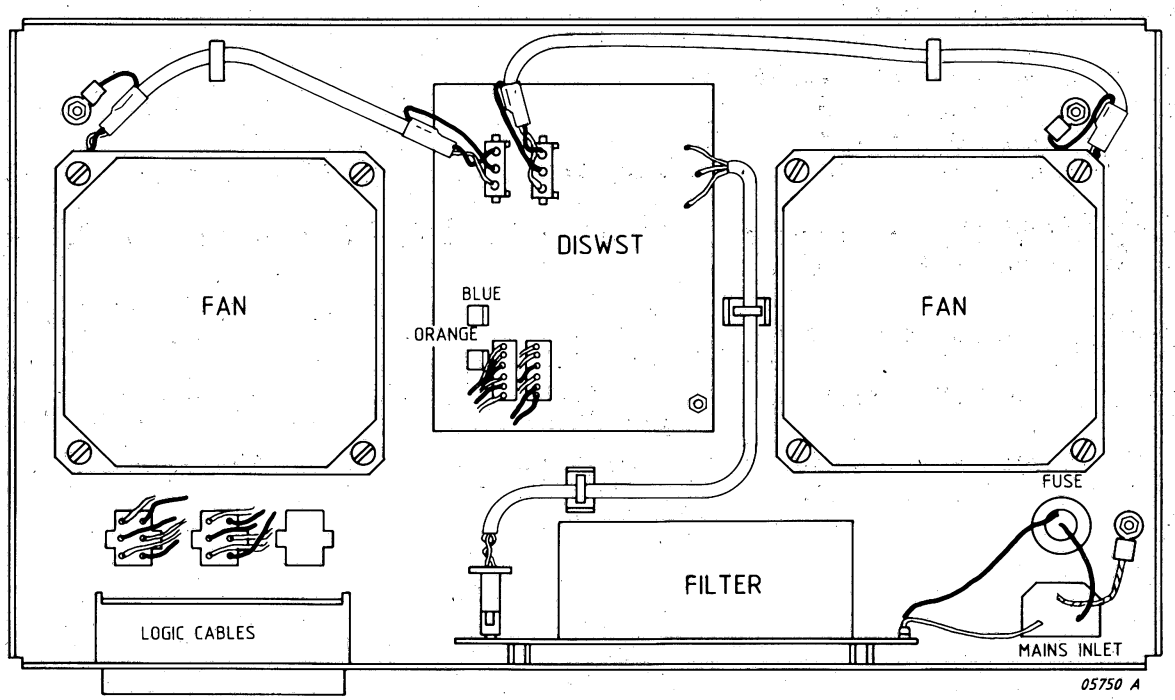


Figure 3.3.2 VENTILATION ASSEMBLY RAWIST (5111 199 53510)

VENTILATION ASSEMBLY RAWIST contains the following main parts:

2 x cable 5V, 24V	5111 199 53571
1 x pcb DISWST	5111 199 53651
2 x fan (110V)	2811 031 01063
1 x filter	5112 291 75702

fuse:

220V 2A slow, 313002	2422 086 01071
110V 4A slow, 313004	2422 086 01428 (Kit 120V 4A)

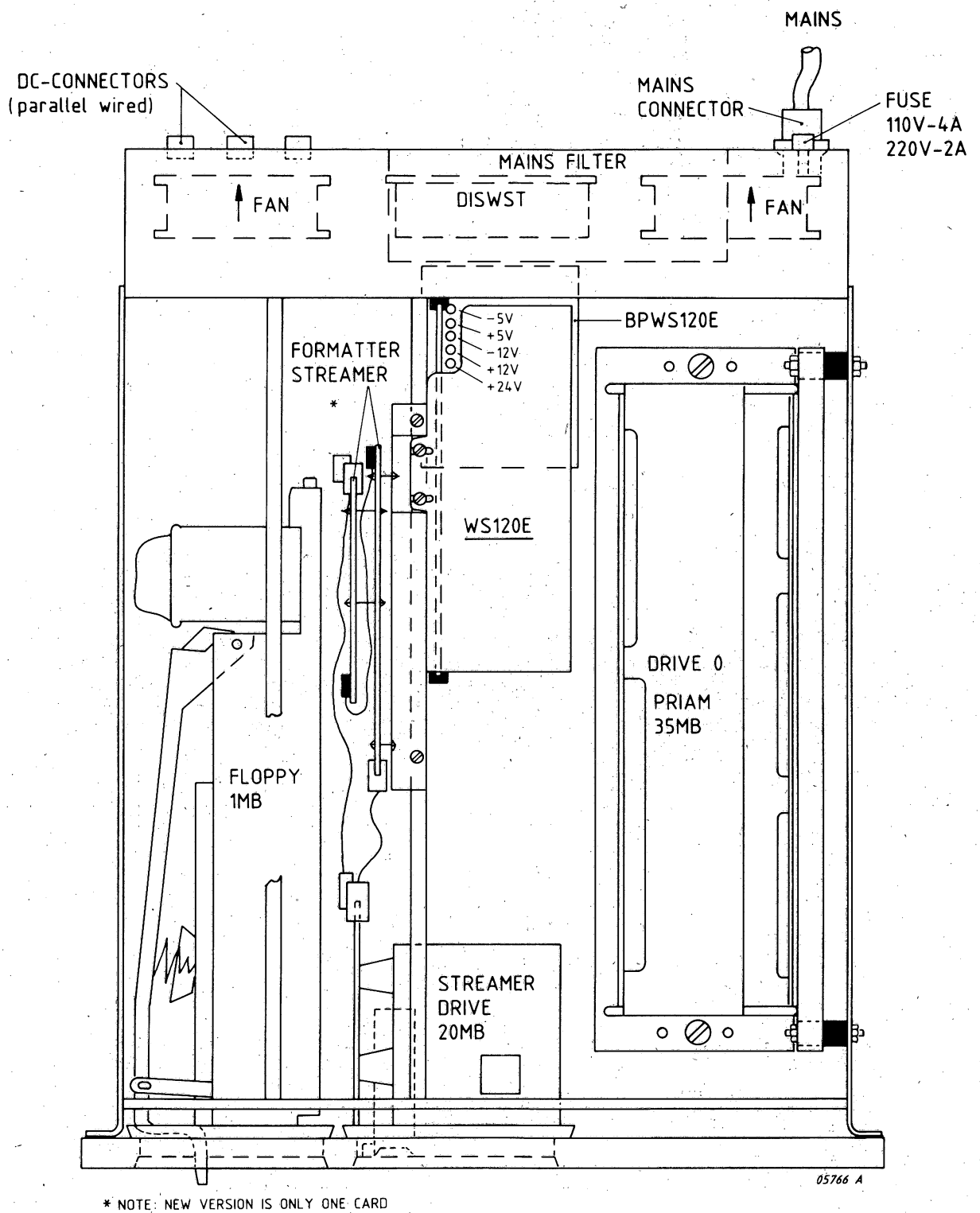


Figure 3.3.3 P829-001 LOCATOR (FIRST RACK)

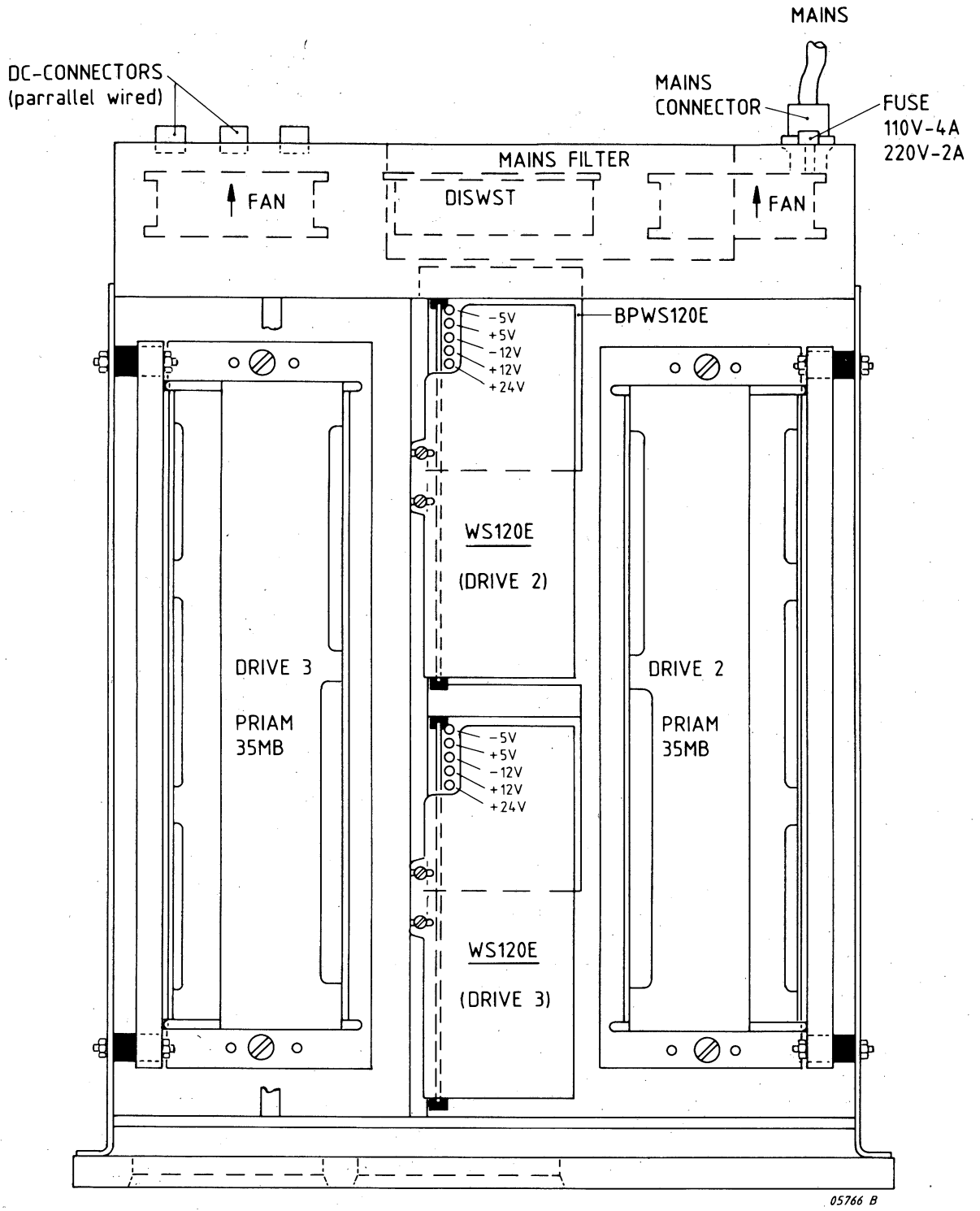
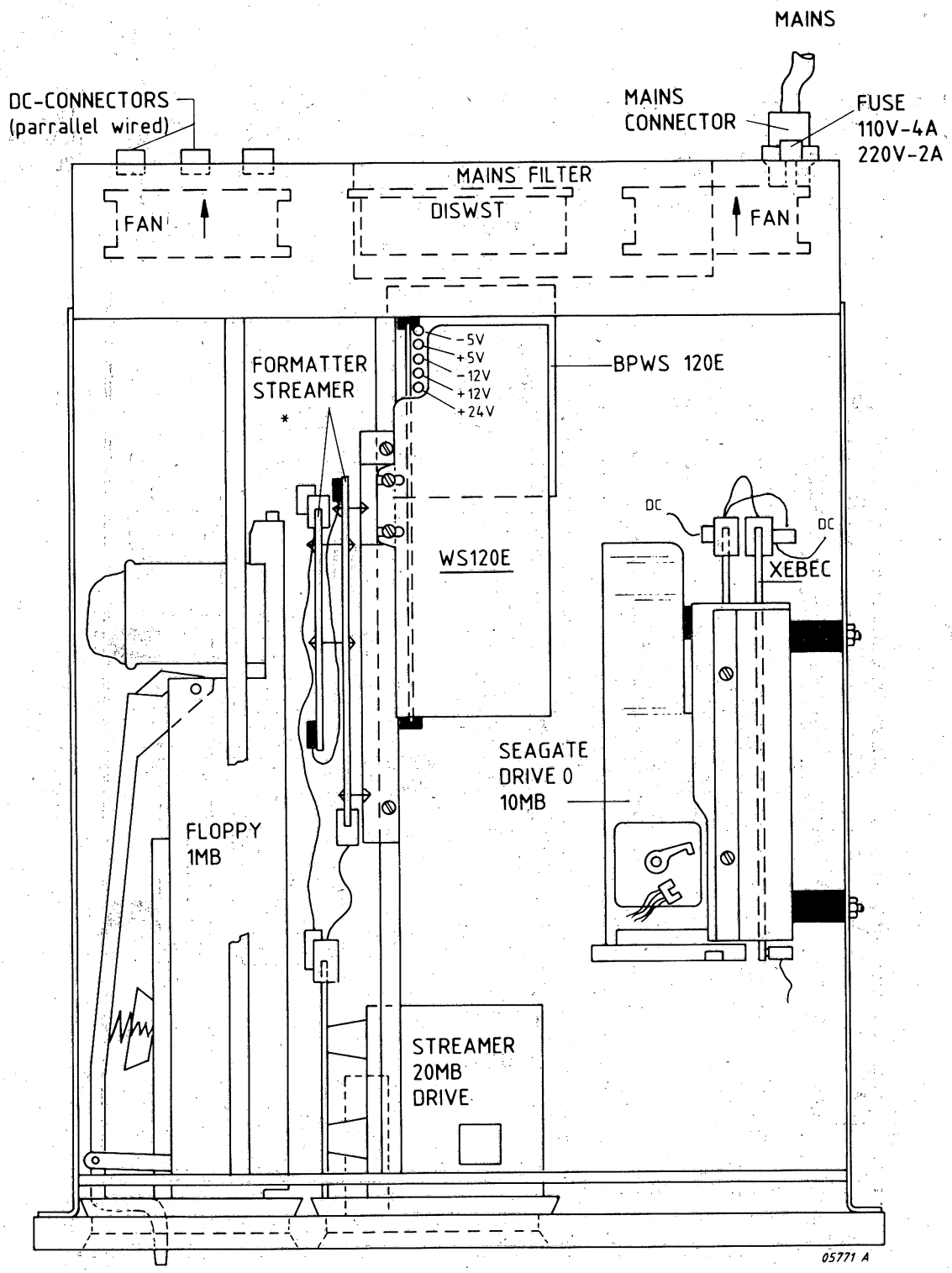


Figure 3.3.4 P829-001 LOCATOR (SECOND RACK)



* NOTE: NEW VERSION IS ONLY ONE CARD

Figure 3.3.5 P829-005 LOCATOR (FIRST RACK)

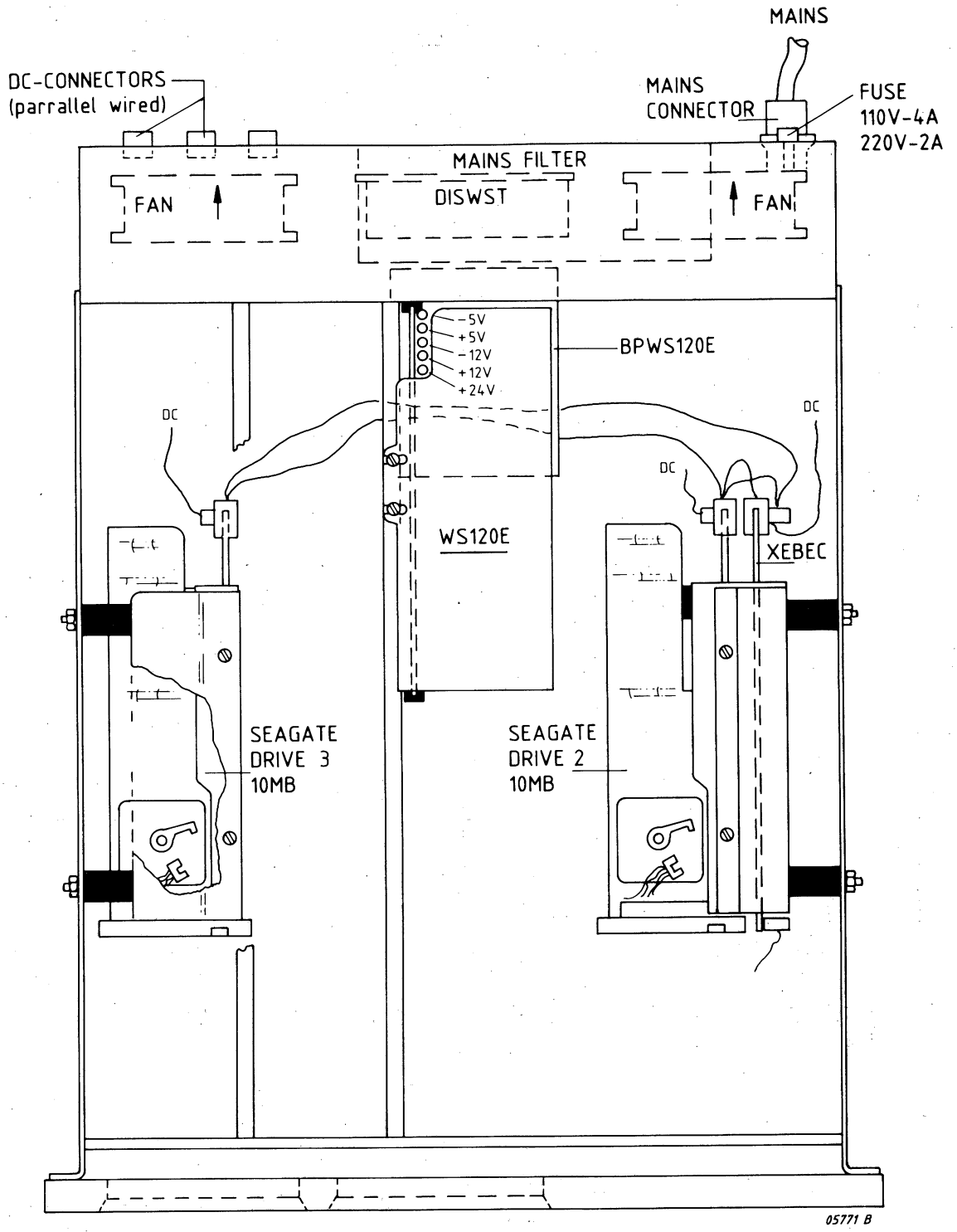


Figure 3.3.6 P829-005 LOCATOR (SECOND RACK)

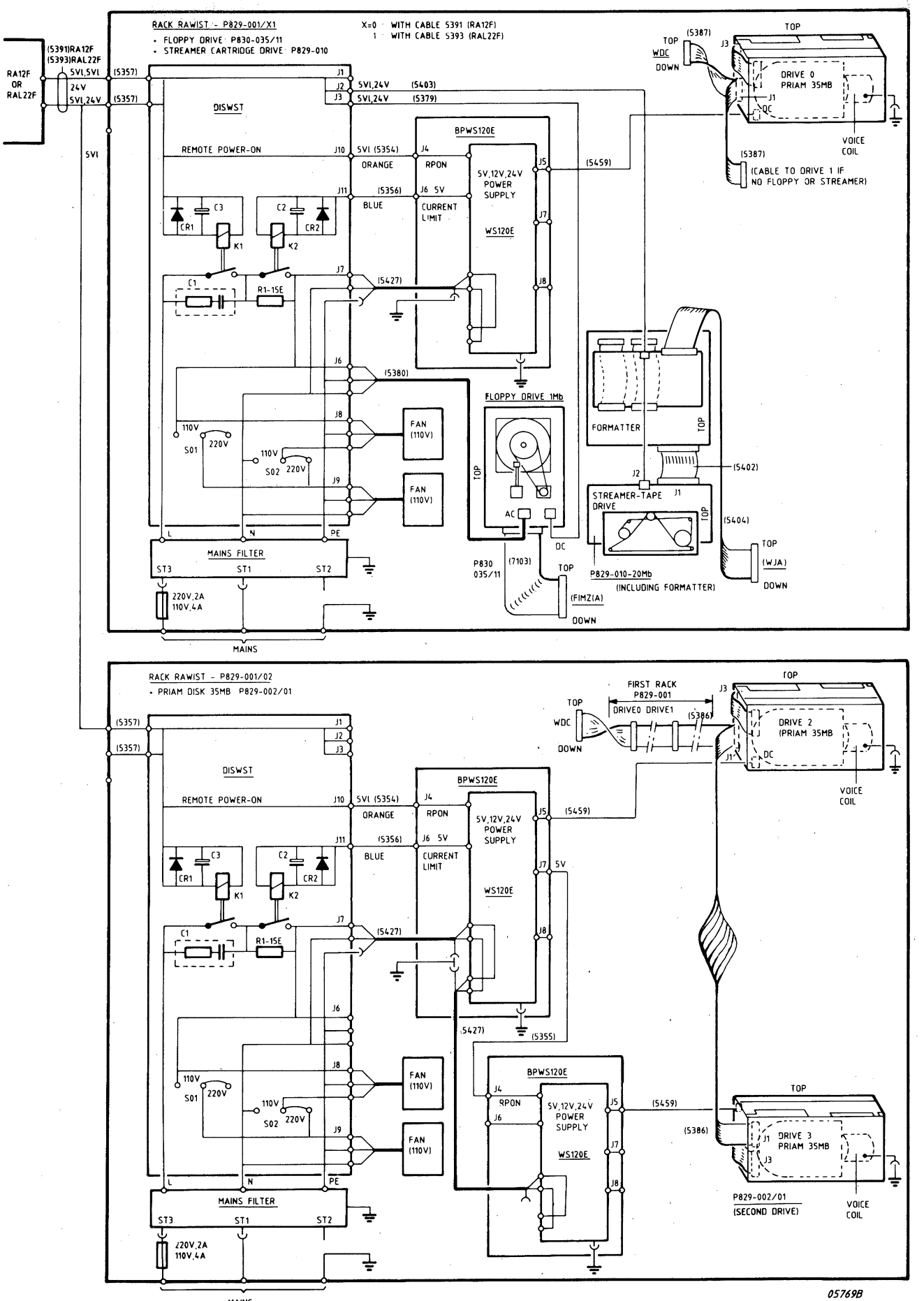


Figure 3.3.7 P829-001 INTERCONNECTIONS

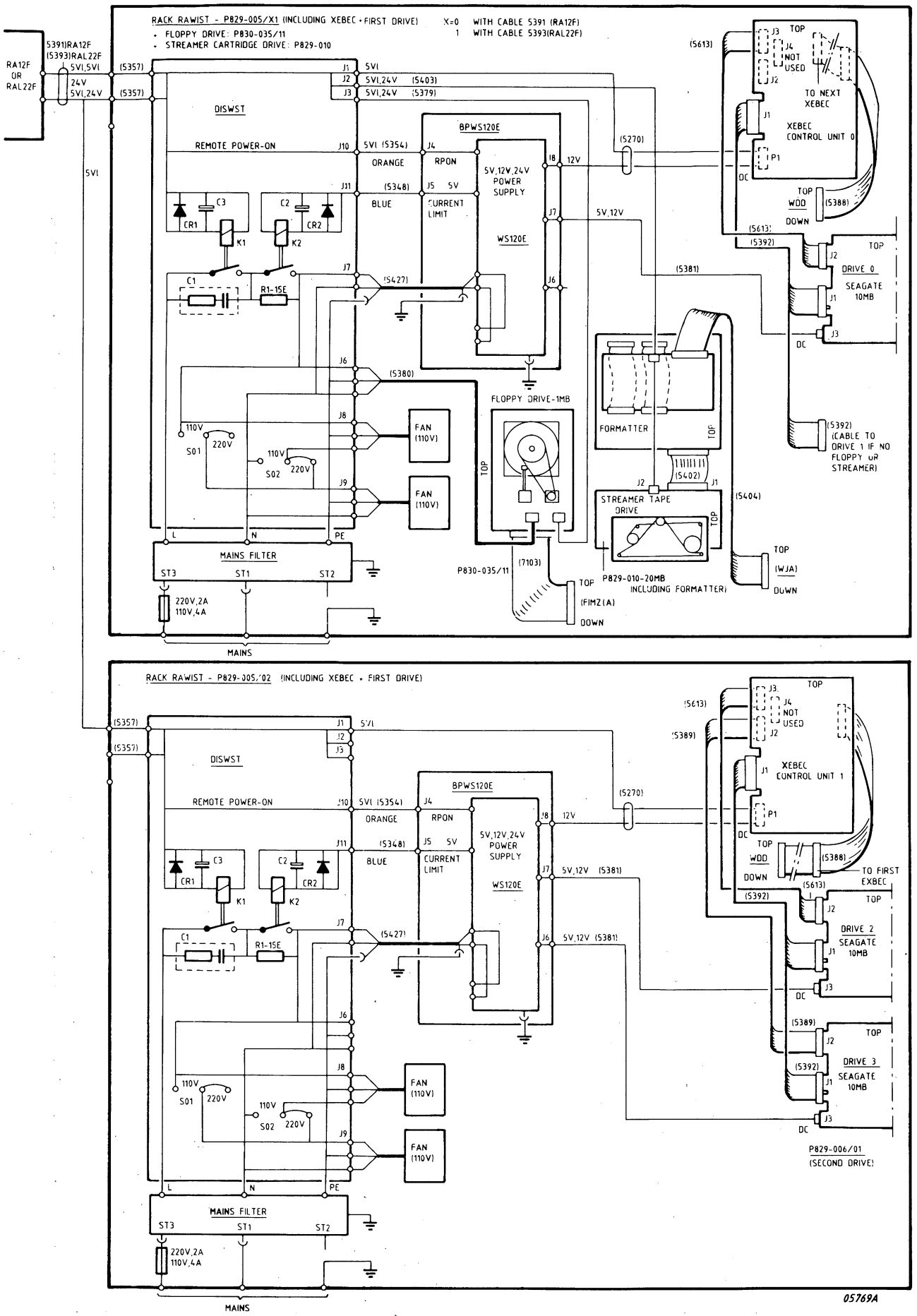
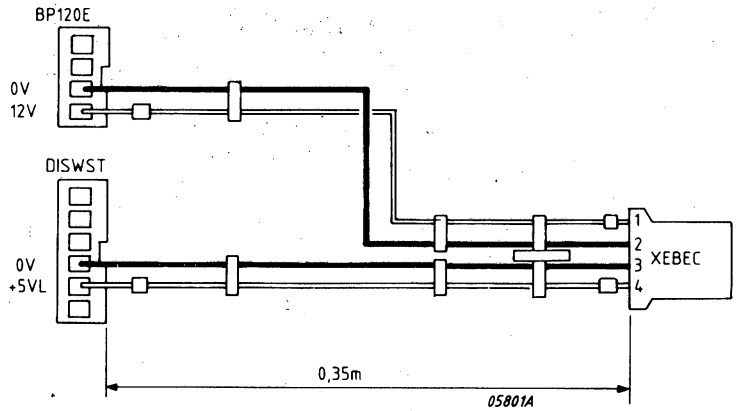
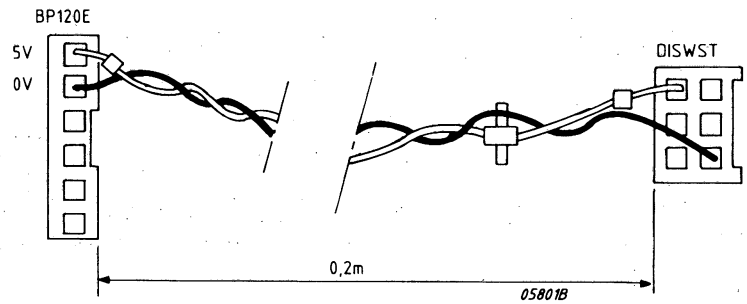


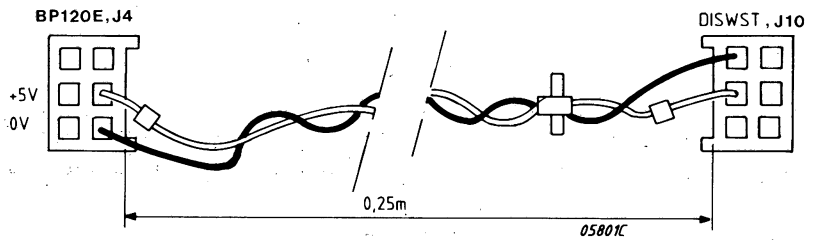
Figure 3.3.8 P829-005 INTERCONNECTIONS



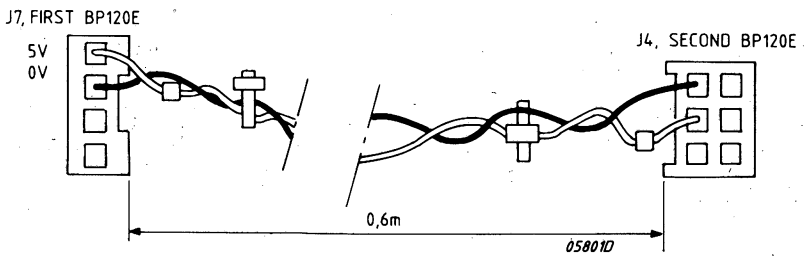
a) CABLE DC XEBEC 5111 199 52700



b) CABLE "CURRENT LIMIT" SEAGATE 5111 199 53480

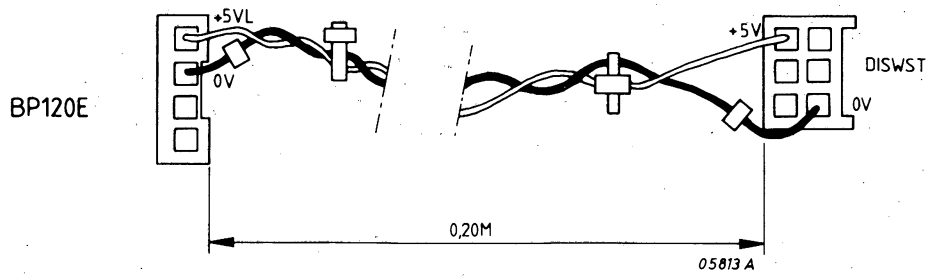


c) CABLE REMOTE 5111 199 53540

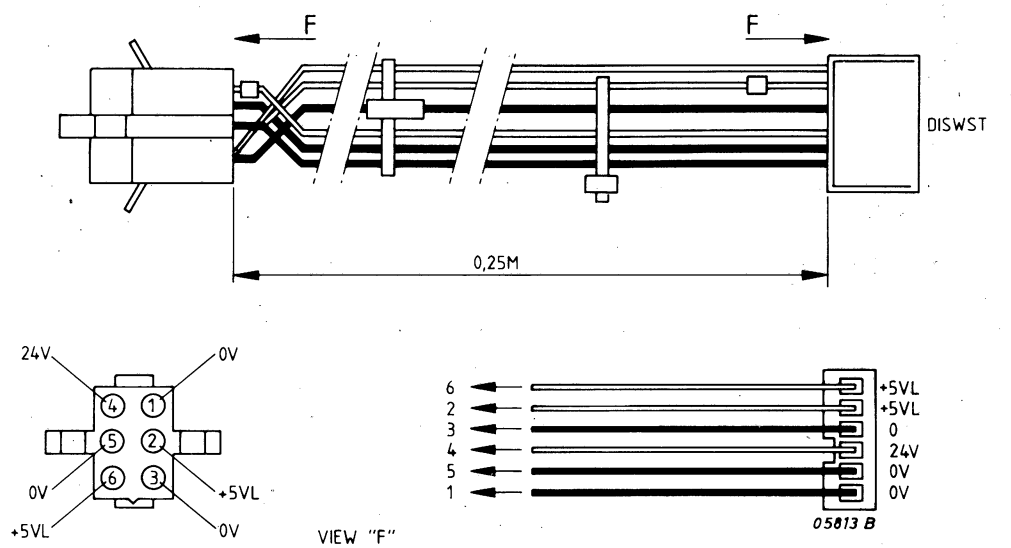


d) CABLE "INTER BACKPANEL" WS120E 5111 199 53550

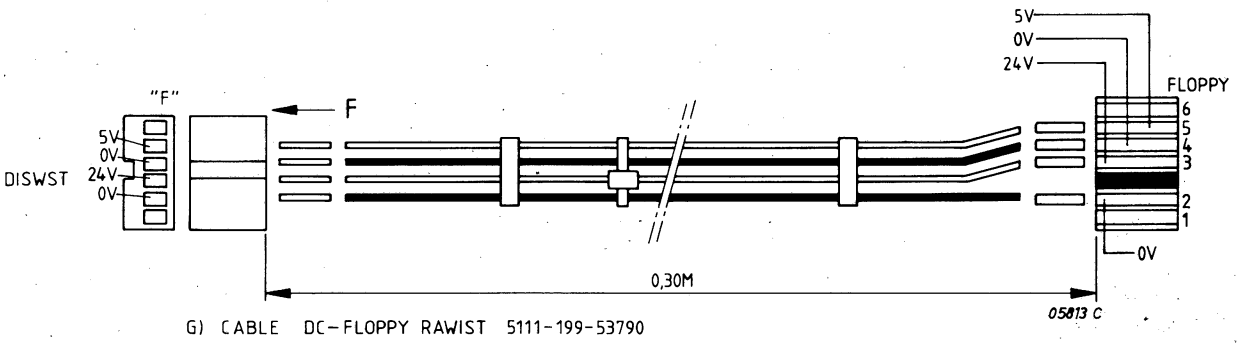
Figure 3.3.9 CABLES RAWIST



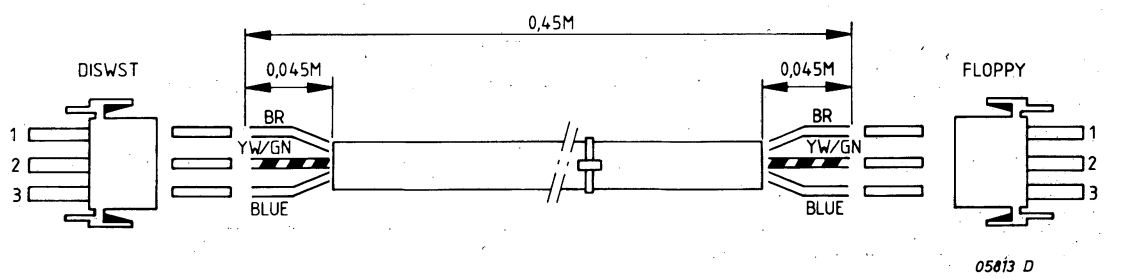
E) CABLE "CURRENT LIMIT" 5111-199-53560



F) CABLE 5V, 24V ENS. VENT. RAWIST 5111-199-53570

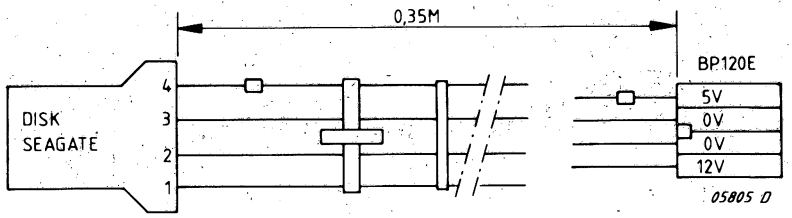


G) CABLE DC-FLOPPY RAWIST 5111-199-53790

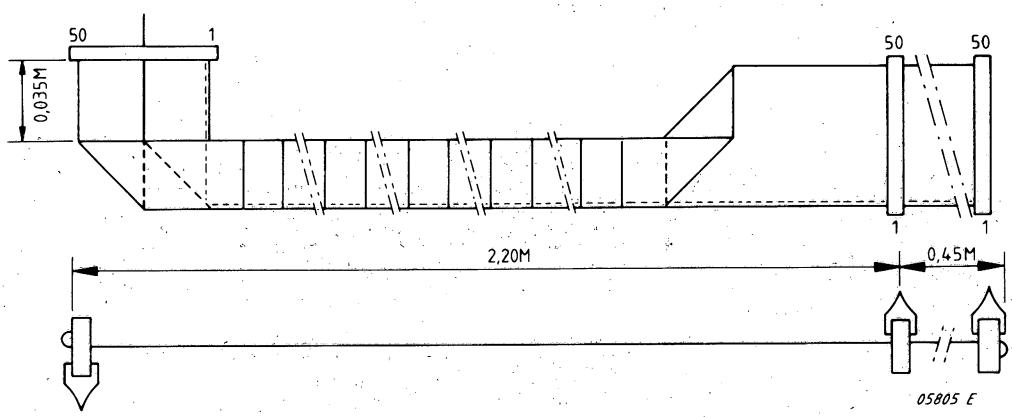


H) CABLE AC-FLOPPY RAWIST 5111-199-53800

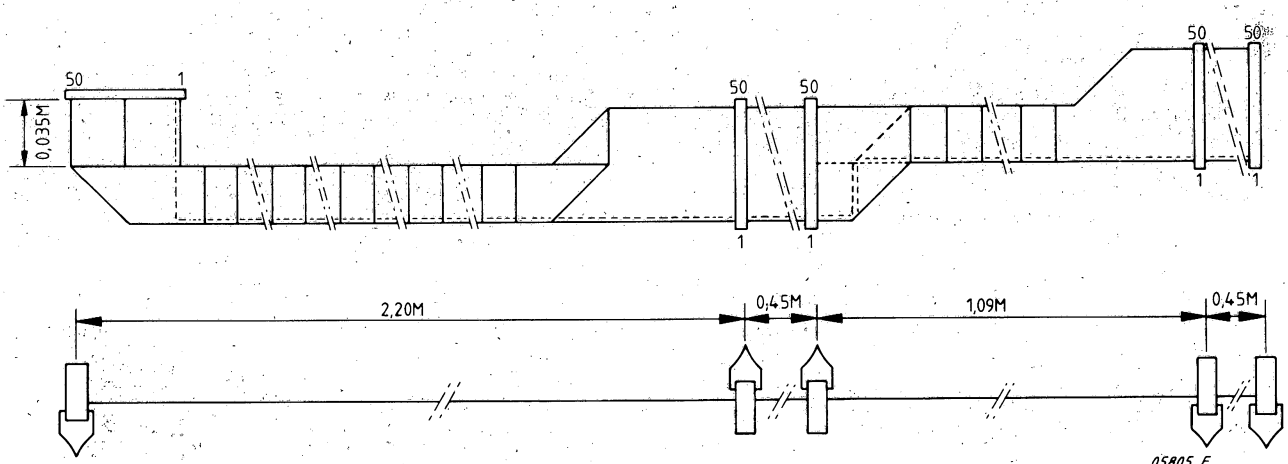
Figure 3.3.9 CABLES RAWIST (CONT'D)



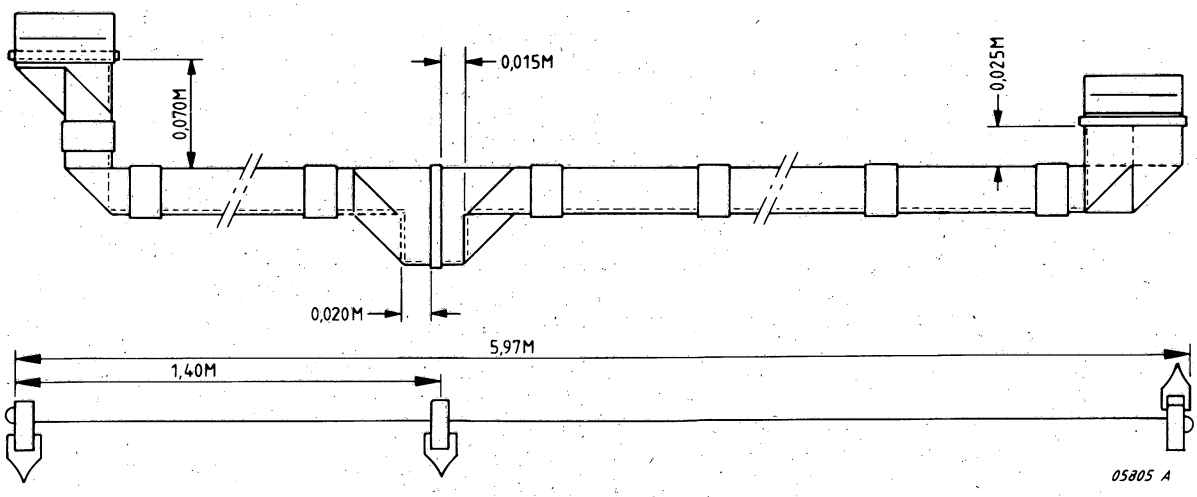
I) CABLE DISK-SEAGATE 5111-199-53810



J) CABLE LOGIC 2 PRIAM 5111-199-53870

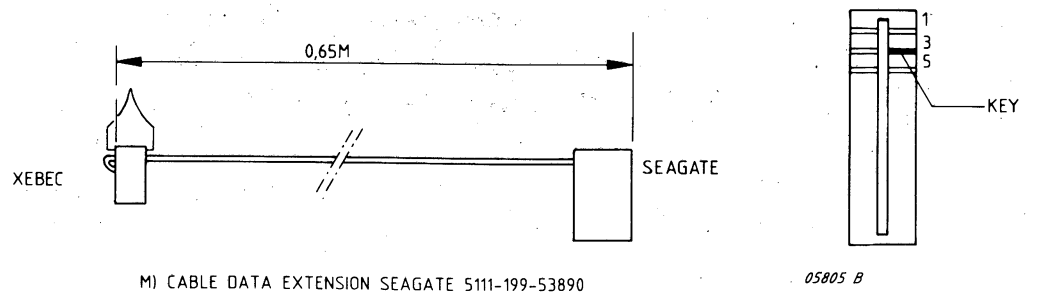


K) CABLE LOGIC 4 PRIAM 5111-199-53860

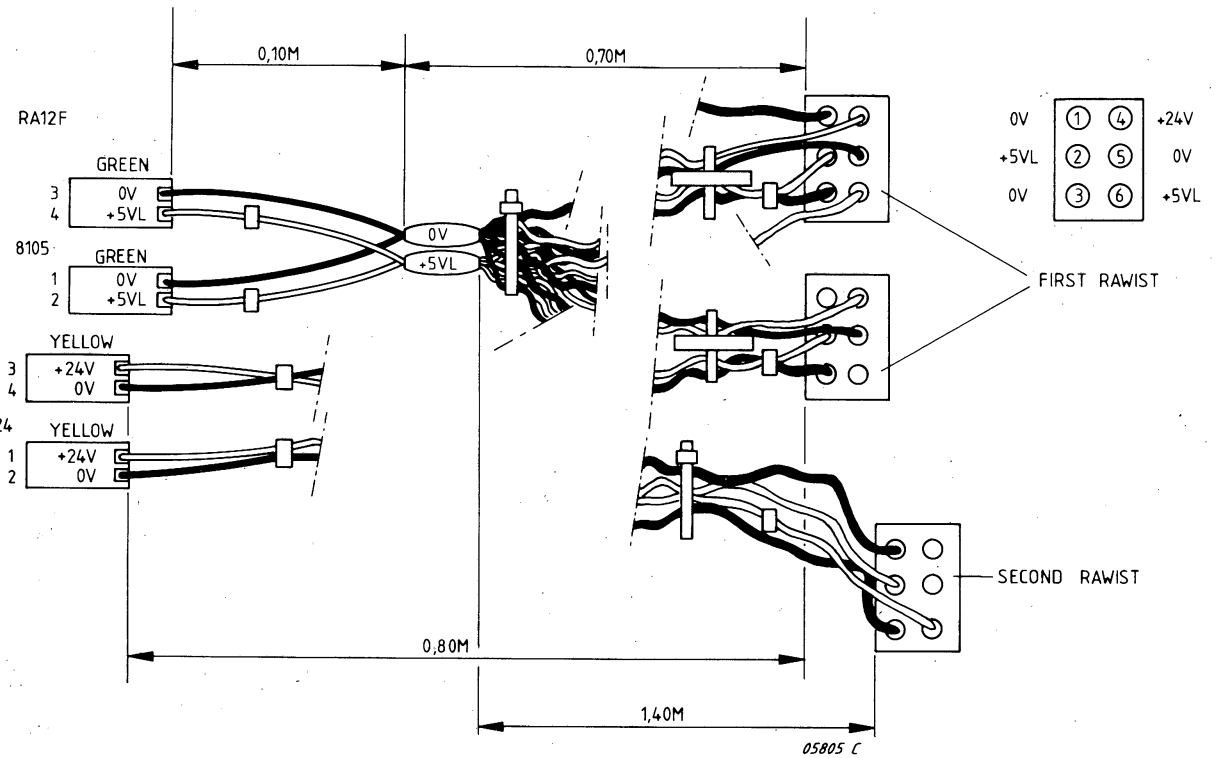


L) CABLE LOGIC SEAGATE 5111-199-53880

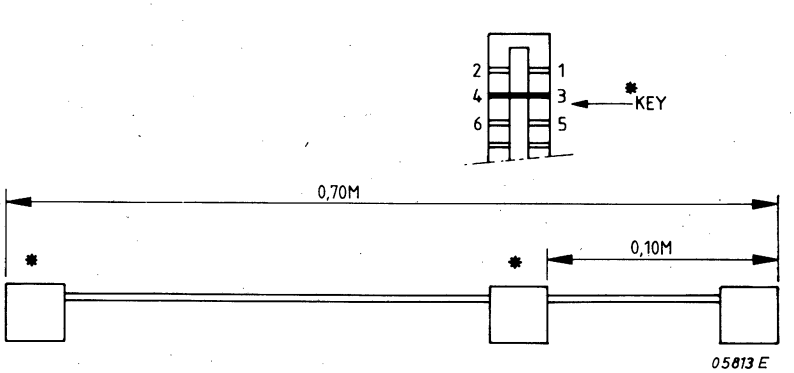
Figure 3.3.9 CABLES RAWIST (CONT'D)



M) CABLE DATA EXTENSION SEAGATE 5111-199-53890

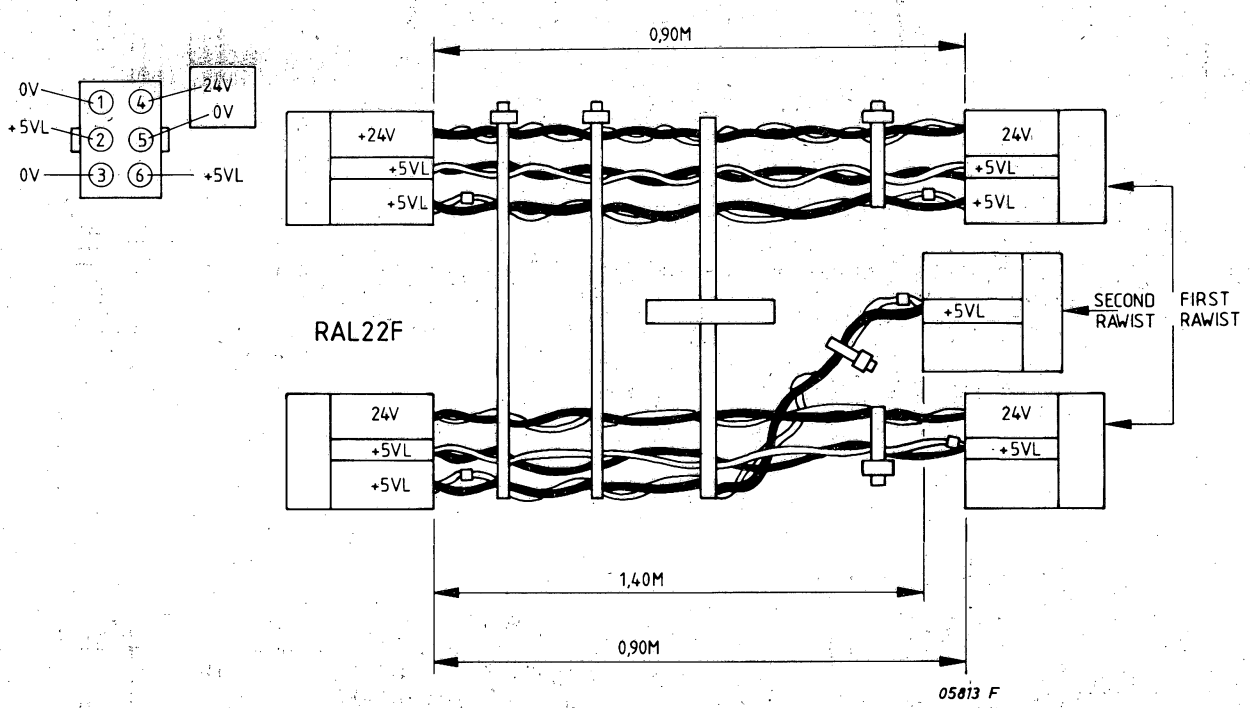


N) CABLE TEL/DC RA12F 5111-199-53910

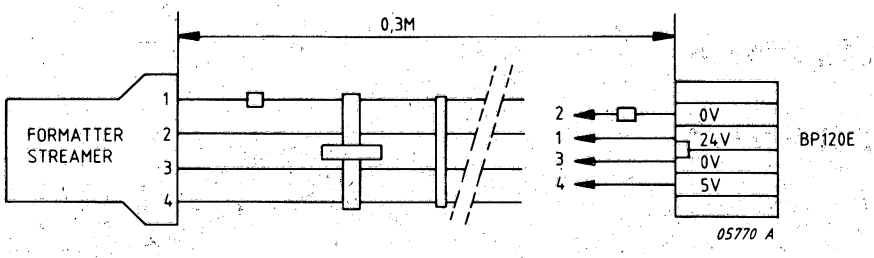


O) CABLE CONTROL SIGNALS SEAGATE 5111-199-53920

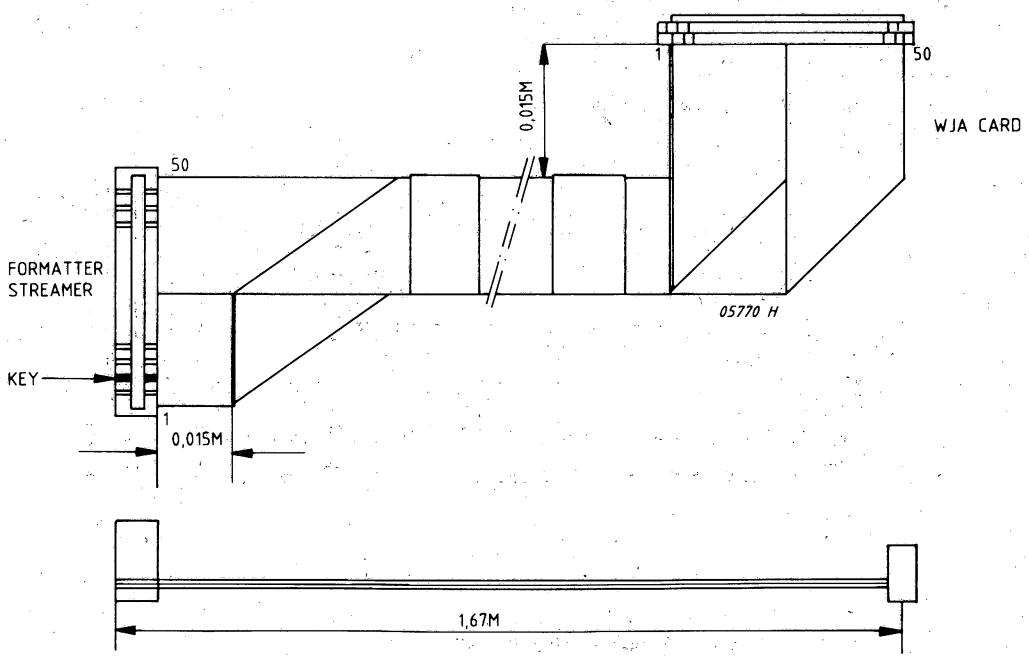
Figure 3.3.9 CABLES RAWIST (CONT'D)



P) CABLE TEL/DC RAL22F 5111-199-53930

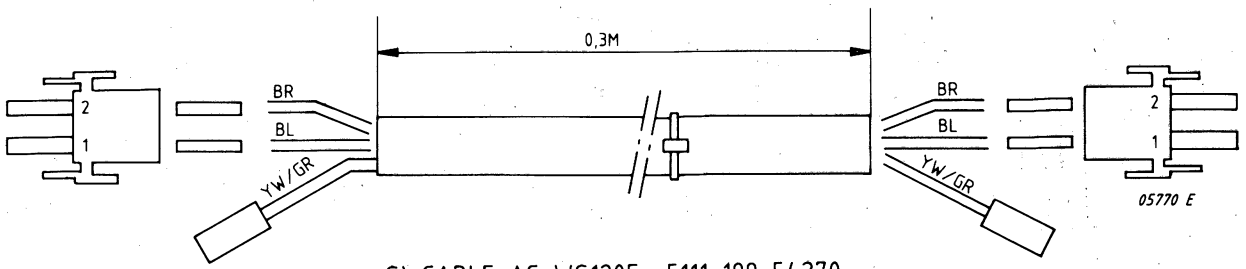


q) CABLE DC STREAMER 5111 199 54030

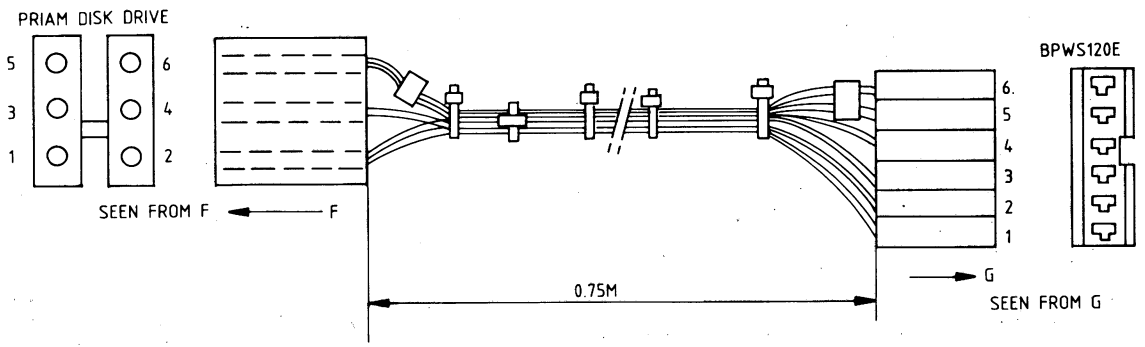


r) CABLE LOGIC STREAMER 5111 199 54040

Figure 3.3.9 CABLES RAWIST (CONT'D)



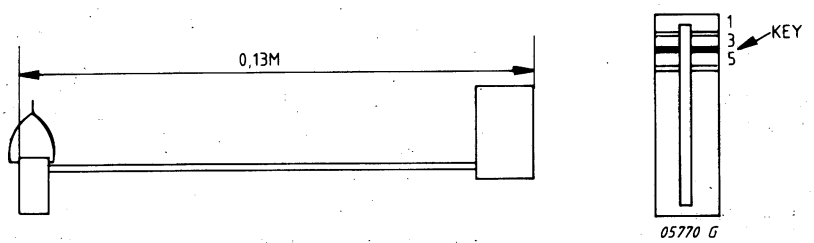
S) CABLE AC WS120E 5111 199 54270



COLOUR	CONNECT. AMP DRIVE	CONNECT. AMP BPWS120E	TENSION D.C.
BLA	1	2	0V
WHT	2	1	+24V
WHT	3	4	-5V
WHT	4	3	-12V
WHT	5	6	+5V
BLA	6	5	0V

05770 F

t) CABLE DC DISK-PRIAM 5111 199 54590



u) CABLE DATA SEAGATE 5111 199 56130

Figure 3.3.9 CABLES RAWIST (CONT'D)

3.3.7 DISTRIBUTION-BOARD (DISWST)

The DISWST is mounted to the ventilation unit.
It has the following functions:

- Remote Switch-On (relays K1, K2)
- AC distribution to FANS, WS120E and FLOPPY
- DC distribution

When the power is switched on by K1, the current is limited by resistor R1 till K2 is energised with the 5V from PSU WS120E.

The AC voltage to the FANS is selected with S01 and S02

220V mains - S01, S02 in upper position.
110V mains - S01, S02 in lower position.

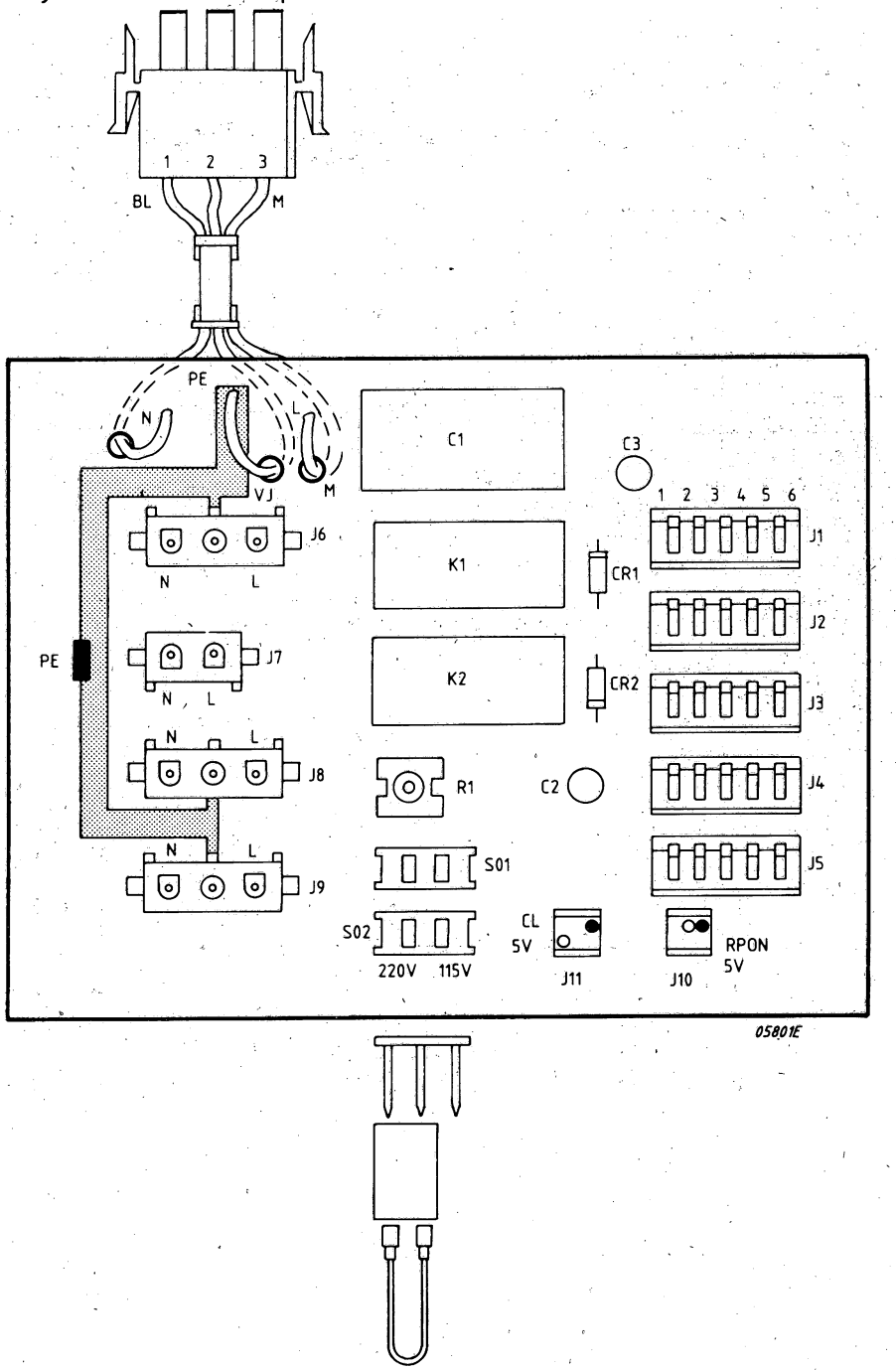


Figure 3.3.10a DISTRIBUTION-BOARD DISWST

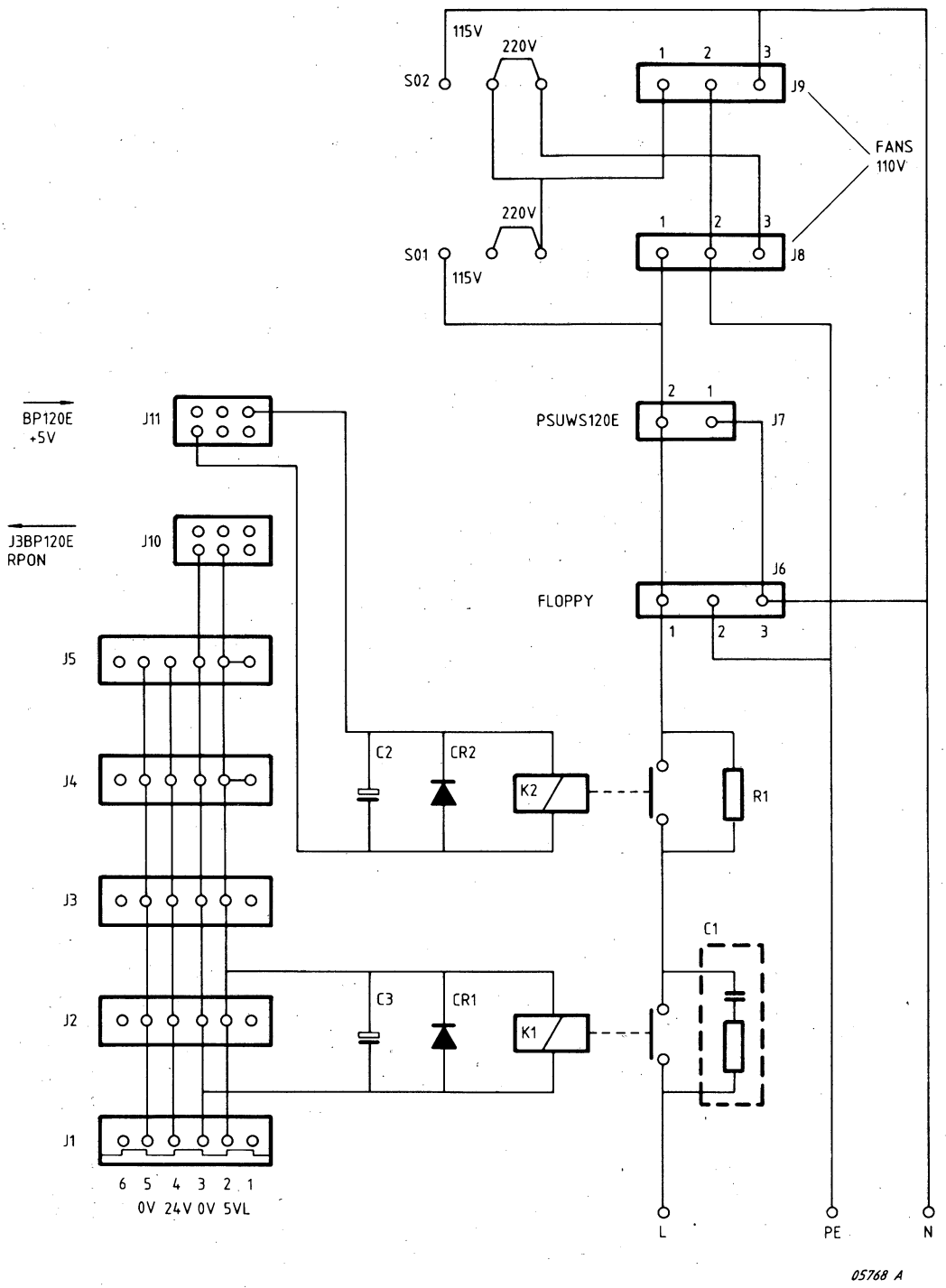


Figure 3.3.10b DISTRIBUTION-BOARD DISWST

3.3.8 PSU WS120E

Note: PSU WS120 is not compatible with WS120E.

TECHNICAL DATA PSU WS120E (5112 291 77780)

Input Voltage - Single phase alternating current
Rated Voltage - 100 - 127 VAC
200 - 240 VAC (repluggable)

Mains Frequency - 50Hz, 60Hz ± 2%

Switching Frequency - 20 KHz

Connection - 2 and 96 pole connector

Dimensions - 233.4 x 150 x 40 mm

Weight - 2.5 kg

DC outputs	Voltage Tolerance	I - rated	I - rated peak
+ 5V	± 3 %	12 Amp	
+ 12V	± 5 %	6	8 Amp
+ 24V	± 5 5	3	4.5 Amp
- 12V	± 5 %	0.8 Amp	1 Amp
- 5V	± 3 %	2 Amp	2.5 Amp

Table 3.3.2 ADMISSABLE LOAD WS120E

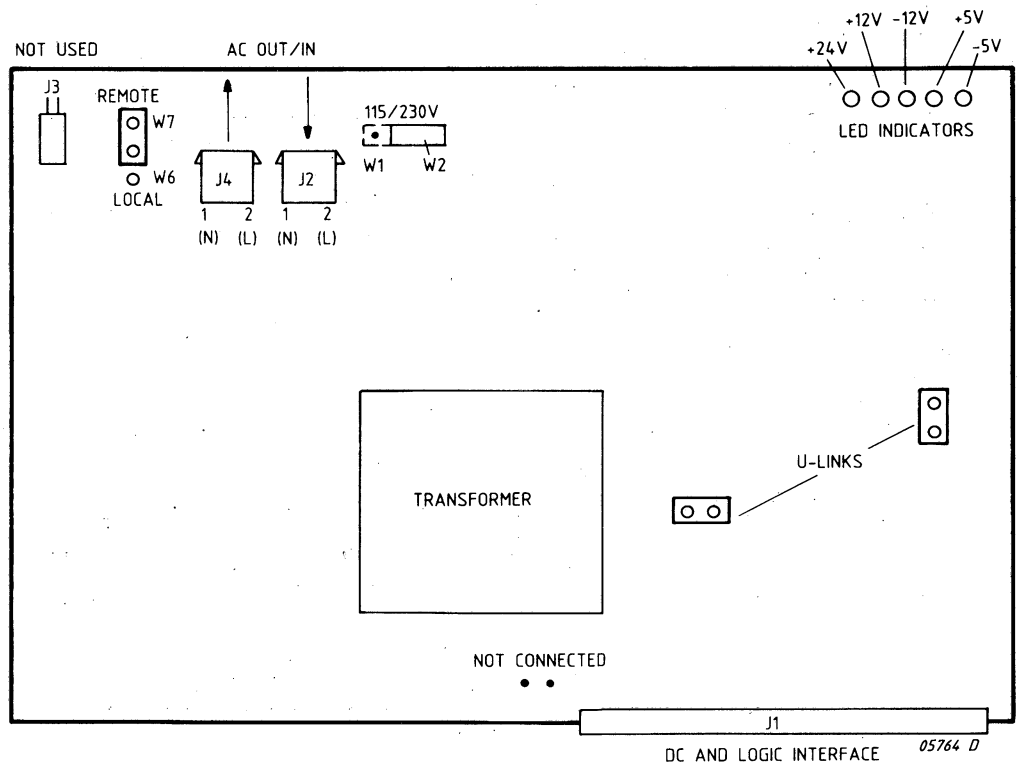
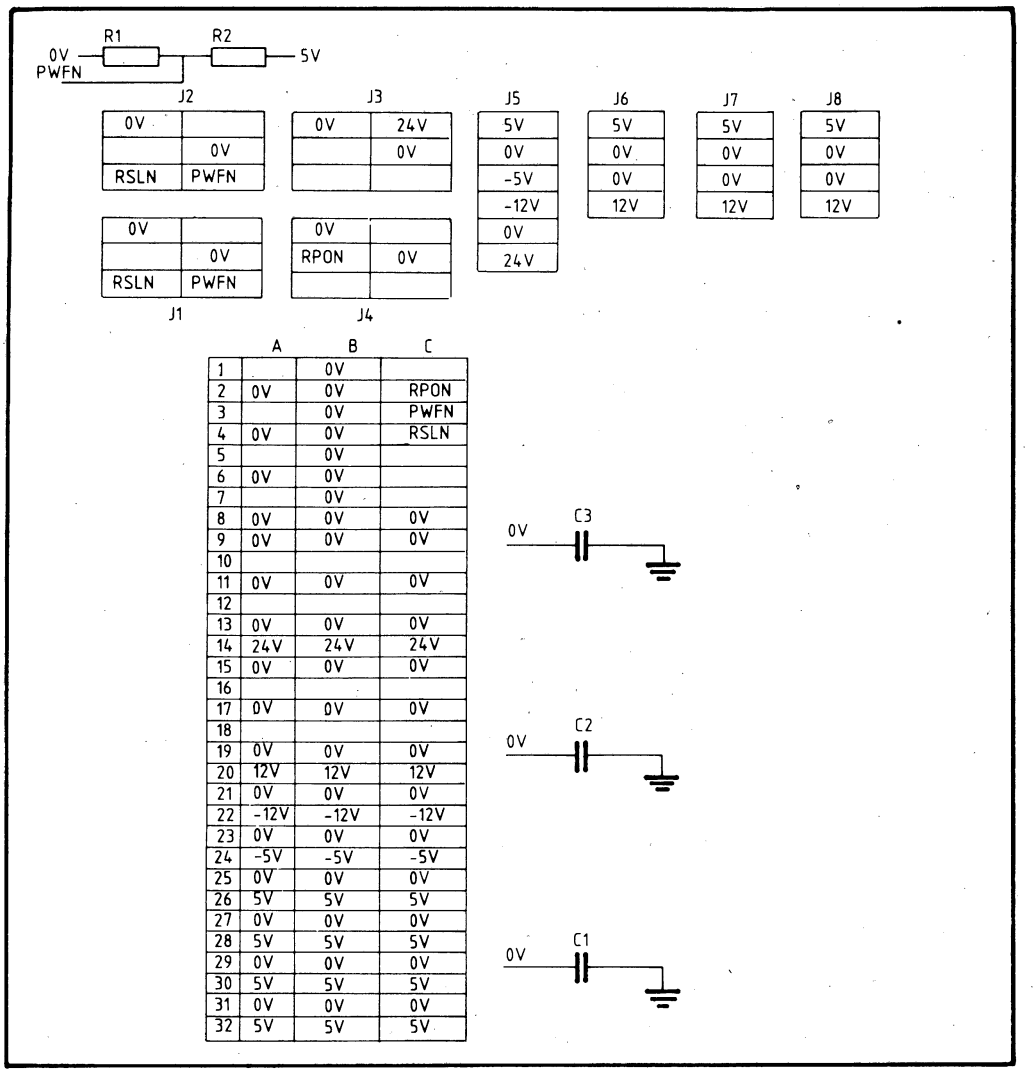


Figure 3.3.11 PSU WS120E



	A	B	C
1		0V	
2	0V	0V	RPON
3		0V	PWFN
4	0V	0V	RSLN
5		0V	
6	0V	0V	
7		0V	
8	0V	0V	0V
9	0V	0V	0V
10			
11	0V	0V	0V
12			
13	0V	0V	0V
14	24V	24V	24V
15	0V	0V	0V
16			
17	0V	0V	0V
18			
19	0V	0V	0V
20	12V	12V	12V
21	0V	0V	0V
22	-12V	-12V	-12V
23	0V	0V	0V
24	-5V	-5V	-5V
25	0V	0V	0V
26	5V	5V	5V
27	0V	0V	0V
28	5V	5V	5V
29	0V	0V	0V
30	5V	5V	5V
31	0V	0V	0V
32	5V	5V	5V

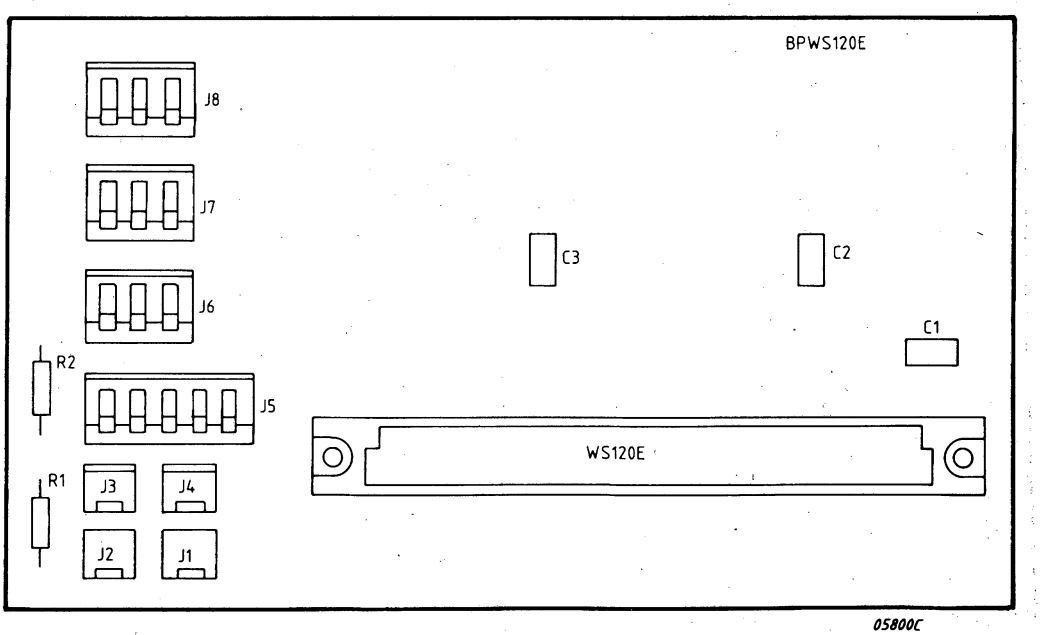


Figure 3.3.12 BACK PANEL WS120E

3.3.9 COMPACT FIXED DISC (PRIAM)

3.3.9.1 IDENTIFICATIONS

Type No.: P829-002

Also called: Winchester disc or Hard Disc Drive (HDD)

Type:	P829-002 PRIAM 3450
Capacity unformatted formatted	 35 Mb 25.5 Mb
Disc size	8 inch
No. of discs No. of data surfaces No. of servo surfaces	3 5 1
Recording method No. of cylinderrs	MFM 525
User cyl.: Alternate:	0-509 510-524
No. of sectors/track for use : Physical:	 39 40
No.of bytes/sector Rotational speed Max. recording density Average access time Start up time	256 3600 rpm 6670 bpi 50 ms 30 sec.
Power consumption	+ 24V 3.5A + 5V 3.2A

Warning . Damage to the disc surface may occur if the heads are moved across a non-rotating disc surface. . Avoid manual rotating of the spindle or movement of the carriage.

Notes: Later drive types have auto-lock. For older versions, spindle and carriage movement had to be locked manually before transport.
Only the last drive in the daisy chain cable connection must contain a terminator.

3.3.9.2 UNPACKING AND HANDLING

Inspect the exterior of the shipping container for obvious signs of shipping damage. If there are indications that the container is damaged, NOTIFY THE CARRIER AT ONCE.

If no damage is apparent, open the container and remove disc drive and documentation. Store documentation. Store packing material for further use.

UNLOCKING

Both the spindle and the head carriage assembly are locked prior to shipment. After the drive has been completely mounted and cabled, these must be unlocked to enable normal operation.

The drive spindle and head carriage lock is fully accessible from one end of the HDA (Head Disc Assembly). Place this lever in the UNLOCK position.

> CAUTION: AVOID MANUAL ROTATION OF THE SPINDLE OR MOVEMENT OF THE CARRIAGE.
>
> DAMAGE TO THE DISC SURFACE MAY OCCUR IF THE HEADS ARE MOVED ACROSS A NON-ROTATING DISC SURFACE.
> THEREFORE MAKE SURE THAT THE DRIVE IS LOCKED OR POWER IS APPLIED TO THE DISC DRIVE WHEN MOVING THE CABINET TO THE FINAL POSITION. IN ANY CASE, TAKE GREAT CARE OF THE DISC DRIVE BECAUSE IT IS CARRYING VITAL DATA.

LOCKING

The drive spindle and the head carriage should be locked whenever the drive is to be physically moved, even if it is not to be shipped. To lock the drive place the lever in the LOCK POSITION.

REPACKING

Repacking is the reverse of the unpacking procedure. Prior to repacking the drive, make sure that the spindle and carriage lock lever is in the LOCK position.

STORAGE

When the environment is severe, or when the drive is to be stored for a long time, it should be repacked prior to storage.

SHIPPING

After locking the drive spindle and head carriage, pack the drive in its original carton or equivalent one.

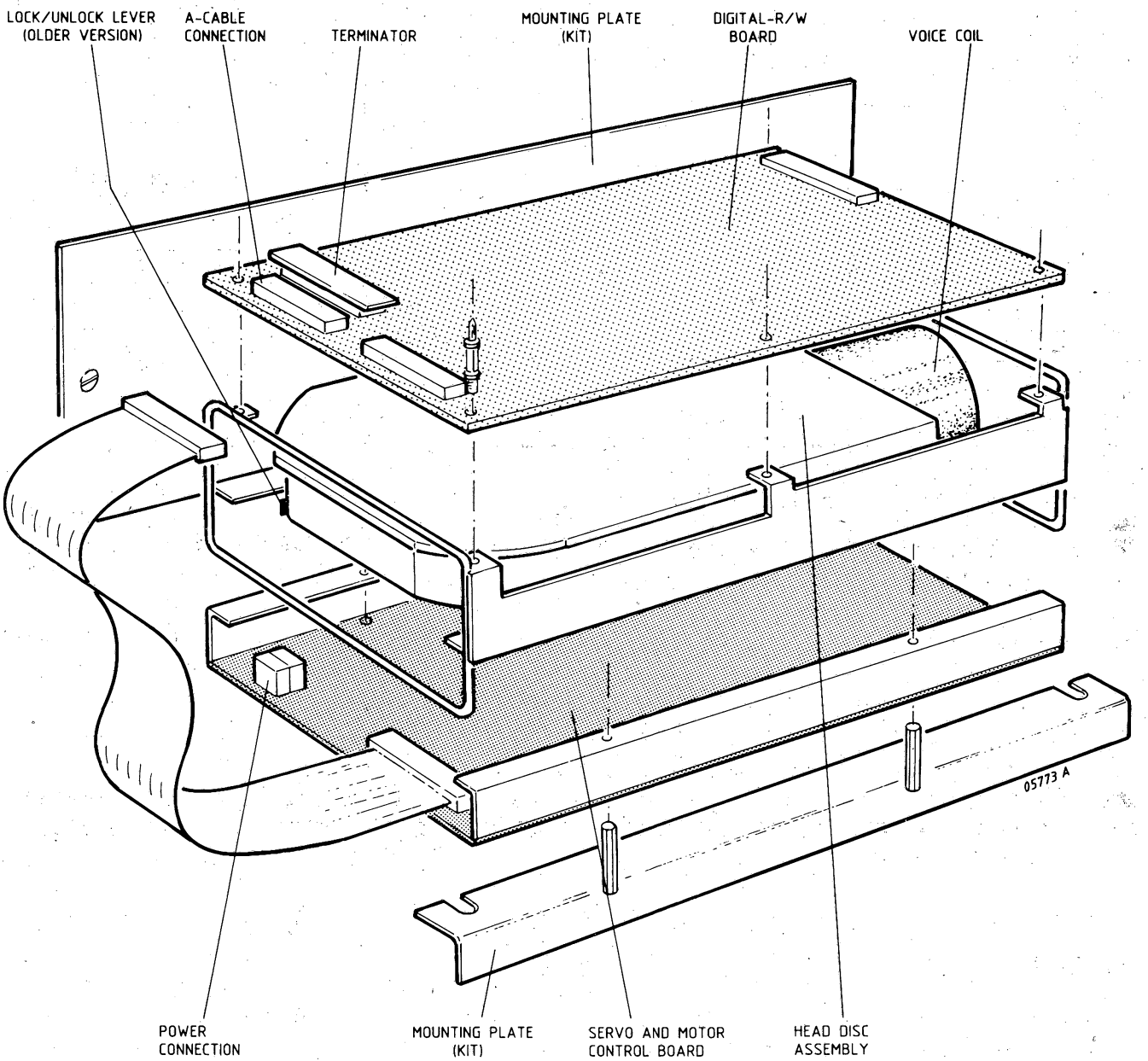
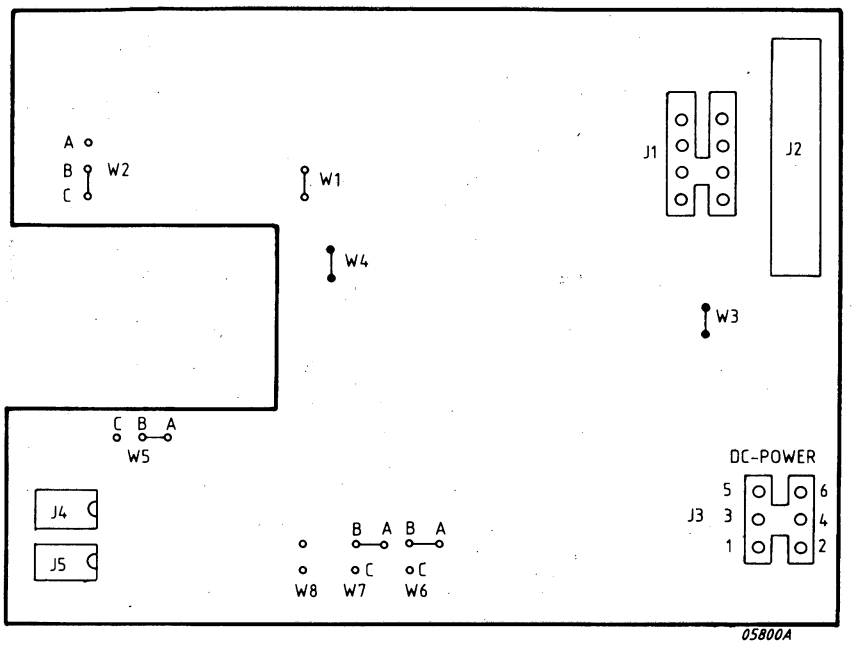


Figure 3.3.13 DISC DRIVE PRIAM

PART NO 200505-2



JUMPER	AUTOLOCK UNIT
W1	IN
W2	BC
W3	IN
W4	IN
W5	AB
W6	AB
W7	AB
W8	--

-- MEANS: JUMPER OUT

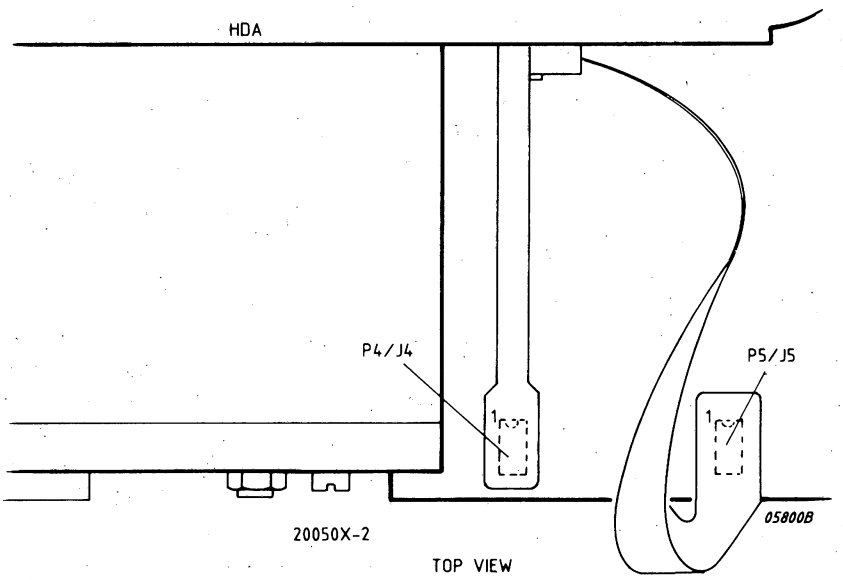
DC VOLTAGES	
J3 -1	0V
-2	+24V
-3	-5V
-4	-12V
-5	+5V
-6	0V

Figure 3.3.14 SERVO MOTOR CONTROL PCB FOR 3450 AND 7050

INSTRUCTIONS FOR CONNECTING P4 AND P5 TO
THEIR RESPECTIVE CONNECTORS J4 AND J5

1 CONNECT P4 (FROM HDA) TO J4 (ON 20050X-2) SUCH THAT THE
NOTCH ON P4 ALIGNS WITH THE NOTCH ON J4
THIS INSURES THAT P4 PIN 1 CONNECTS TO J4 PIN 1.

2 CONNECT P5 (FROM HDA) TO J5 (ON 20050X-02) SUCH THAT THE
NOTCH ON P5 ALIGNS WITH THE NOTCH ON J5
THIS INSURES THAT P5 PIN 1 CONNECTS TO J5 PIN 1.



PROPER CONNECTION OF HDA FLEX CABLE PLUGS P4 AND P5
INTO CONNECTORS J4 AND J5 ON SERVO/MOTOR
CONTROL PCB 20050X-2

Figure 3.3.15 HEAD DISC ASSY CONNECTIONS

part no. 200233-21 for 3450
200233-22 for 7050
(the main different between the two pcb's is the PROM contents, location 9H.)

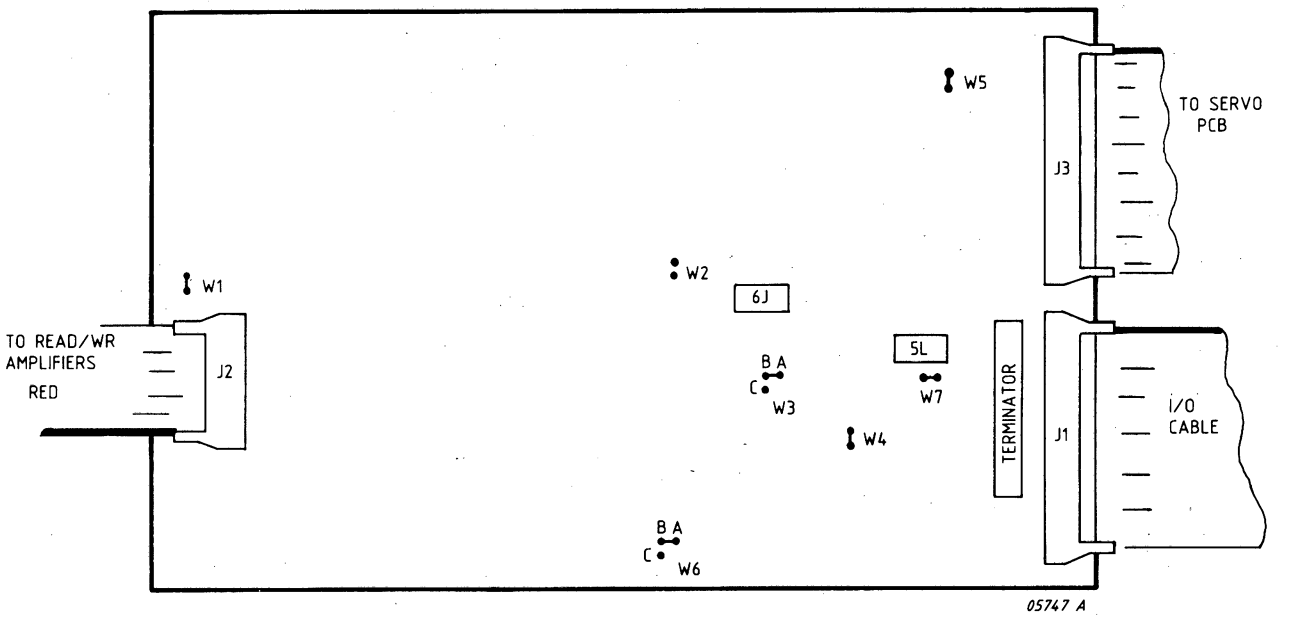


Figure 3.3.16 WRITE AND DIGITAL PCB FOR 3450 AND 7050

Note: TERMINATOR only on last drive in daisy chain.

	3450 (35Mb)	7050 (70Mb)
W1	IN	OUT
W5	IN	OUT
W2	OUT (= short reset)	
W3	AB (skip defect rec; AB=prot.)	
W4	IN (ready dependant on busy)	
W6	AB	
W7	IN (=write clk from CU)	

PROM 9 H	
3450	7050
300275 EC2004	300276 EC2004

switches 6J:

Switch	1	2	3	4	5	6	7	8
setting	up	dn	dn	up	dn	up	dn	dn
sectors per track	1	2	4	8	16	32	64	128

example: 41 sectors/track

switches 5L:

switch	1	2	3	4	5	6	7	8
setting: drive 0	up	dn	dn	dn	x	x	x	up
1	dn	up	dn	dn	x	x	x	up
2	dn	dn	up	dn	x	x	x	up
3	dn	dn	dn	up	x	x	x	up
function	drive no.				none			write enable

Note: up/dn means 'where pushed'
or 'moved to' depending of the used
DIP-switch type.

Table 3.3.3 STRAP SETTING PRIAM DISC DRIVE

3.3.10 CONTROL UNIT 'XEBEC'

3.3.10.1 IDENTIFICATIONS

The 'XEBEC' Control Unit converts WDD commands according 'Small Computer System Interface' (SCSI) into Seagate disc interface 'ST506'.

The 'XEBEC'-CU is mounted on the Seagate hard disc drive and included in the product No. 'PTS 6794 Hard Disc Drive'.
Features:

- Full-sector buffer
- Hardware 32-bit ECC polynomial with 11-bit burst error correction
- Software selectable automatic retries during disc access (4 times)
- Internal diagnostics
- Separate Identifier (ID) and data fields with an ECC each
- High level command set
- Variable interleave
- Optimal interleave (=skip) factor is 4
- A full track can be read/written in 4 revolutions
- Sector '0' is positioned after track index
- The drive recording method is MFM.

The format for a Seagate ST412 disc:

capacity	10 Mbytes
sector/track	32 (always) of 256 bytes/sector
No. of cylinders	*306 (=No. of track sets)
No. of heads/surface	1
No. of data surfaces	4
fastest step rate code	6
No. of alternates	6 (recommended)

* It is possible to use less cylinders, e.g. for dimming reasons.

- Track Assignment:

  Primary tracks on cyl. 0 through 298
  Alternate tracks on cyl. 299, 300, 301, 302, 303, 304
  Service track on cyl. 305
  Note: The service track has no alternate facility, but there will be at least one error-free sector.
  Sector lay-out is determined by the 'XEBEC'-CU and cannot be influenced by the WDD. Identifiers cannot be read by the WDD.

- Sector Position Calculation:

  RSN = NOH * NOS * TSNR + NOS * HDNR + SCNR

  where: RSN = Real Sector Number
  NON = Number Of Heads (No. of tracks/cyl.)=4
  NOS = Number Of Sectors/track=32
  TSNR = Track Set Number (=cyl. No.)
  HDNR = Head Number
  SCNR = Sector Number within track

Power Consumption: +5V 2.0A (2.5A max.), +12V 48mA (66mA max.).

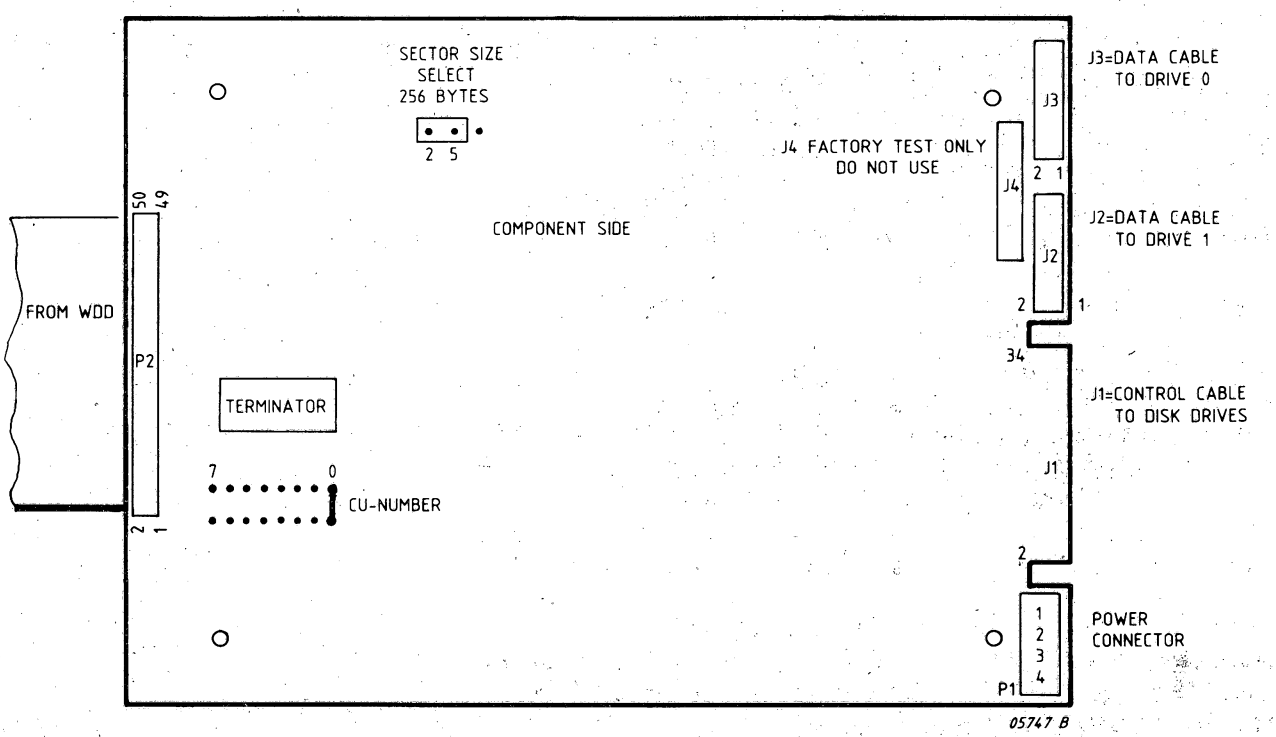


Figure 3.3.17 XEBEC CONTROL-UNIT

3.3.10.3 INTERFACE XEBEC

P1 - pin 1 = +12V
pin 2 = 0V
pin 3 = 0V
pin 4 = +5VL (from system rack)

P2 - WDD CU interface (see Chapter WDD)

J1 - CONTROL CABLE DAISY CHAIN (2 drives)

J2, J3 - DATA CABLE for each drive.

3.3.11 HARD DISC DRIVE SEAGATE

3.3.11.1 IDENTIFICATIONS

Type NO.: P829-006 SEAGATE Hard Disc drive, model ST-412 (Winchester disc)

Technical Summary:

- technology	Winchester
- capacity unformatted	12.76 Mbytes
- capacity formatted	10.0 Mbytes
- disc size	5.25 inch
- number of discs	2
- number of heads	4
- track density	345 tpi
- No. of sectors/track	32
- No. of bytes/sector	256
- No. of cylinders	306
- rotational speed	3600 rpm
- recording density	9074 bpi max
- average access time	85 ms
- transfer rate	5 Mbits/sec
- access time average/max	85 / 205 msec
- single track seek/settle	16.67 msec max.

Power Consumption:

+12V 1.8A during running
5.4A max (start up)

+5V 1.0A
1.7A max.

Unpacking

WARNING : - DO NOT ROTATE THE SPINDLE MOTOR

- DO NOT ROTATE THE STEPPER MOTOR

- DRIVE CAN EASILY BY DAMAGED BY MECHANICAL SHOCKS

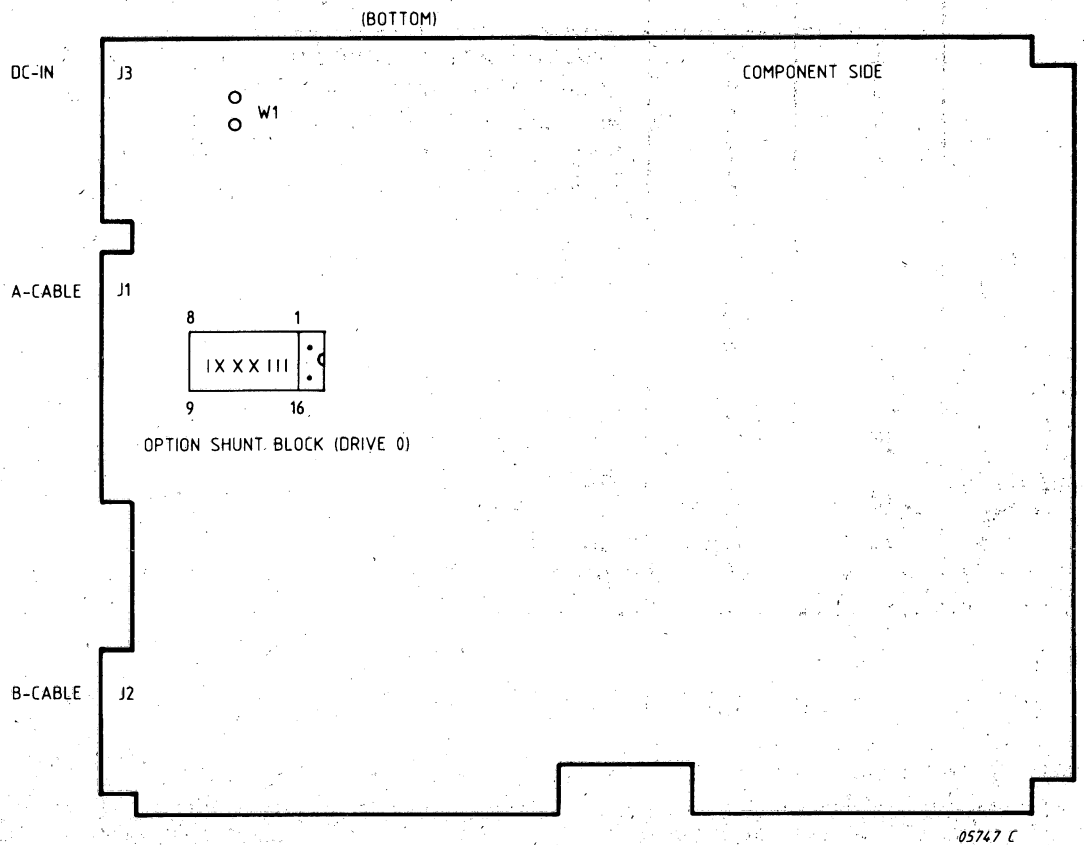
- COVER OF DUSTFREE AREA MAY NOT BE REMOVED (repair in NO-workshop not allowed!)

- TRANSPORT: only either in RAWIST or in special single unit package.

Note: Start up / power on and power off are controlled by software.

TRANSPORT: To prevent damage on track '0', the heads must e moved by program from this track.
The DC plug must be disconnected after power off.

3.3.11.2 INSTALLATION SEAGATE



NOTES:

- W1 NORMALLY OPENED (CONTINUOUS SEEKING IF CLOSED)
- OPTION SHUNT BLOCK:

1 - 16 N.C. (CONTINUOUSLY SELECTED IF CLOSED)
2 - 15 } NOT USED,(CLOSED)
3 - 14 }
4 - 13 }
5 - 12 DRIVE SELECT DS4
6 - 11 DRIVE SELECT DS3
7 - 10 DRIVE SELECT DS2
8 - 9 DRIVE SELECT DS1

DRIVE 0	1	2	3
X	X	X	–
X	X	–	X
X	–	X	X
–	X	X	X

(– = CLOSED, X= OPEN)

Figure 3.3.18 MAIN CONTROL PCB OF SEAGATE DISC

3.3.11.3 INTERFACE SEAGATE

GROUND RETURN	SIGNAL PIN	SIGNAL NAME
1	2	Reduced Write Current
3	4	Head Select 2^2
5	6	Write Select Gate
7	8	Seek Complete
9	10	Track 00
11	12	Write Fault
13	14	Head Select 2^0
15	16	Reserved
17	18	Head Select 2^1
19	20	Index
21	22	Ready
23	24	Step
25	26	Drive Select 1
27	28	Drive Select 2
29	30	Reserved
31	32	Reserved
33	34	Direction in

Table 3.3.4 J1 CONTROL SIGNALS SEAGATE

1	Drive Selected	2	0V
3	Spare	4	0V
5	Spare	6	0V
7	Reserved	8	0V
9	Spare	10	Spare
11	0V	12	0V
13	MFM Write Data +	14	MFM Write Data -
15	0V	16	0V
17	MFM Read Data +	18	MFM Read Data -
19	0V	20	0V

Table 3.3.5 J2 DATA SIGNALS SEAGATE

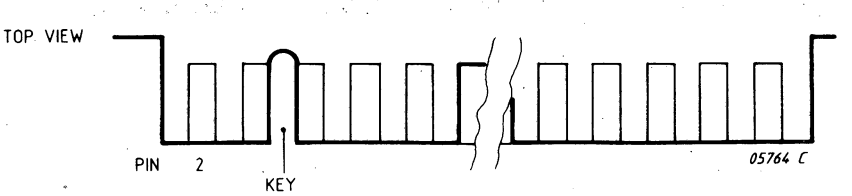


Figure 3.3.19 CONNECTORS J1/J2

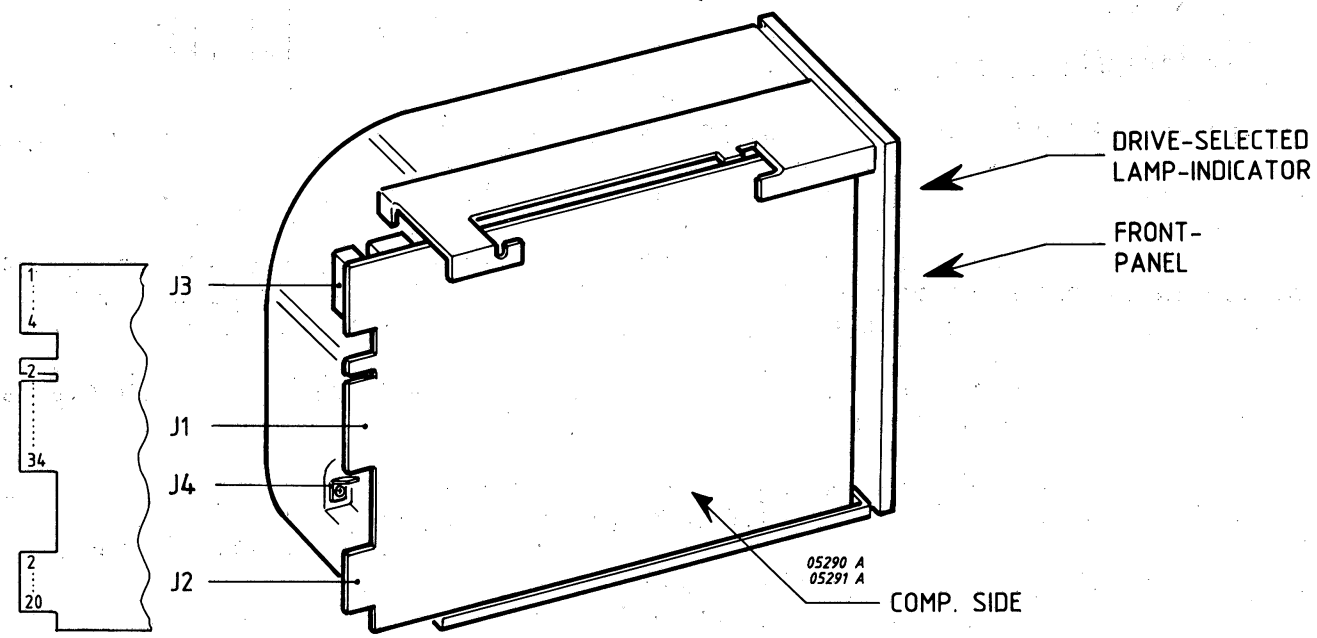


Figure 3.3.20 DISC DRIVE SEAGATE

PIN	USE
1	+ 12 Volt
2	+ 12 Volt Return
3	+ 5 Volt Return
4	+ 5 Volt

Table 3.3.6 POWER CONNECTIONS J3 SEAGATE

J4: FASTON connection for earth cable

3.3.12 STREAMER TAPE DRIVE 9020I

3.3.12.1 IDENTIFICATIONS

- Type No: P829-010 ARCHIVE SIDEWINDER 9020I (20MB)

- Features

The drive is designed to write/read data in a streaming mode without frequent stops. A formatter is mounted in the rack RAWIST. This means that to and from the CU only data is sent, the formatter acts as a big first out memory.

Also recovery during read and write is performed by the formatter. This includes read after write, rewrite, reread.

Care must be taken to the fact that the performance (read and write times) is directly correlated with the availability of data from the control unit.
With a data block length of 10M the time for a whole cartridge will be 2 minutes with 64 K:5 min., with 32 K:8 min, with 16 K:15 min., etc.

The control unit uses no data buffer.

Hardware error recovery is done by the formatter.

Model	9020I
No. of Tracks	4
No. of Heads	2
Formatted Capacity	20 MB
Unformatted Capacity	21.6 MB
Dump Time	4 Min.
Recording Mode	NRZI
Recording Density	8K BPI
Flux Density	10K FCI
Track Capacity	5.2 MB
Tape Speed	90 IPS
Start/Stop Time	300 MS

Table 3.3.7 SIDEWINDER PERFORMANCE (STREAMER)

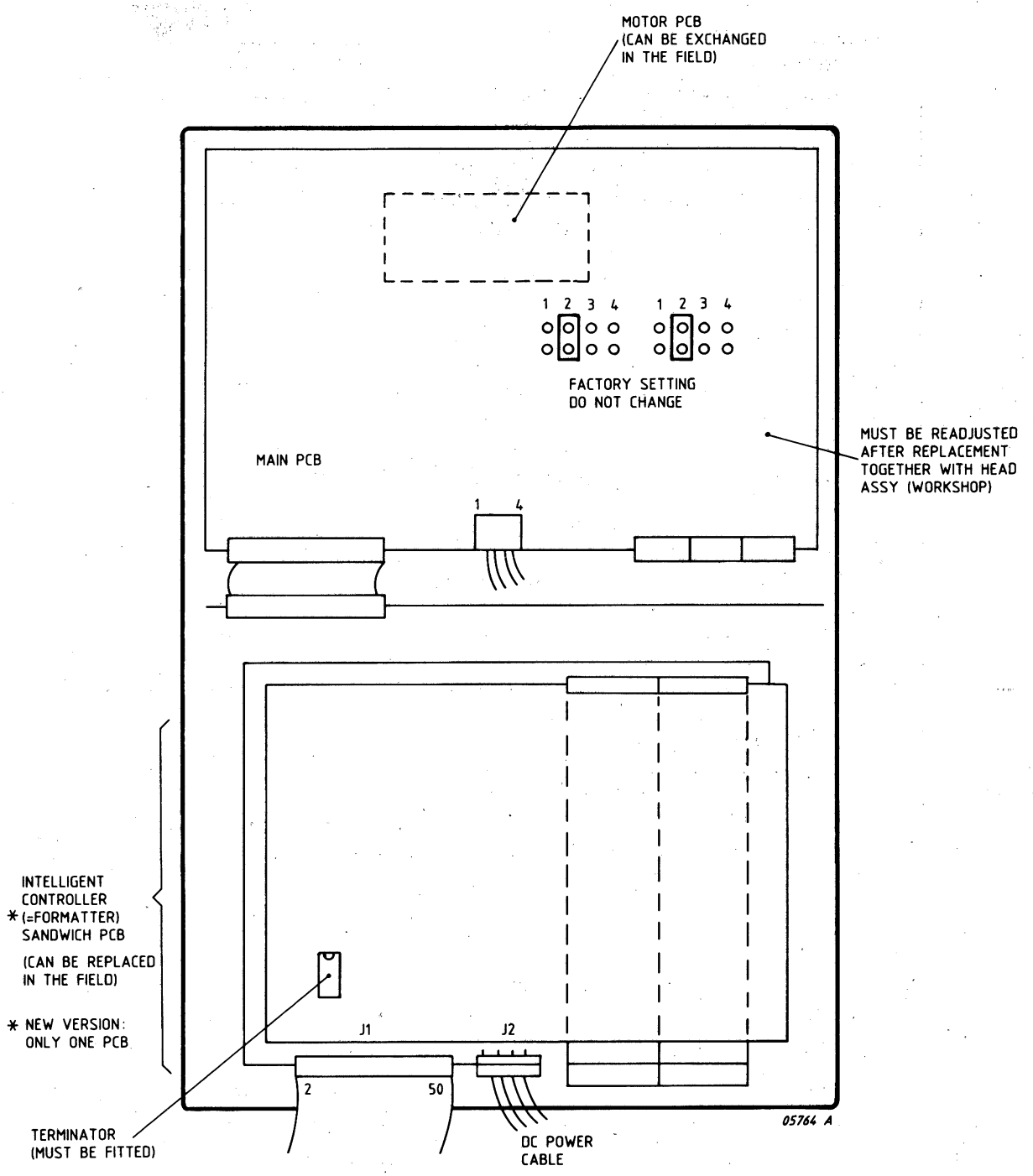


Figure 3.3.21 TAPE DRIVE AND FORMATTER

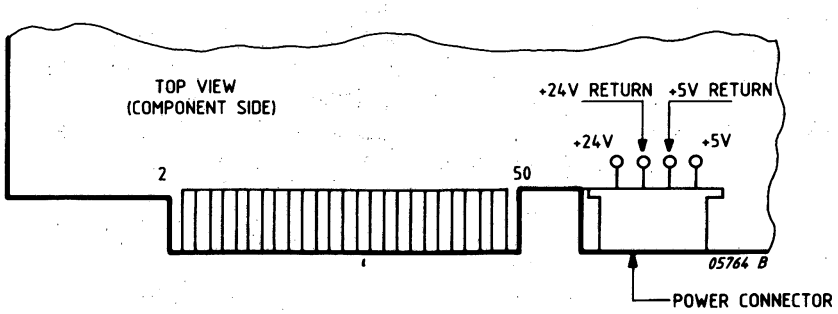


Figure 3.3.22 CONNECTORS J1/J2 FORMATTER/DRIVE

3.3.12.3 PERFORMANCE DATA

Voltage	Inteligent Drive (Drive and Formatter)
+24 VDC	+24 ± 10% vdc Standby; 0.2 amp Operating; 0.8 amp - max. 1.7 amps - surge, 2.5 amps
+5 VDC	+5 ± 5% vdc Standby; 3.5 amps Operating; 3.5 amps
Power Dissipation	35 Watts, typical 60 Watts, maximum
Basic Drive: Depth Width Height Weight	152.4 ± 0.51 mm 196.9 ± 0.51 mm 114.3 ± 0, -5.1 0.95 ± 0.05 kg
	Operational / Non-Operational
Temperature	+5 to +45°C / -30 to +60°C

Table 3.3.8 PERFORMANCE DATA STREAMER

3.3.12.4 DATA BUS COMMANDS

Command	Result
Select	Selects Basic Drive to be used.
Position	Causes tape to be moved to BOT, erased, or retensioned.
Write Data	Write data onto tape.
Write File Mark	Write File Mark at the end of last data block.
Read Data	Read data from tape and transfer it.
Read File Mark	Move the tape to the next File Mark without transferring data.
Read Status	Transfer six bytes of status and statistics.

Table 3.3.9 COMMANDS FORMATTER-STREAMER

3.3.12.5 SOFT ERROR STATISTICS

Read and write error statistics are available to the host through the Read Status command. Typically, the Read Status command should be requested after completion of each cartridge used and the statistics reported at least on an exception basis. An increase in the soft write error rate normally indicates a deterioration of the recording media. If retensioning the cartridge does not reduce the soft errors dramatically, a known good tape should be used. If the soft error rate is high on a known good tape, the drive is ready for servicing. If the soft write error rate is low on a known good tape, the cartridge with the high soft write error rate should be replaced with a new cartridge.

3.3.12.6 PREVENTIVE MAINTENANCE

CLEANING

Clean the read/write/erase head assembly and the tape hole detector openings with a clean, lintless cotton swab dampended with IBM head cleaning solution or 95% isopropyl alcolhol using the following schedule:

1. After an intial pass with a new tape cartridge or, if using all new tape cartridges, after every 2 hours of actual use.
2. After every 8 hours of normal use.

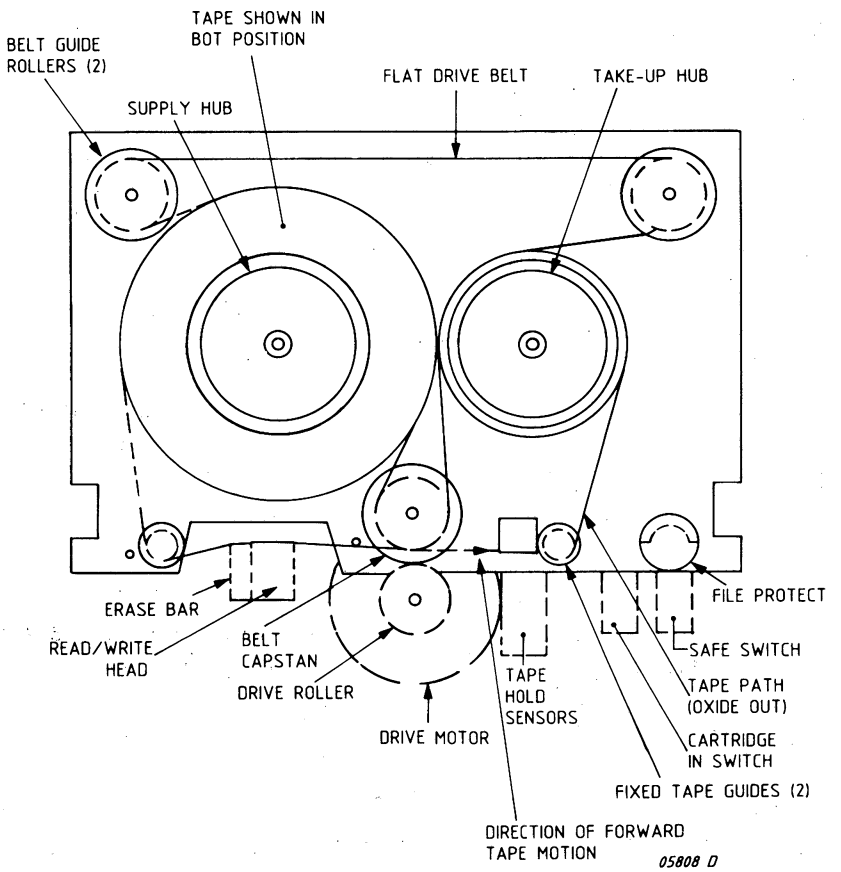


Figure 3.3.23 STREAMER TAPE

3.4 FLOPPY DISC RACK P830-010

3.4.1 IDENTIFICATIONS

RACK:
P830-010/11 Equipment shelf for 2 x FDD - 5111 199 60860

DRIVE-0.25Mb, CDC 9404:
P830-015/01 FDD-0.25Mb with door-lock - 5111 010 03910

DRIVES-1.Mb, CDC 9406:
P830-035/01 FDD-1Mb with door-lock 220V, 50Hz - 5111 010 04770

P830-035/02 FDD-1Mb with door-lock 110V, 60Hz - 5111 010 08830

Power Consumption:
- RACK: 220V-0.7A/240V-0.65A/115V-1.35A

- Drives:

9404	9406
220V-0.5A	110V-1,0A 220V-0.5A
+ 5V-0.8A +24V-1.3A	+ 5V-1.1A +24V-1.4A

Table 3.4.1 POWER CONSUMPTION FLOPPY DRIVES

3.4.2 GENERAL DESCRIPTION

The P830-010 FLOPPY-RACK can be used for installation of max. 2 drives: P830-015/035.

Max. 4 drives P830-015 or 2 drives P830-035 can be connected to the F1MZA control unit.

3.4.3 FUNCTIONAL DESCRIPTION

The FLOPPY RACK is equipped with the necessary power-supply and AC/DC wiring, which is described in the figures of this section. For logic cables refer to description in F1MZA chapter.

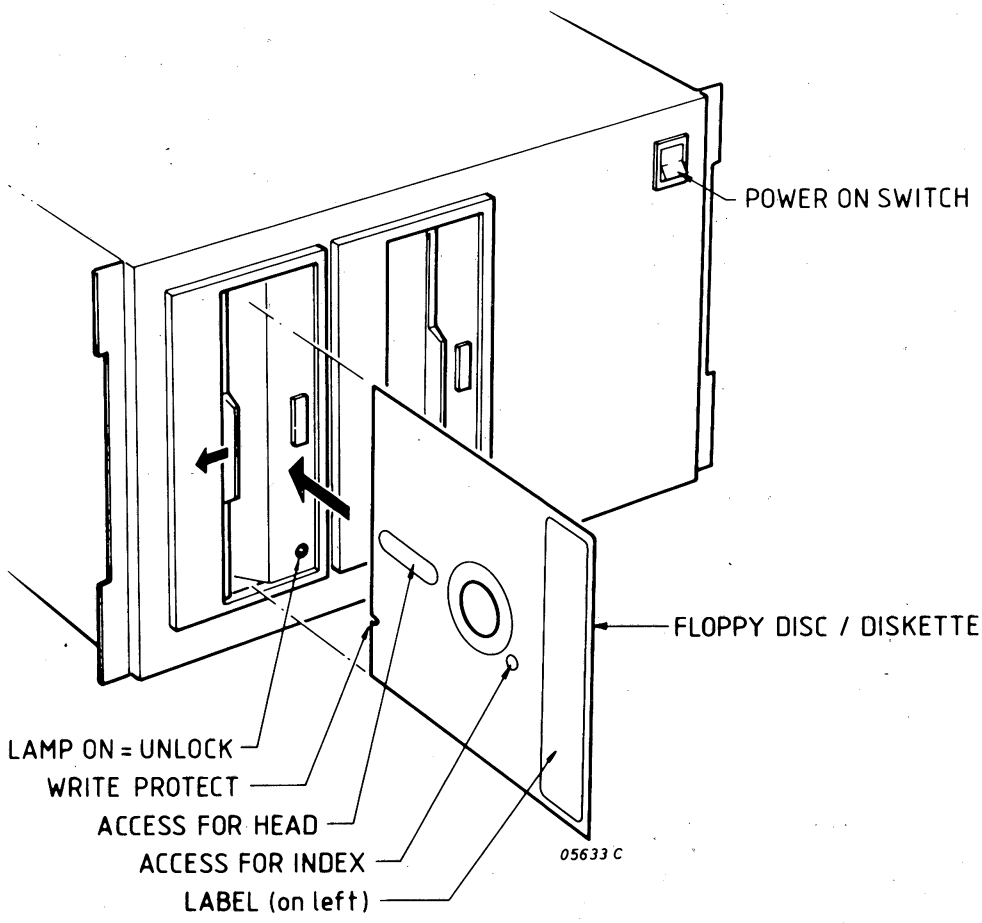


Figure 3.4.1 FLOPPY-DISC RACK (FRONT VIEW) P830-010

WARNING:
1. Never switch off power with a discette inserted
2. Only insert a discette if the spindle is rotating

3.4.4. INSTALLATION

The FLOPPY RACK is shipped without FLOPPY drives. The FLOPPY drives can be mounted after removing the front cover of the rack and are fixed with 2 screws on the top.
The cable from the F1MZA CU is mechanically secured at the rear of the rack.
The rack is fixed to the cabinet with 4 screws at the front.

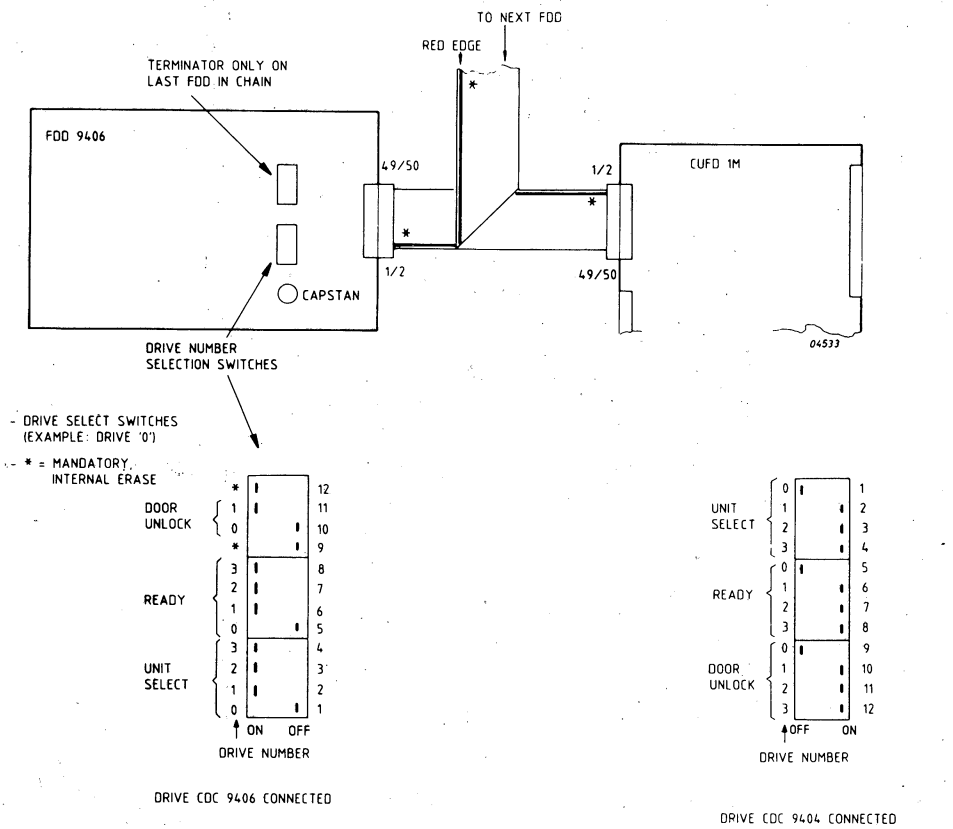


Figure 3.4.2 CONTROL UNIT CONNECTION WITH DRIVES 9404/9406

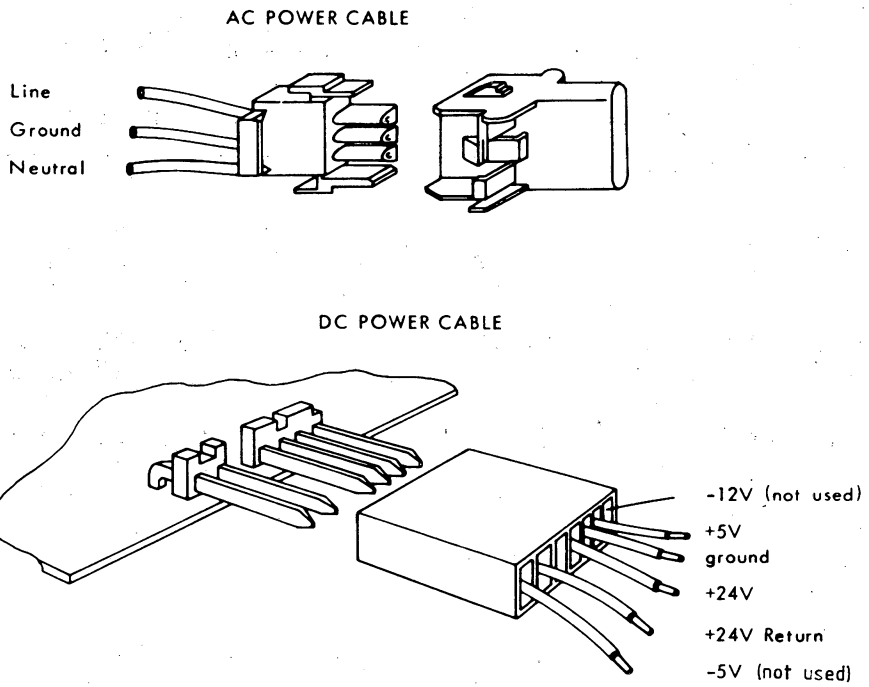


Figure 3.4.3 POWER CABLES AC/DC FLOPPY

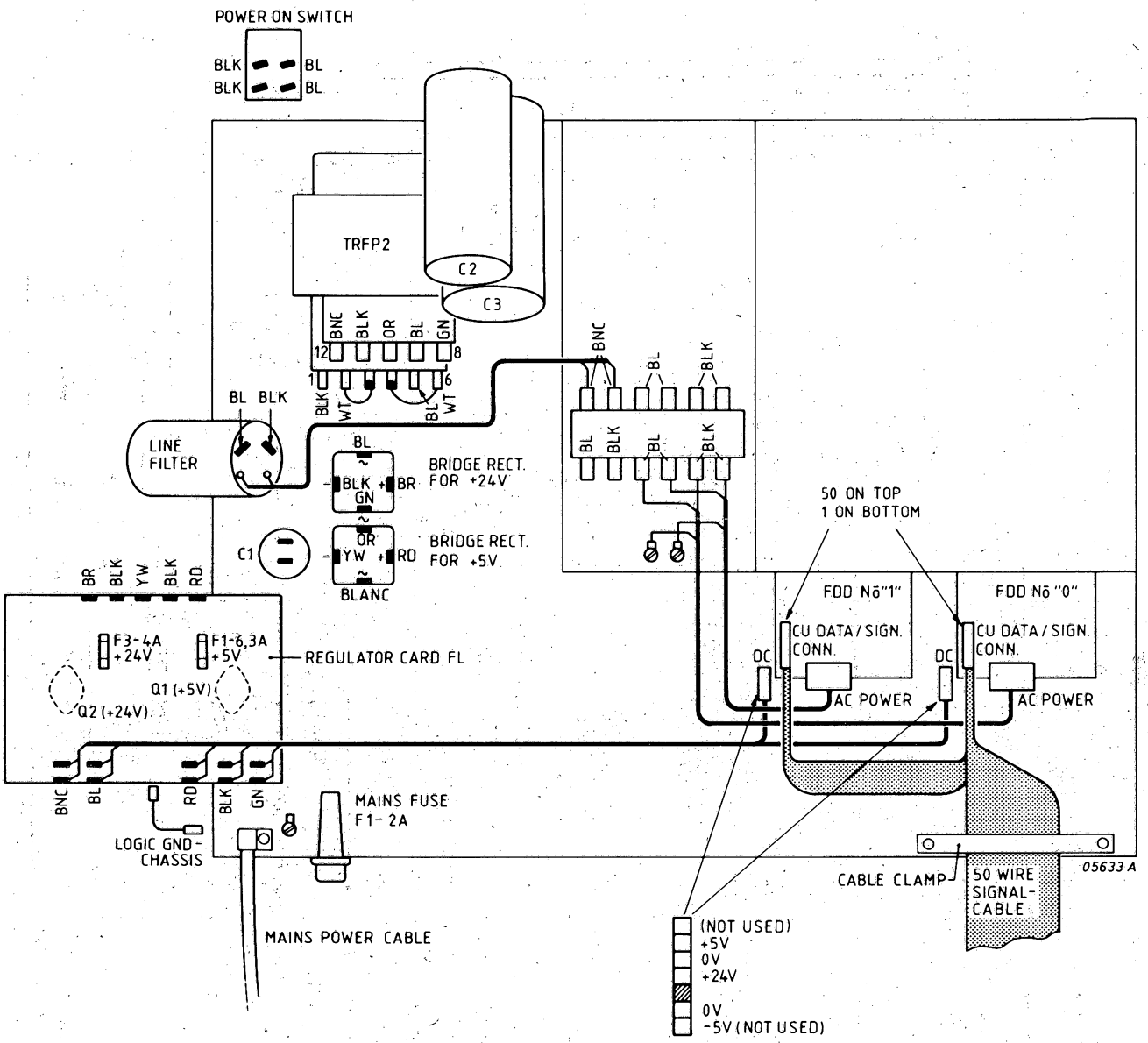
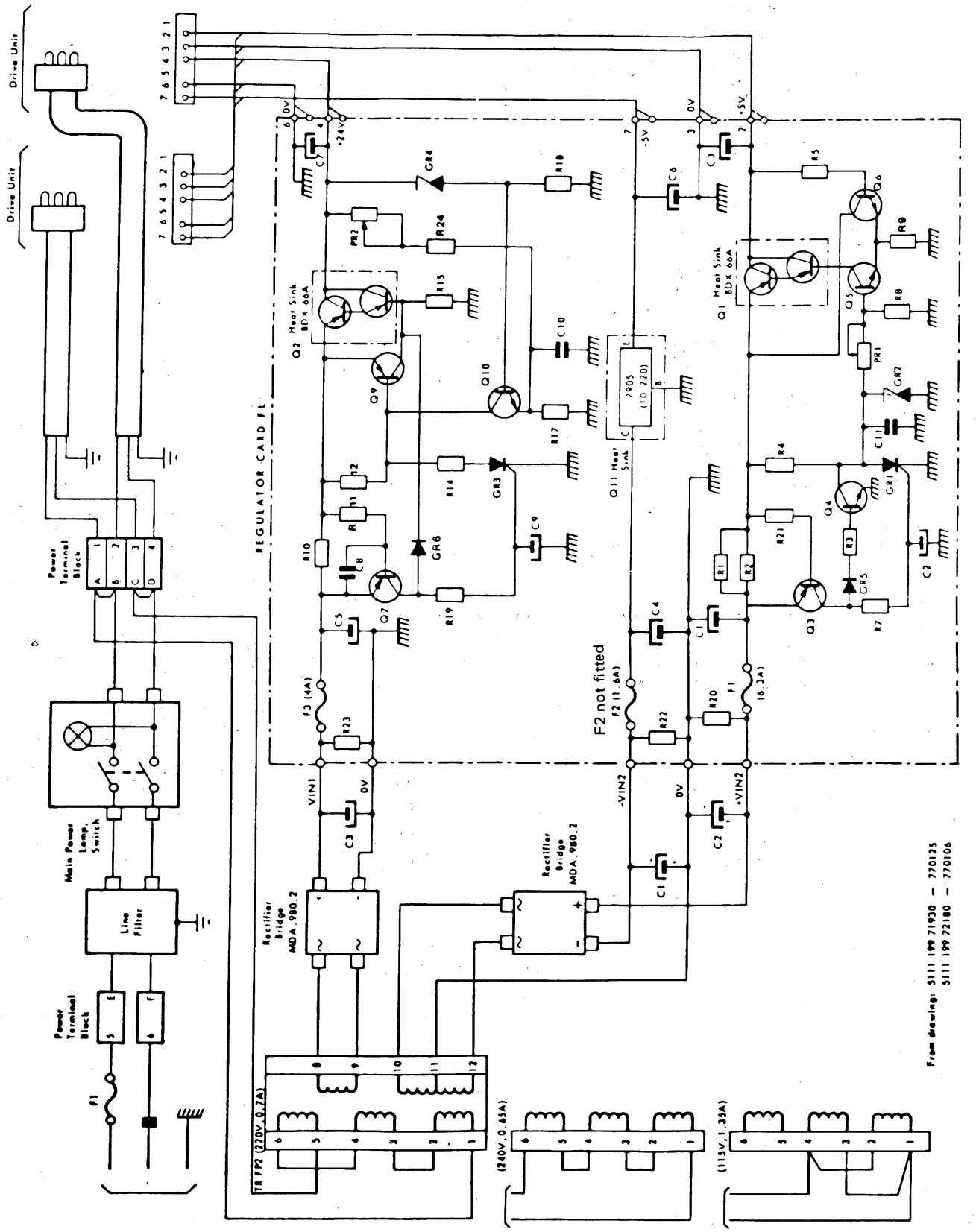
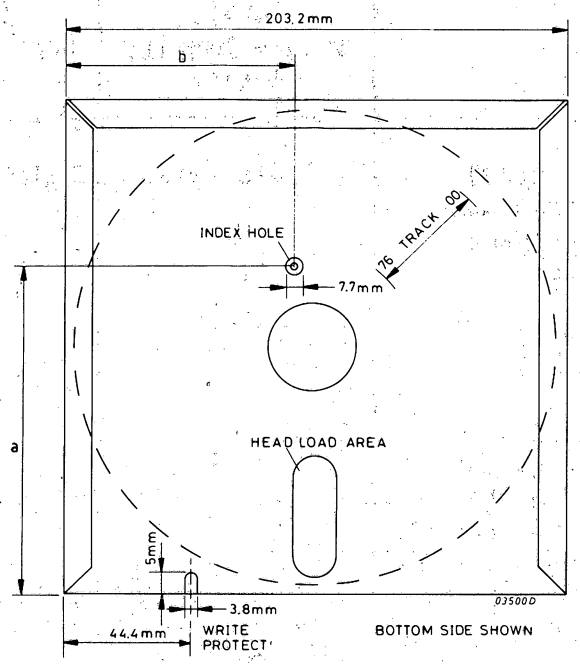


Figure 3.4.4 POWER SUPPLY CONNECTIONS FLOPPY RACK



Figures 3.4.5 POWER SUPPLY SCHEMATIC FLOPPY RACK

3.4.5 FLOPPY DIMENSIONS



	0.25M	1M
a =	139.4mm	135.9mm
b =	96.5mm	86.4mm

Figure 3.4.6 FLOPPY DIMENTSIONS

3.4.6 DRIVE CHARACTERISTICS

	CDE9404 Single Density 1 side	CDC9406 * Double Density 2 sides
Capacity (unformatted) (formatted and excluding spare tracks and track 00) - format 0 - format 1 - format 2	401,016 bytes 246,272 bytes	1,604,064 bytes 246,272 bytes 985,088 1,212,416
Number of discs Number of heads Tracks/surface (including spares)	1 1 77	1 2 77
Transfer rate Recording method	250K bits/sec (4uS/bit) FM (double frequency)	500K bits/sec (2uS/bit) MFM 250K bits/sec (4uS/bit) FM
Disc speed Latency time (1/2 revolution) Seek time - track to track - maximum Settling time Random average see time (incl. setting time) Head load time	360 rpm 83 ms 10 ms 760 ms 10 ms 260 ms 60 ms	360 rpm 83 ms 3 ms 228 ms 20 ms 96 ms 40 ms

Note: (*) On drive 9406 may also be loaded discettes single density, 1 sided, to be written/read according formt 0.

Table 3.4.2 DRIVE CHARACTERISTICS 9404/9406

3.4.7 PREVENTIVE MAINTENANCE

3.4.7.1 PREVENTIVE MAINTENANCE P830-035 (CDC 9406)

The 2 read/write heads can only be cleaned with a special head cleaning disc.

3.4. 7.2 PREVENTIVE MAINTENANCE P830-015 (CDC9404)

CLEANING THE READ/WRITE HEAD

Every 600 hours the read/write head requires cleaning which is carried out as follows:

- Use a lint free cloth to lightly dry buff head surface. Cleaning is completed if deposits are removed.
- If oxide deposits were not removed in the step above, dampen (do not soak) cloth with head cleaning solution (isopropanol), and wipe head surface. Finish by slightly dry buffing again to ensure that the head is dry and no alcohol residue is left.

CAUTION

Do not smoke while cleaning. Do not touch a head surface with fingers. Do not leave residue or line on the head. surfaces. Residual particles can result in a stored disc and/or loss of a head.

REPLACING THE HEAD LOAD PAD

Every 1200 hours, in addition to the cleaning above, the head load pad should be inspected. If the pad is worn, dirty, torn or loose it should be replaced, as described below:

. Remove power from the unit.
. Move the carriage assembly to its rear most position (toward the stepper motor) by turning the back part of the stepper motor shaft. This will provide clearance for lifting the head load arm.
. Lift the head load arm until the head load pad is visible.
. If head load arm is a 77603108 proceed four steps ahead, if not go to next step.
. Remove the used pad with a sharp tool, if necessary, and discard. Be sure to remove all of the old pad and adhesive. Alcohol may be used to remove the old adhesive.
. Remove the protective packing from the new head load pad and position pad in approximate center of recess in head load arm. Press pad firmly to insure adhesion with a clean tongue depressor or with a thumb using a lintfree cloth to protect pad from grease or dirt.
. Go to the last step.
. Loosen clamping screw holding rim of head load pad.
. Insert screw driver and rotate head load pad with flat side toward clear clamping screw.
. Remove Pad Holder Assembly.
. Insert new Assembly, with flat side toward clamping screw.
. Assuring that head load pad is fully seated, rotate pad 180°.
. Tighten clamping screw to hold pad in place.
. Lower arm gently on to head.

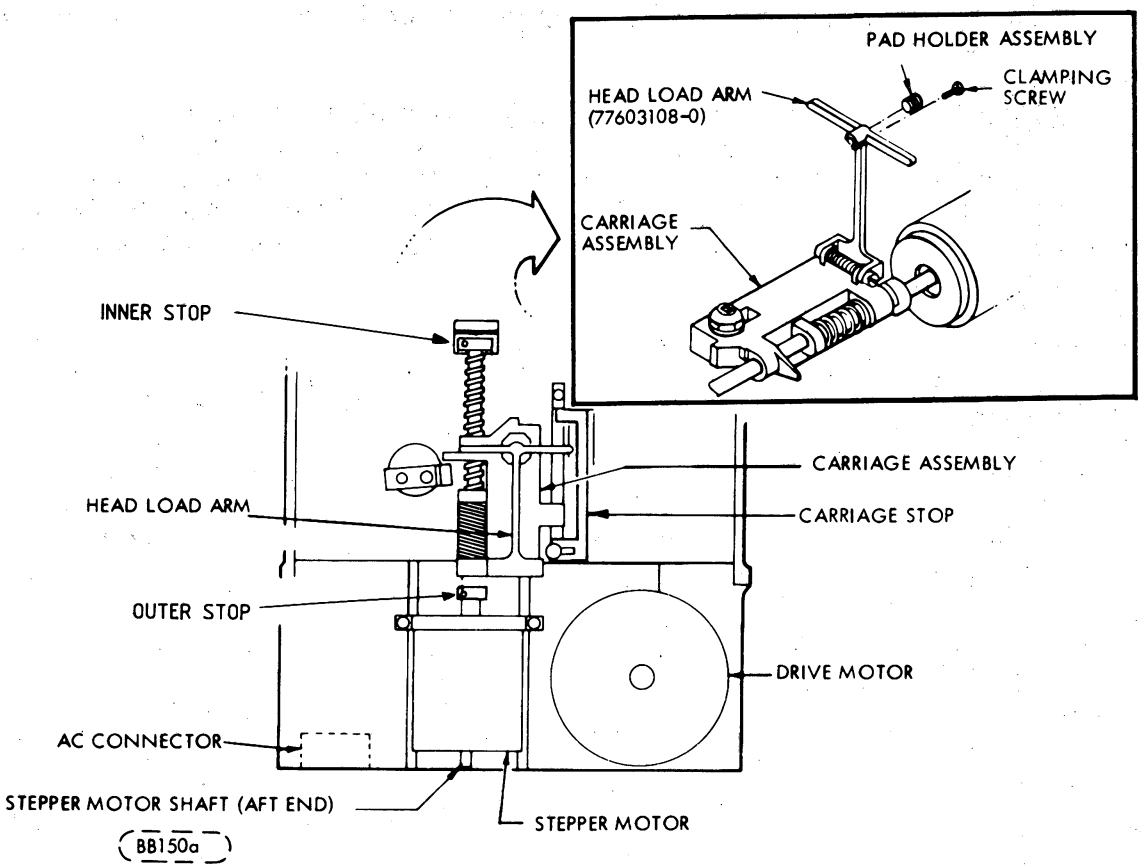


Figure 3.4.7 HEAD LOAD PAD REPLACEMENT P830-015

OPERATING FREQUENCY CONVERSION PROCEDURE P830-015 (CDC 9404)

This procedure should be used to convert the FDD unit from 50Hz. operation to 60Hz. operation or vice vers. This is accomplished by reversing the dual diameter reversible pulley on the spindle motor shaft using the following steps:

. Remove AC power.
. Disconnect I/O cable from J1 on the printed circuit board.
. Disconnect I/O harnesses from J2, J3, J4, J5 and J6 on the board.
. Remove two screws from board adjacent to connector J1 (see figure A).
. Remove board by detaching it from the four push-in clips shown in figure A.
. Remove the belt from the spindle motor pulley (accessible from the under side of unit.
. Loosen set-screw and remove pulley.
. Reverse pulley and replace on motor shaft.
. Position pulley allowing tolerance of 0.079" (2.01 mm) ± 0.010" (0.254 mm) between shoulder of motor mounting screws and pulley. (Figure B).
. Tighten down set-screw.
. Replace belt and printed circuit board.

Note: It is important that the new operating frequency is marked on the units rating nameplate.

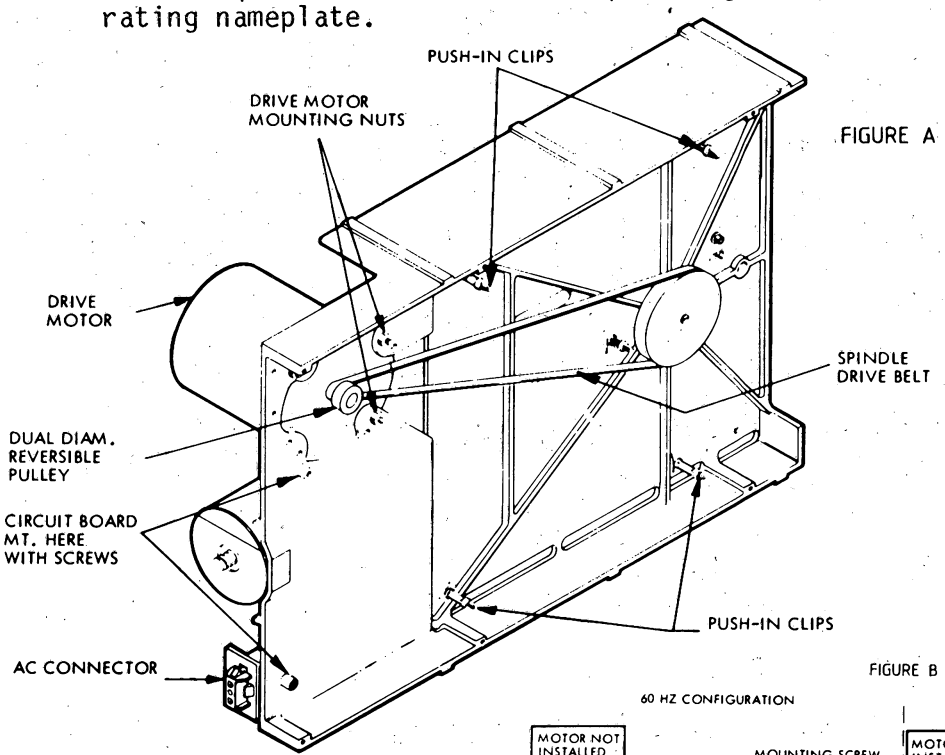


FIGURE A

FIGURE B

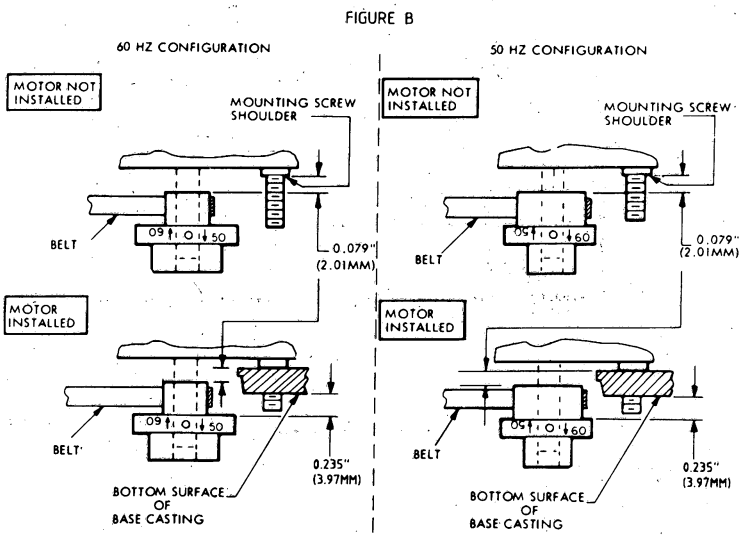


Figure 3.4.8 FDD FREQUENCY CONVERSION INSTRUCTIONS P830-015

3.5 EQUIPMENT SHELF E2 P843-001

3.5.1 IDENTIFICATIONS

P843-001/02: Equipment Shelf E2 (6 slots) - 5111 199 60910
P843-009/01: Terminator GP-bus - 5111 199 77690

3.5.2 DESCRIPTION SHELF E2

Number of slots : 6 card slots for control units (slaves) connected directly to GP Bus.

Size : Height 3U (approx. 132.5mm)

Terminator : A terminator must be connected at the end of the GP-Bus in the last E2 shelf.

Mains Fuse : 220V - 3.15A / 115V - 6.3A

Power Supply : + 5V 18A
+18V 1A
-18V 1A

Remote Control : +5VL from main rack is used if Local/Remote Switch in position Remote.

In the P871/P874/P876 systems the E2 shelf can only be used if connected via the TUGP card.

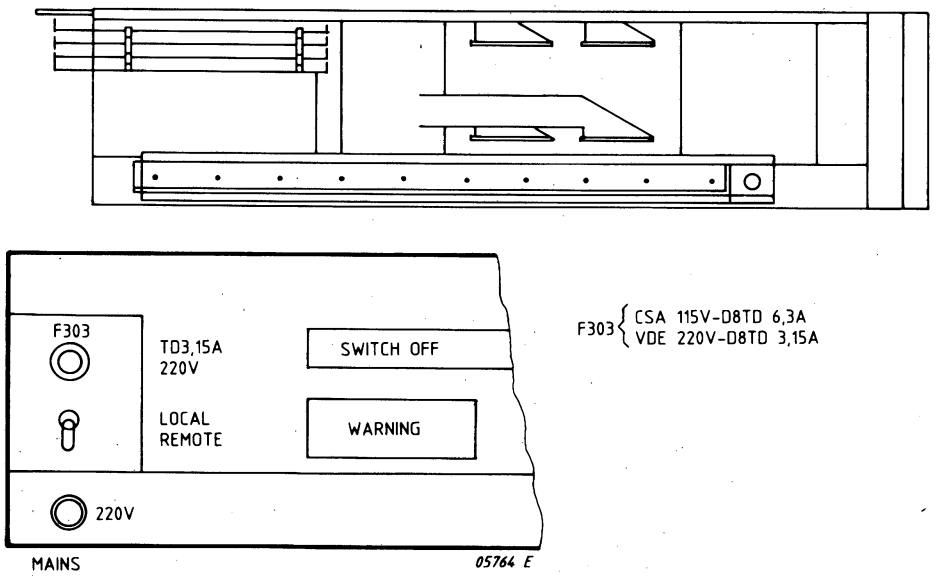


Figure 3.5.1 EQUIPMENT SHELF P843-001 (E2)

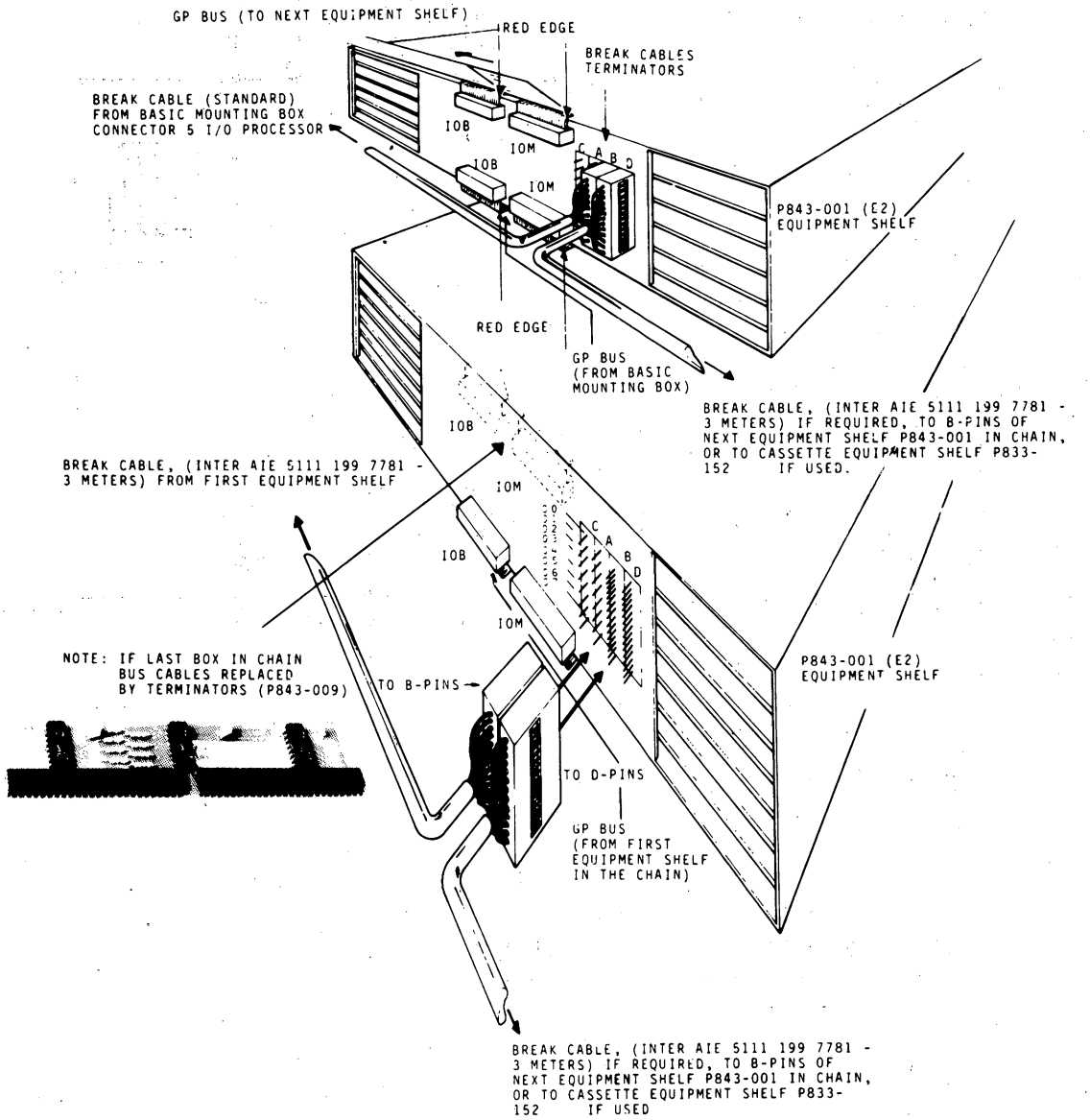


Figure 3.5.2 BUS AND BREAK CABLE EXTENSION (E2)
(USING P843-001 EQUIPMENT SHELF)

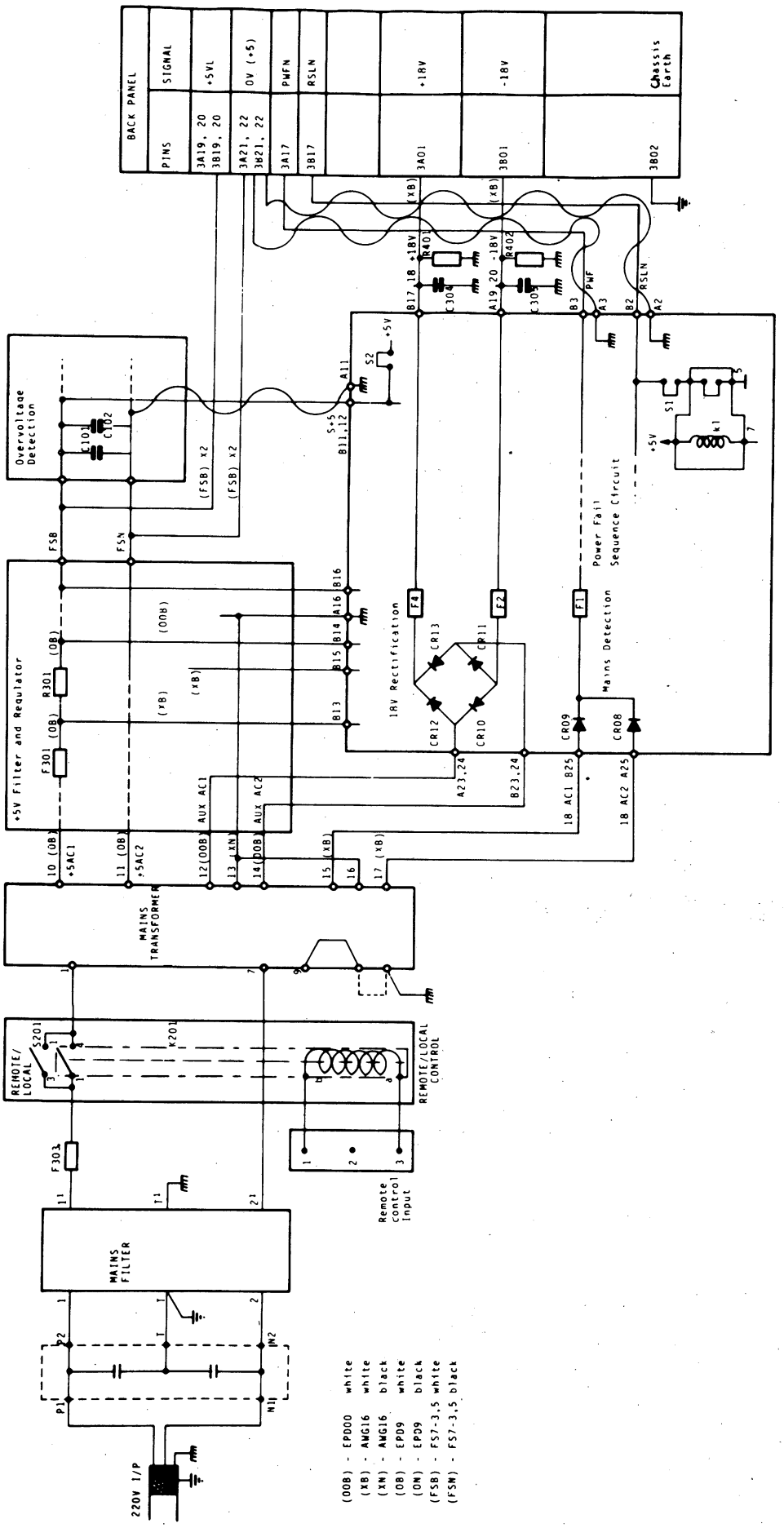


Figure 3.5.3 POWER SUPPLY SCHMATIC P843-001

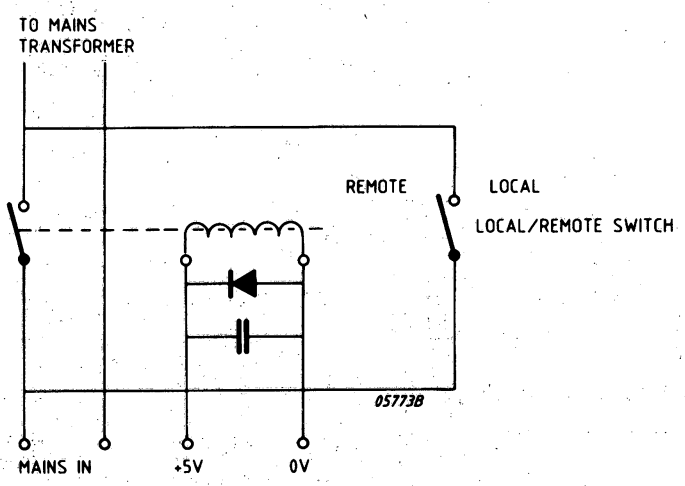


Figure 3.5.4 REMOTE CONTROL CIRCUIT P843-001

4 INSTALLATION

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4.1 INTRODUCTION

Each P800 computer system is supplied with a set of configuration Sheets (that were compiled when the system was tested in the factory) which give the following details:

. Invoice sheet of the system or units ordered.

. Parts list specifying the major items in system (including I/O cards and logic options.

. Wiring instructions for the interconnecting and signal cables.

With the information in these sheets most systems can be installed without any problem; however, for large systems (and when enlarging existing systems) problems can arise which are not always covered by the Configuration Sheets.

4.2 SITE PREPARATION

Extensive site preparation is not normally required before installing a system. For simple configurations that will be part of a much larger existing system no site preparation is necessary. In general the only requirement is a floor strong enough to support the component parts of the system. A floor able to support a static loading of 500 kg/m^2 is strong enough for any mini-computer system.

4.2.1 ENVIRONMENTAL CONDITIONS (TABLE 4.1)

The CPU can operate through a wide range of environmental conditions so the need for air conditioning etc., will depend on the peripherals used by the system. It is expected that the CPU and its peripherals will be located in an office/factory environment where the air is not contaminated by industrial processes. The general conditions for storage (with or without packaging), transport and operating are given in the following two tables; however, peripherals using magnetic media may specify more stringent conditions.

CLIMATIC CONDITIONS		O	NO	T
Temperature Range		0 to 50°C	-40 to 70°C	-40 to 70°C
Temperature Gradient		.LE. 1° C/mn	.LE. 1° C/mn	.LE. 1° C/mn
Pressure		600 to 1100 mb	600 to 1100 mb	600 to 1100 mb
Humidity without Condensation	RH%	.LE. 95%	.LE. 95%	
	TRE	.LE. 40°C	.LE. 40°C	
	DEW POINT	.LE. 30°C	.LE. 30°C	

Table 4.1 CLIMATIC CONDITIONS

MECHANICAL CONDITIONS	O	NO	TS
Vibrations	Freq. Range: 10-58Hz Peak Value : 0.75mm	Freq. Range: 10-500Hz	Freq. Range: 10-500Hz.
		Peak Value: 0.75mm	Peak Value: 0.75mm
	Freq. Range: 58-500Hz Acceleration: 0.5 g.	Acceleration: 1g.	Acceleration: 2.5g.
	Sweep Rate: 1 oct./mn	Sweep Rate: 1 oct./mn	Sweep Rate: 1 oct./mn
Shocks	Acceleration: 5 g.	Acceleration: 15g.	Acceleration: 15g.
	Duration: 11ms	Duration: 11ms	Duration: 11ms
	Motion: Half-sine One direction: -Oz	Motion: Half-sine One direction: - Oz	Motion: Half-sine Six directions

Note: For Operating conditions, the vibrations and shocks are those encountered at rack level.

Table 4.2 MECHANICAL CONDITIONS

4.2.2 ELECTRICAL REQUIREMENTS

A single phase a.c. supply complying with the following specification should be provided for the exclusive use of the computer system. It should be either a 3 wire single phase, neutral and earth, or two phases and earth; its current carrying capacity must be adequate for the total power requirements of both the CPU and the peripherals. The requirements are:

Voltage: : 115V, 220V or 240V r.m.s. ± 10%

Frequency : 50±2Hz or 60±3Hz

Voltage Transients : 1.5kV peak amplitude for a duration not exceeding 10 microseconds between half peak points at a repetition frequency of 3 to 10Hz. for not more than 10 minutes.

Transient State : The time between the voltage falling from nominal to zero and then returning to nominal must be not greater than 0.5 seconds.

Power Interrupts : Less than one every 10 seconds for a duration not exceeding 10ms.

If the mains supply is subject to frequent interruptions or failures, it is advisable to install an alternative supply source such as a rotary motor/generator.

4.3 CONFIGURATION GUIDE

This guide mainly concerns operational access and uniformity of appearance, but is not important as far as system performance is concerned. The only critical layout restrictions concern the interconnecting peripheral signal cables and transmission lines. The rack is divided into imaginary levels and table 4.3 shows the recommended positions for the different units.

	NAME
1U	VENTILATION UNIT
6U	FLOPPY DISC RACK
4U	CONTROL PANEL-KEY VENTILATION UNITS
6U	CPU - LOGIC RACK
2U	CABLE SUPPORT - FAN
1U	
6U	FIRST RACK "RAWIST"
1U	
6U	SECOND RACK "RAWIST"
3U	POWER DISTRIBUTION

* 1 unit = 1.75 inches = 44.45 mm.

Table 4.3 RECOMMENDED UNIT POSITIONS P876

4.4 RULES FOR CONNECTING GROUNDS IN A SYSTEM

Each cabinet must have a mechanical ground or safety earth point to which the safety earth points of all the units mounted in the cabinet are connected. This safety earth point must be electrically connected between the main frame and the earth wire of the power cable supplying the cabinet from the site mains. Each cabinet must also have an electrical ground of OV and the shields of cables must not be used as inter-unit safety earth conductors. Cable shields must be connected to the safety earth using earthing leads as short as possible and of the same cross sectional area. To avoid either internal or inter-cabinet Electromagnetic interferance, the mains cables to the different units should be mounted against the left-hand side of the mainframe and the I/O cables should be mounted against the right-hand side of the mainframe (view from rear side).

4.4.1 GROUNDING RULES FOR MOUNTING BOXES AND CABINETS

The following rules should ensure a good ground continuity between the cabinets and the mounting boxes:

- Fixed Mounting Boxes
  These mounting boxes are fastened to the mainframe by screws and a good continuity between the cabinet and the box is ensured by keeping the mating surfaces clean.

- Slide Mounted Boxes
  A box mounted on telescopic slides does not have a reliable ground path so it is essential that an electrical link is made using metal braid. Remember using the ground conductor of the main lead or cable shielding for the ground connection is NOT acceptable.

- Cabinet Panels and Doors
  All doors and panels must have a good electrical link to the mainframe and in particular the doors must be connected with metal braid.

The following diagram shows some examples:

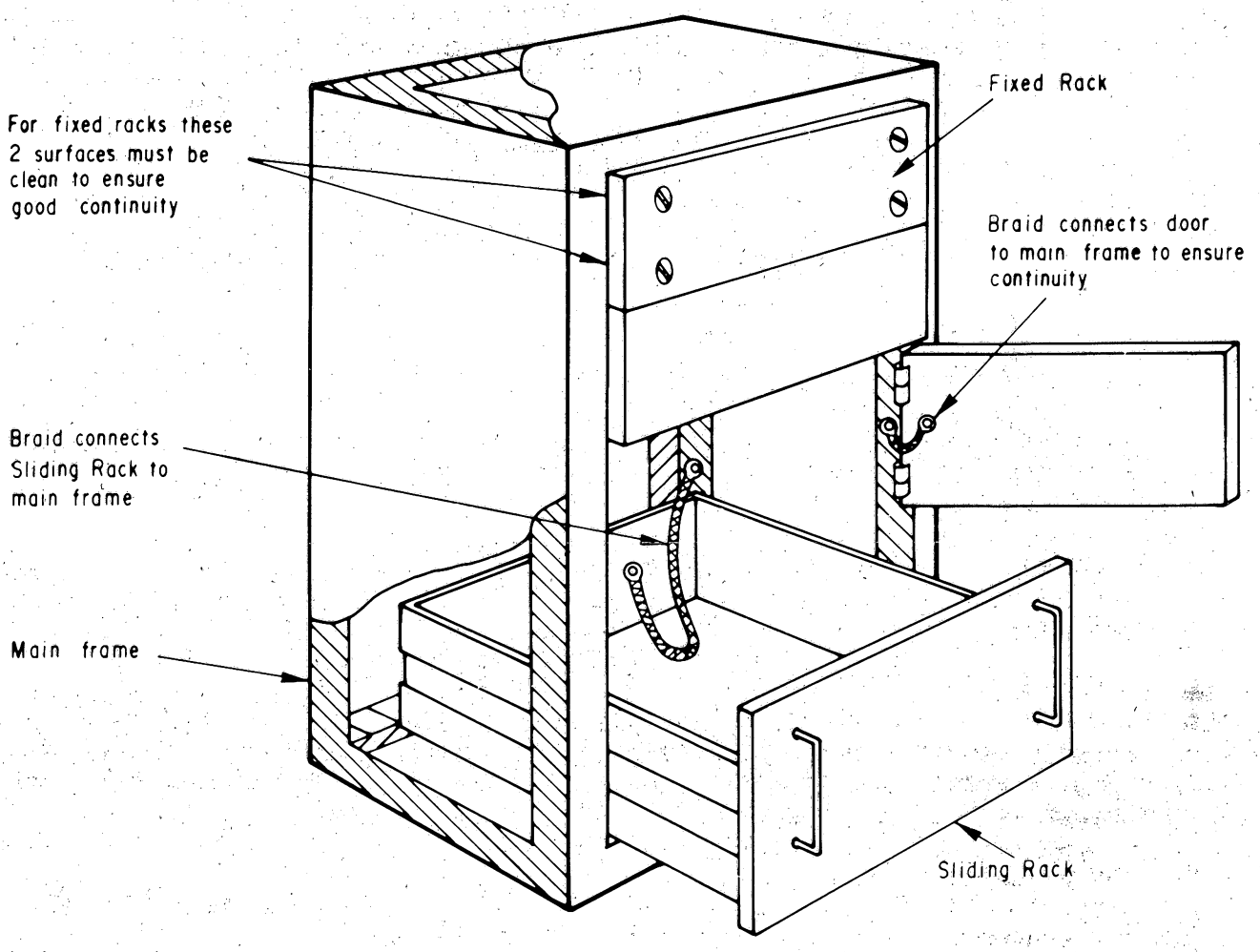


Figure 4.1 EXAMPLE FOR SYSTEM GROUNDING

4.4.2 LOGIC GROUND AND MECHANICAL GROUND

Logic ground and mechanical ground points are provided in each Mounting Box. They are situated close to each other and may be either connected or disconnected.
Figure 4.2 gives an example for Flexible Disc Drive shelves.

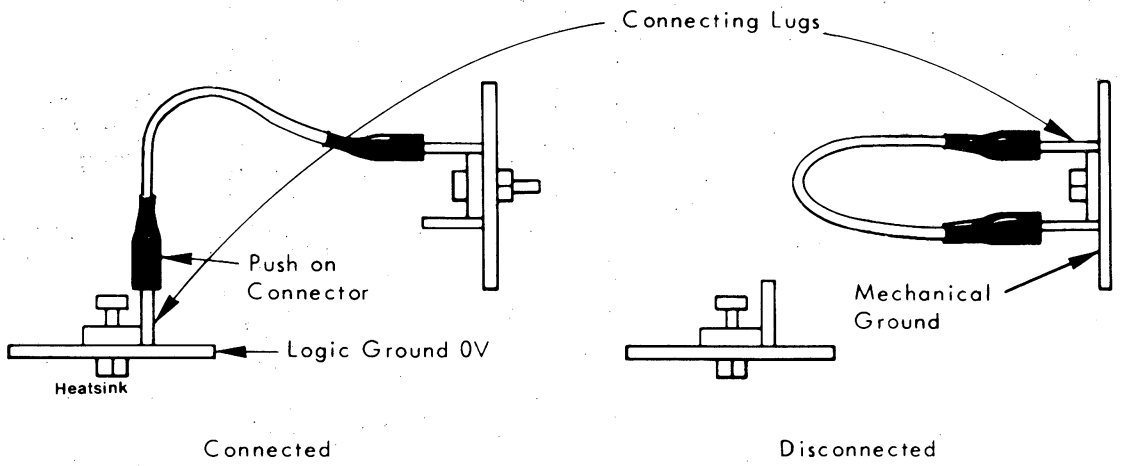


Figure 4.2 LOGIC AND MECHANICAL GROUND

A system may use several cabinets each containing a number of Mounting Boxes, but only one may have this link connected. All other cabinet links are disconnected.

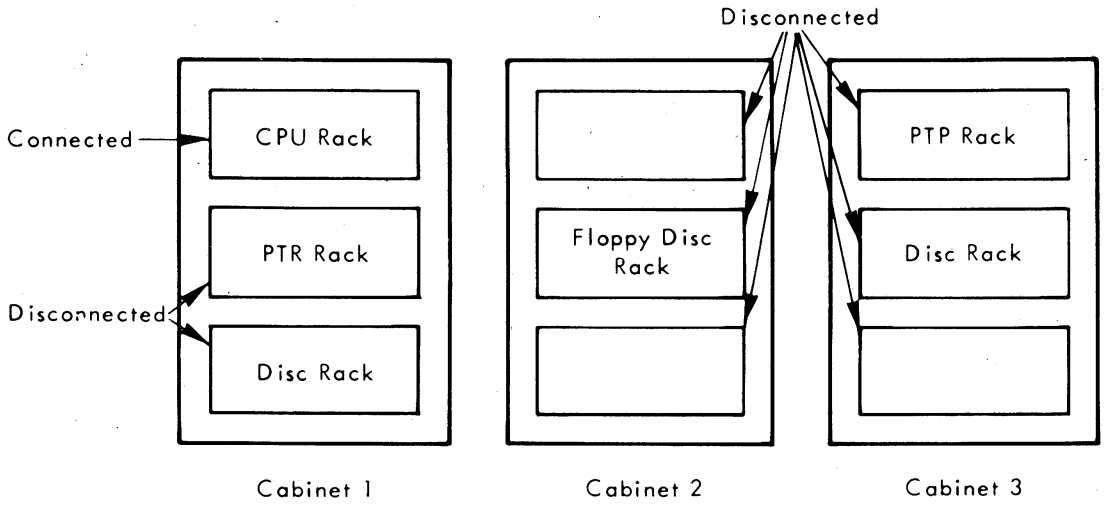


Figure 4.3 GROUNDING OF MOUNTING BOXES

In a normal configuration the cabinet that holds the CPU/CIP is connected and all other cabinets are not connected. If more than one CPU/CIP is being used in the system then the user decides which CPU/CIP cabinet is to have the link connected.

4.4.3 FLAT CABLES

Flat cables without shielding may cause electromagnetic fields to be set up in the equipment, so the use of such cables should be avoided. If this is not possible, the following special precautions must be taken:

- If channel type supporting members are in the cabinet, then they should be used so as to provide a shield around the cable.
- If these supporting members are used, then the cables should be run separately; either clamped flat against the panels or against the outside of other supporting members.
- Mounting flat cables one on top of the other should always be avoided. If this method must be used, then a metal plate (suitably supported and electrically connected to the cabinet) should be inserted between the cables.

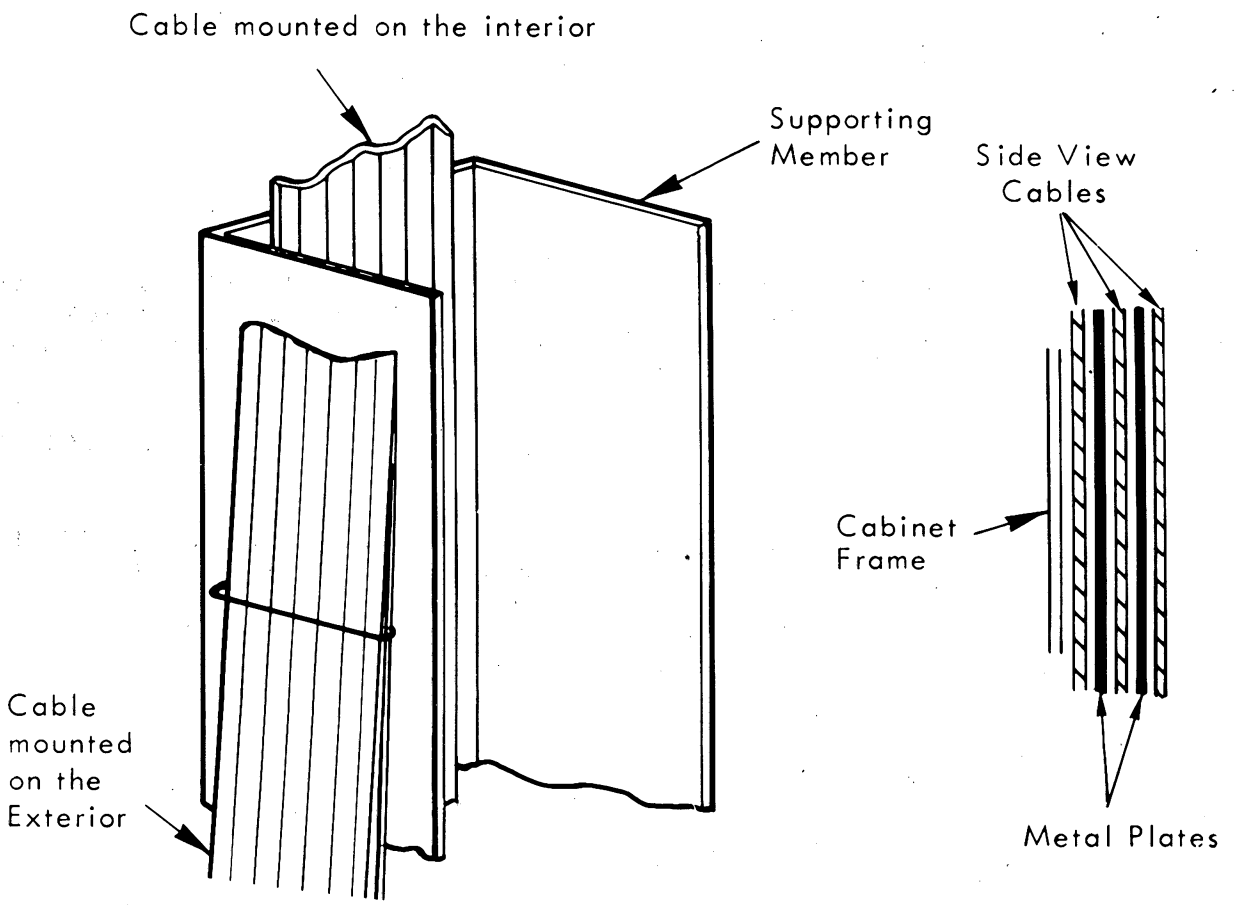


Figure 4.4 FLAT CABLE MOUNTING

4.4.4 MAINS CABLES

When planning an installation, an area along the mainframe should be reserved for the mains cables and all other cables should be kept as far as possible from this part of the mainframe. It is recommended that the cable be shielded either before or after the mains filter and that this shielding be connected to the mechanical ground at each end of the cable. The mains cable must be secured to the chassis by a metal clamp at the point where the shielding extends outof the cable sheath. Remember that the screw fixing the ground conductor to the chassis must be as close as possible to the metal cable clamp.

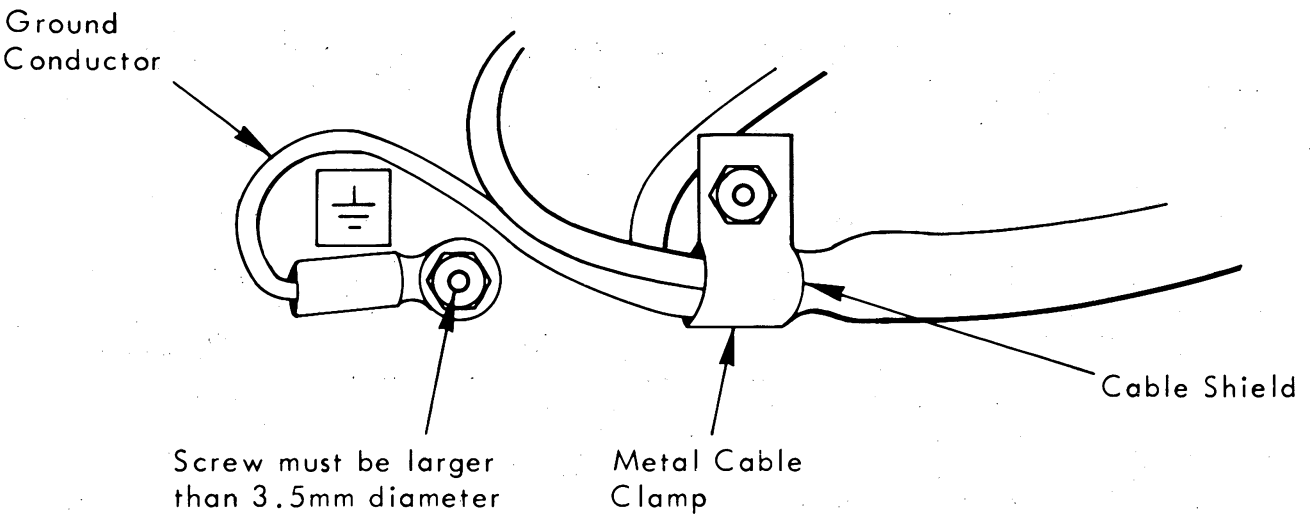


Figure 4.5 MAINS CABLE MOUNTING

4.4.5 GENERAL RULES FOR SHIELDED CABLES

All twisted pairs must be contained inside a shielded cable and this shield must be connected to mechanical ground at each end. Specific lead dimensions are given for some peripherals but as a general rule the following dimensions should be adhered to:

- The lead must be as short as possible and never exceed a maximum length of 15 cm.
- Connections to the shielding must be soldered and connections to the mechanical ground must be made with either an eye-lug (for a 3 mm screw) or a push-on type connector (Faston 6.35 or equivalent).
- The cross section of the lead must be a minimum of AWG16 guage.

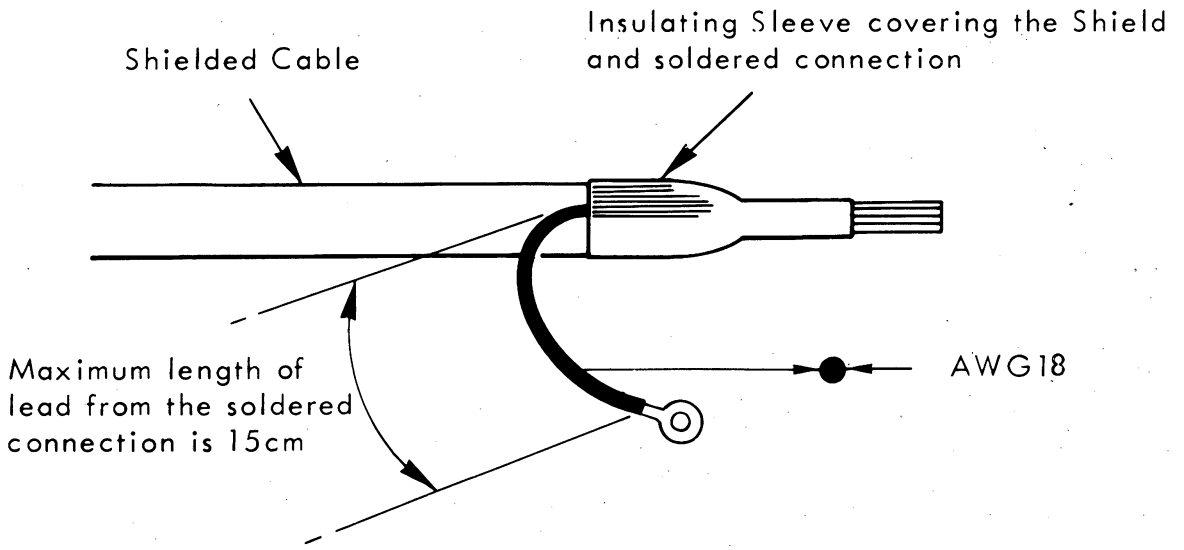


Figure 4.6 SHIELDED CABLE MOUNTING

4.4.6 SPECIAL RULES FOR SHIELDED CABLES

For some devices the lead dimensions for connecting the shielded cables at the device and at the CPU/CIP are different from the general rules. These devices are listed in the following table.

	AT THE DEVICE			AT THE CPU/CIP		
	AWG	MAX. LENGTH	EYE LUG	AWG	MAX. LENGTH	EYE LUG
Magnetic Disc X1215/16	16	20cm	4mm	16	15cm	3mm
Magnetic Disc 9760/9762	16	08	3	16	10	3
Line Printer X1415/25	16	10	3	16	10	3
PER3100 (V24 Interface)	16	15	4	16	10	3
PER3100 (Curr. Loop Int.)	16	15	4	18	03	Molex pin 3
Display P817	16	10	4	16	10	3
Display P816/818	PUC system			PUC system		
Cables with "BERG" conn.	PUC system			PUC system		
Flat cables	-			-		
	At the Terminal Box					
Remote Control Cables	18	10	--	18	03	Molex Center Pin
Break Cables	At the Extension Box					
	16	10	3	16	15	3

Table 4.4 SPECIFIC LEAD DIMENSIONS

4.4.7 GROUND LEADS IN CABINETS OR BOXES

The connection of ground leads for cabinets or boxes depends on the type of installation. The following examples show the different type of ground connections:

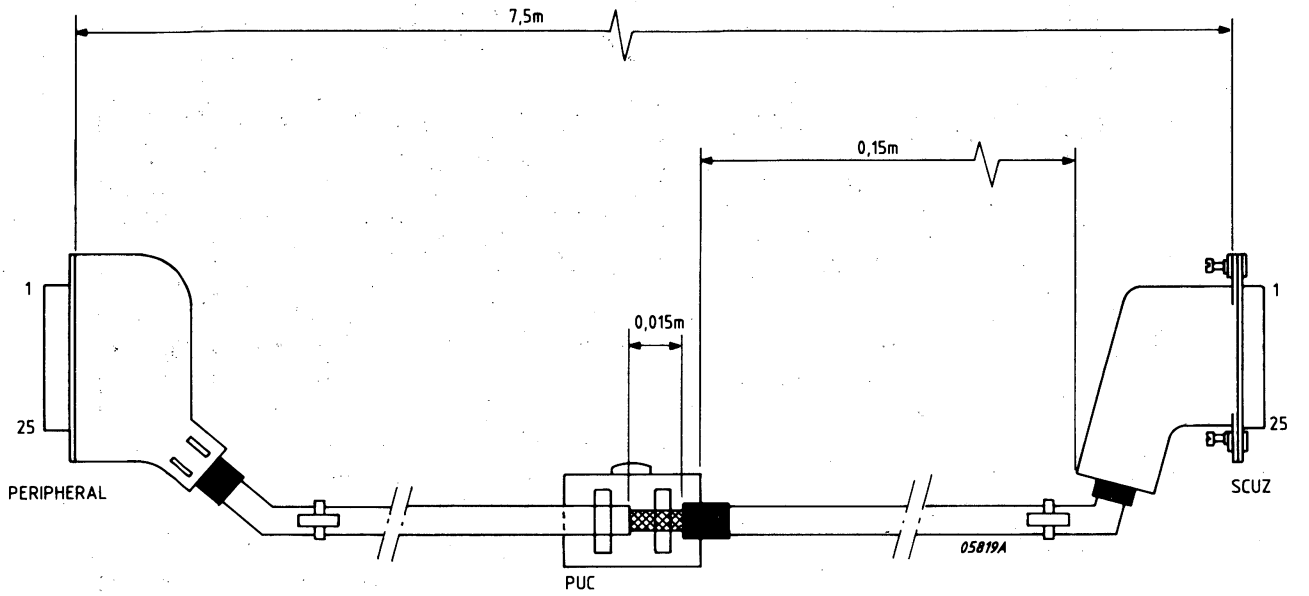


Figure 4.7 SCUZ CABLE USING PUC SUPPORT (CABLE 5111 199 52550)

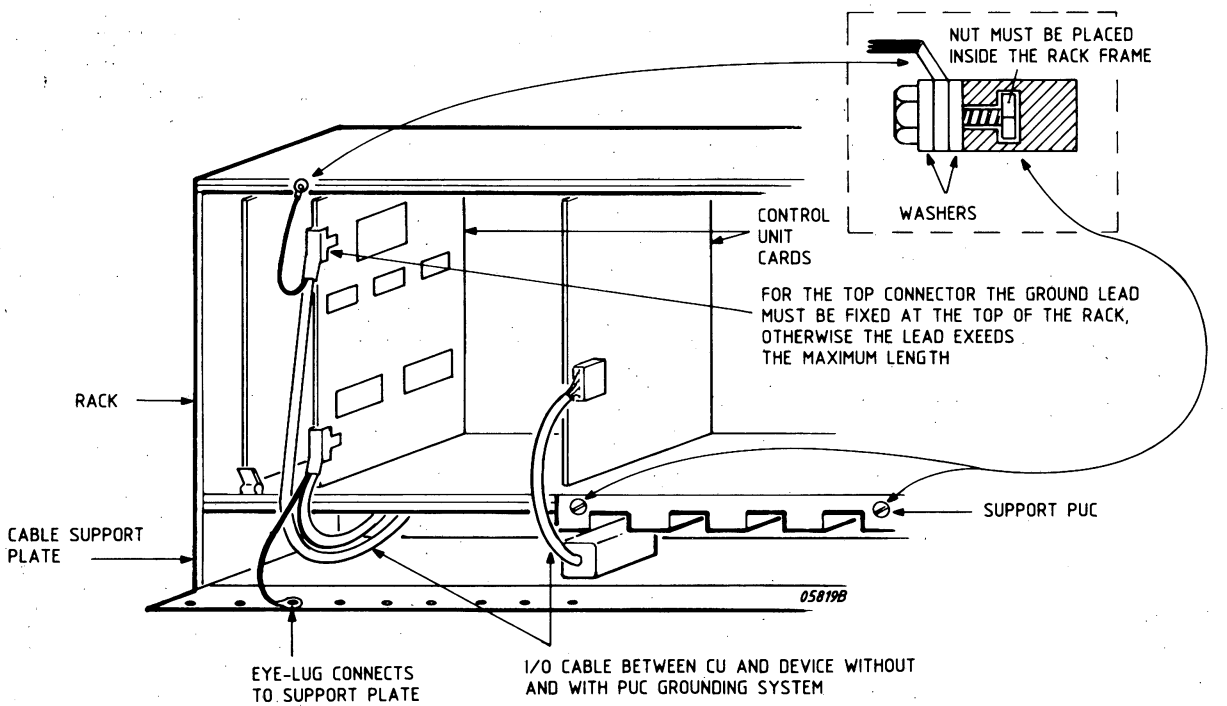


Figure 4.8 EXAMPLE USING CABLE SUPPORT PLATE AND PUC SUPPORT

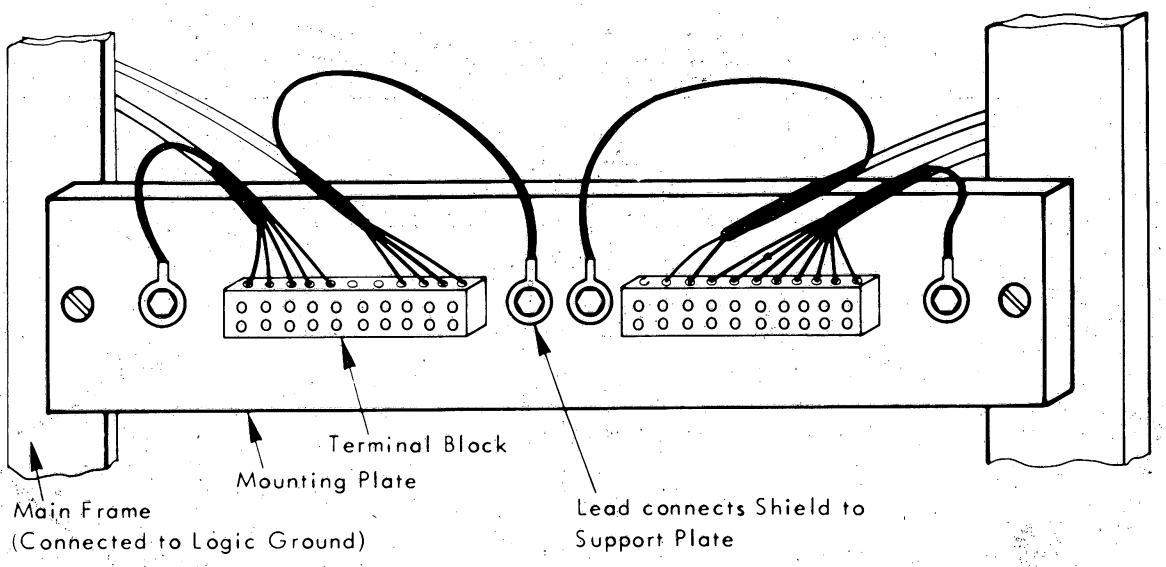


Figure 4.9 EXAMPLE USING TERMINAL BLOCKS

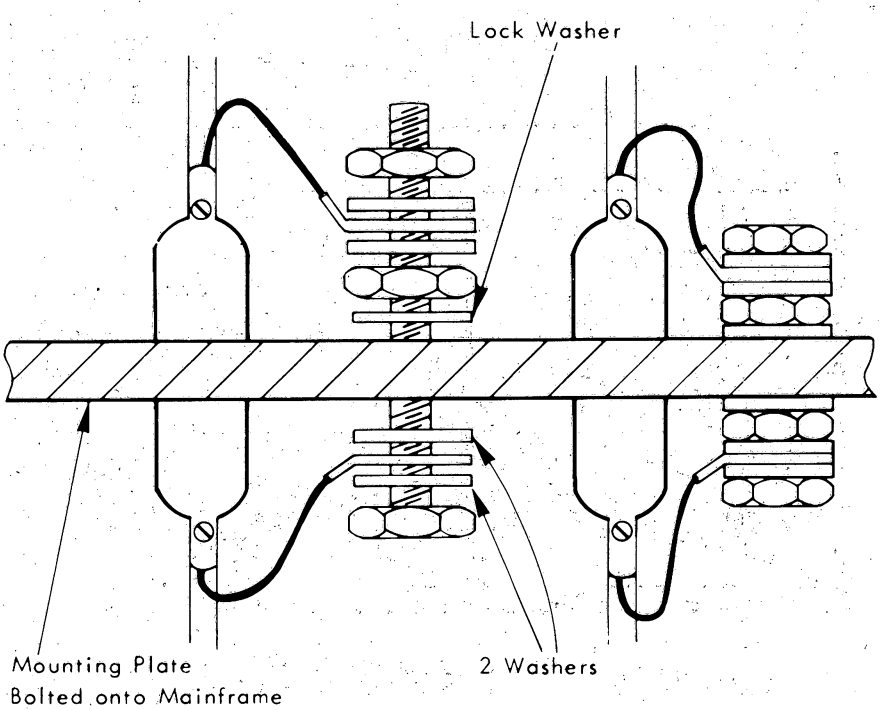


Figure 4.10 EXAMPLE USING CONNECTORS (TOP VIEW)

4.4.8 GROUND LEADS TO DEVICES

The following illustrations show how a ground lead is connected at some of the peripheral devices:

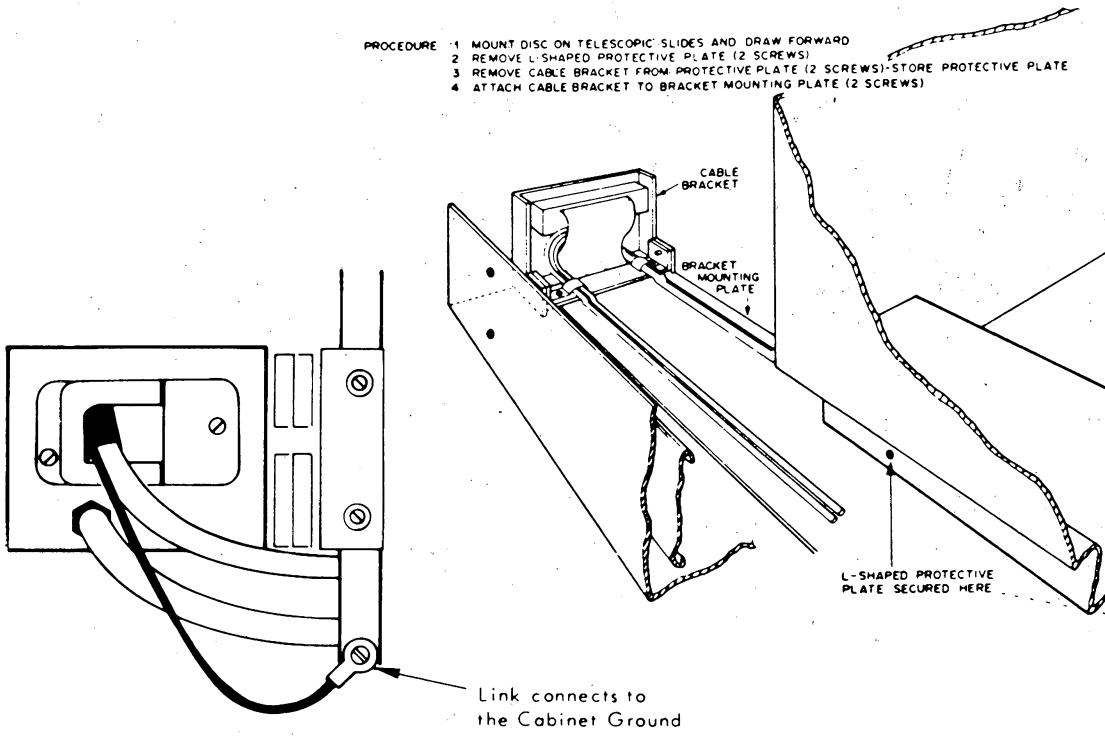


Figure 4.11a GROUND LEAD P824-012/014 (CARTRIDGE DISC DRIVE)

Figure 4.11b MOUNTING THE P824-012/014 (CARTRIDGE DISC DRIVE)

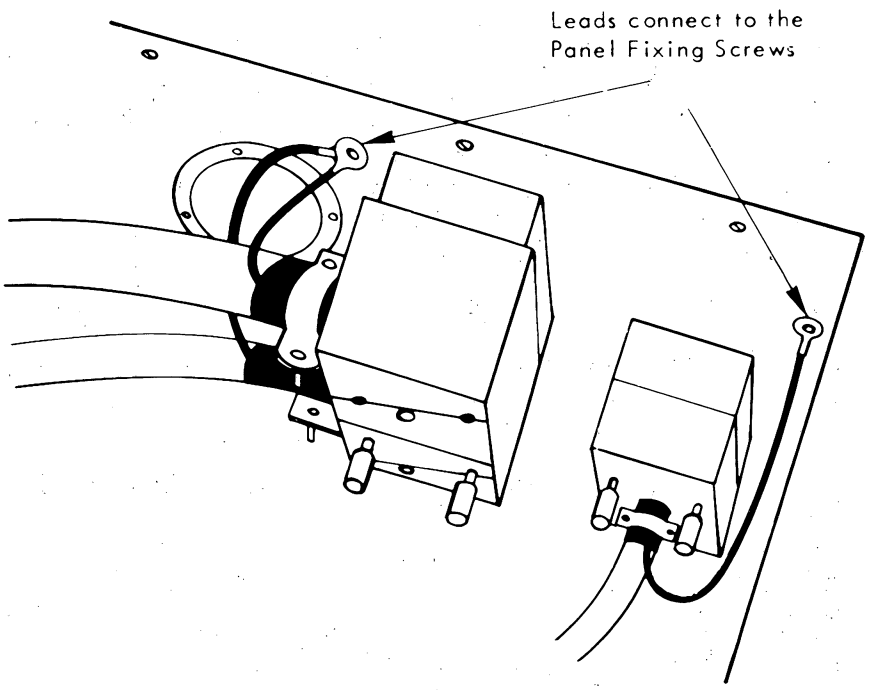


Figure 4.12 GROUND LEAD - P825-008 (STORAGE MODULE DISC DRIVE)

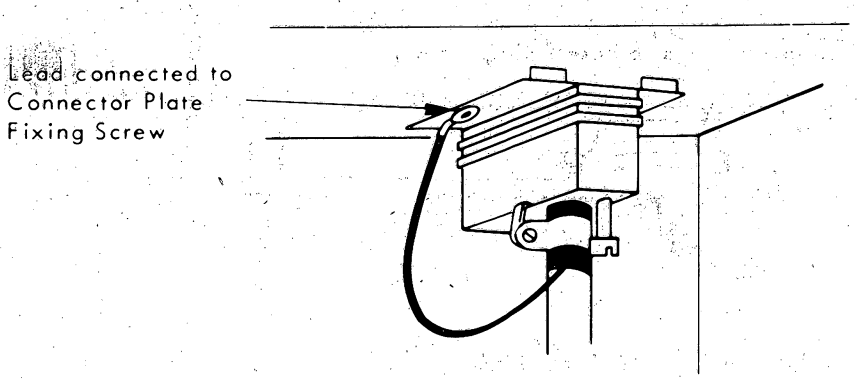


Figure 4.13 GROUND LEAD - P809-002/004 (LINE PRINTER)

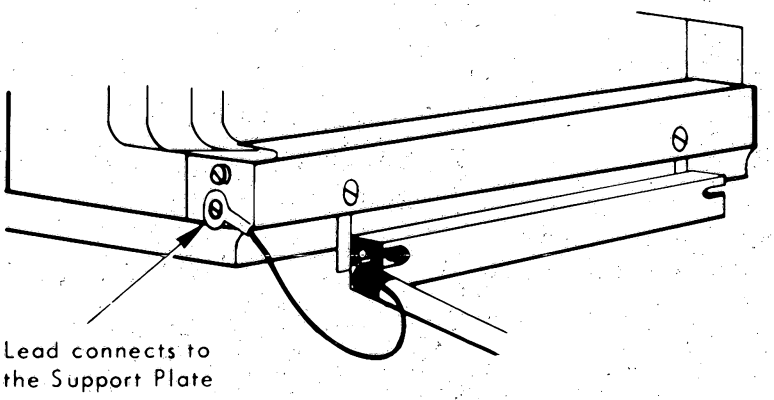


Figure 4.14 GROUND LEAD - P801-802 (PAPER TAPE READER)

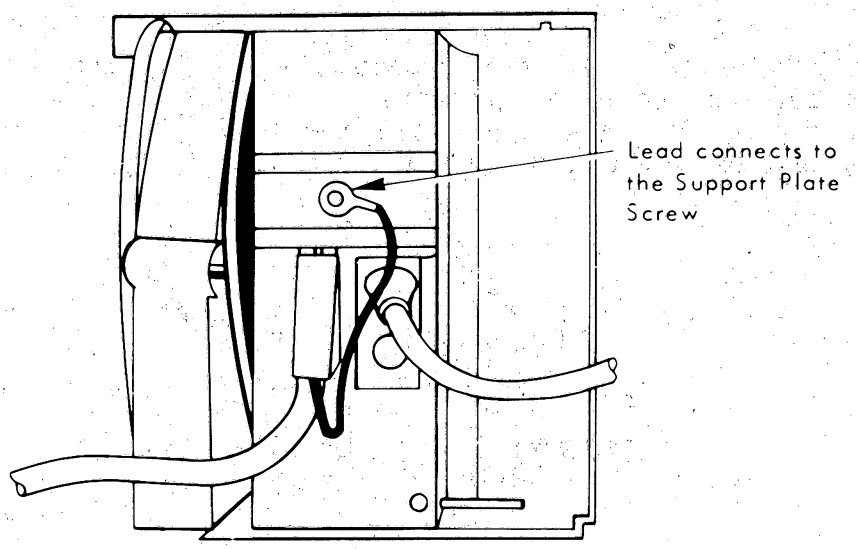


Figure 4.15 GROUND LEAD - P803/804 (PAPER TAPE PUNCH)

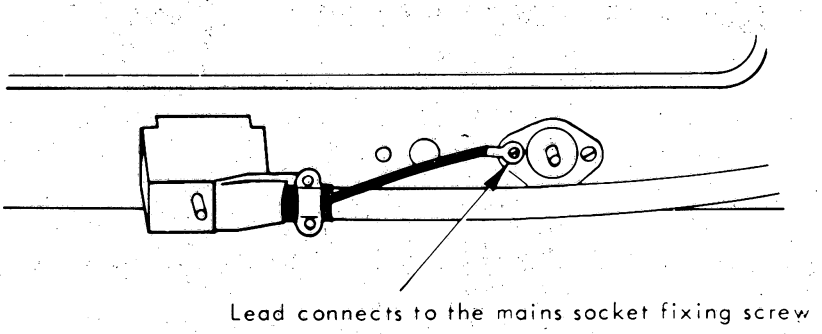


Figure 4.16 GROUND LEAD - P806/102 (CARD READER)

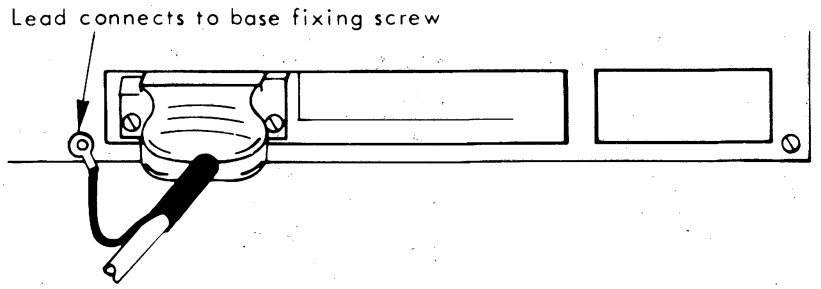


Figure 4.17 GROUND LEAD - P817 (VIDEO DISPLAY UNIT)

V24 Interface - At the device a tapped hole near the connector should be used to attach the lead.

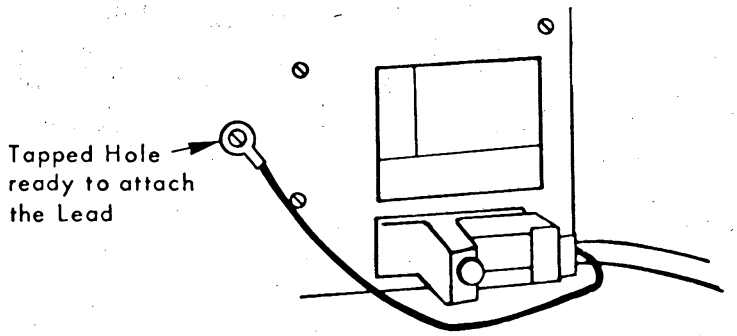


Figure 4.18 GROUND LEAD - P842 (PER3100)

Current Loop Interface - At the device when using the extension cable the connection between the Molex connector pin 6 and the ASR mechancal ground is made with the cable shielding. Note that under no circumstances the Molex connectors must be situated outside the ASR base.

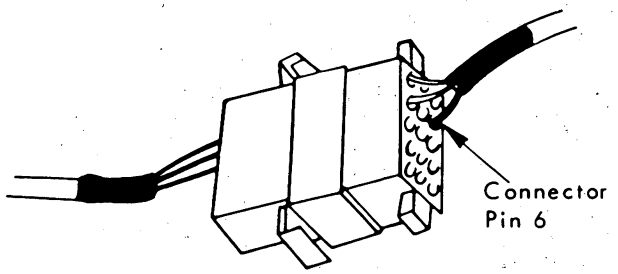


Figure 4.19 CURRENT LOOP INTERFACE CONNECTION

Cabinet side - The shielding is connected to the central pin of the Molex connector.

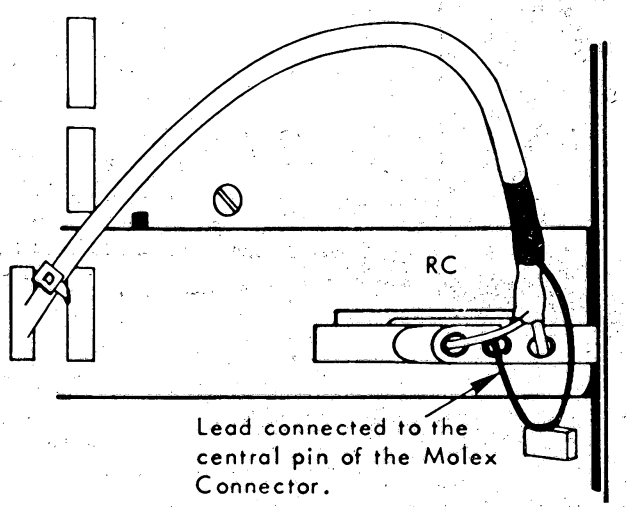


Figure 4.20a REMOTE CONTROL CABLE - CABINET SIDE

Connection at the Cabinet Terminal Box - When connecting the shielding of two cables at the Terminal Box, connect to the same terminal to ensure good continuity.

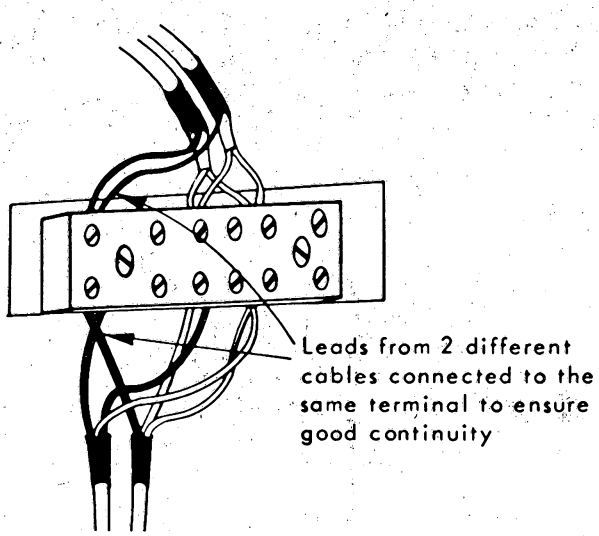


Figure 4.20b REMOTE CONTROL CABLE - CABINET TERMINAL BOX SIDE

Break Cable

At Extension Rack

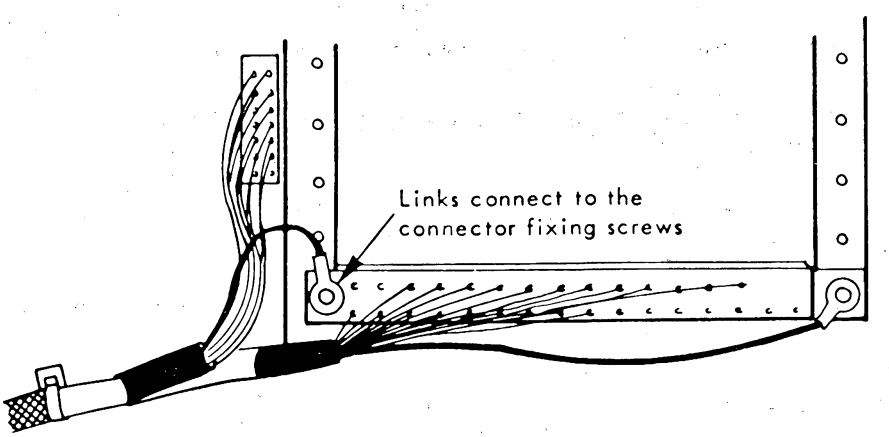


Figure 4.21 BREAK CABLE EXTENSION RACK

Formatter Tape

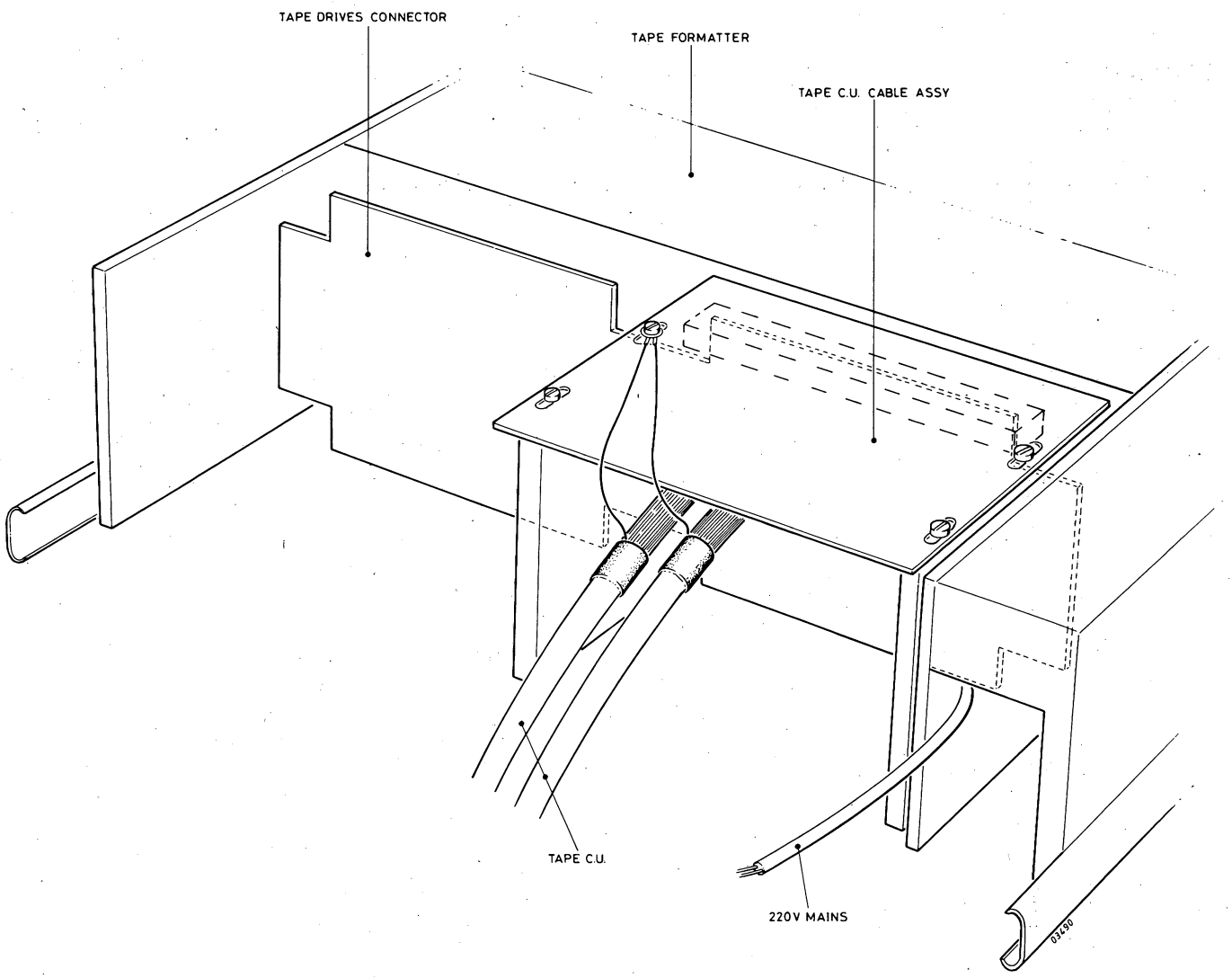


Figure 4.22 CABLE - TAPE FORMATTER

4.5 PUC KIT WITH BERG CONNECTOR

. Cut the cable to its precise length (allowing for subsequent movement of equipment for servicing).

. Thread the cable marker(s) and strip the cable according to top figure.

. Fold screen back over the sheath and apply 1 1/4 layers of CU-tape around the wires, close to the sheath.

. Restore the screen and apply another 1 1/4 layer of CU-tape, not around the screen over the previous layers.

. Tie the for part of the screen, thread on the insulating tube and tie it at the rear end.

. Strip 4 mm of the wire ends and crimp on the sockets.

. Fit the sockets into appropriate positions of the connector block.

. Mount the connector unit, ensuring that there is a good contact between the bare CU-tape and the lower clamp.

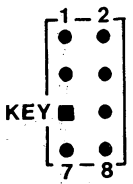
PUC KITS:

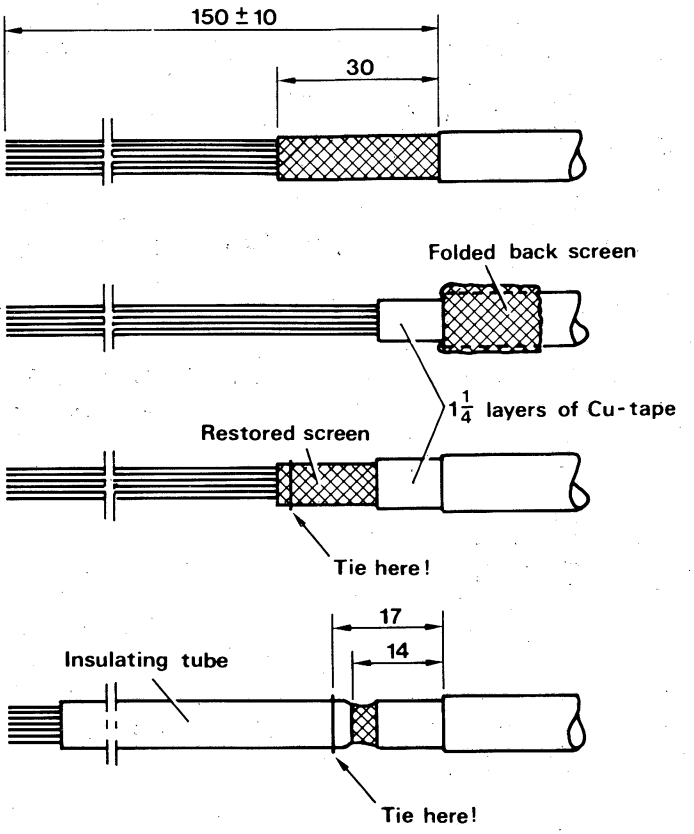
P843-015/01 Kit with 10 PUC I sets: 511 199 52460

P843-016/01 Kit with 5 PUC II sets: 511 199 52450

PUC I is used for thin cables and PUC II for big cables.

Socket seen from wire side





PHILIPS CONNECTOR UNIT

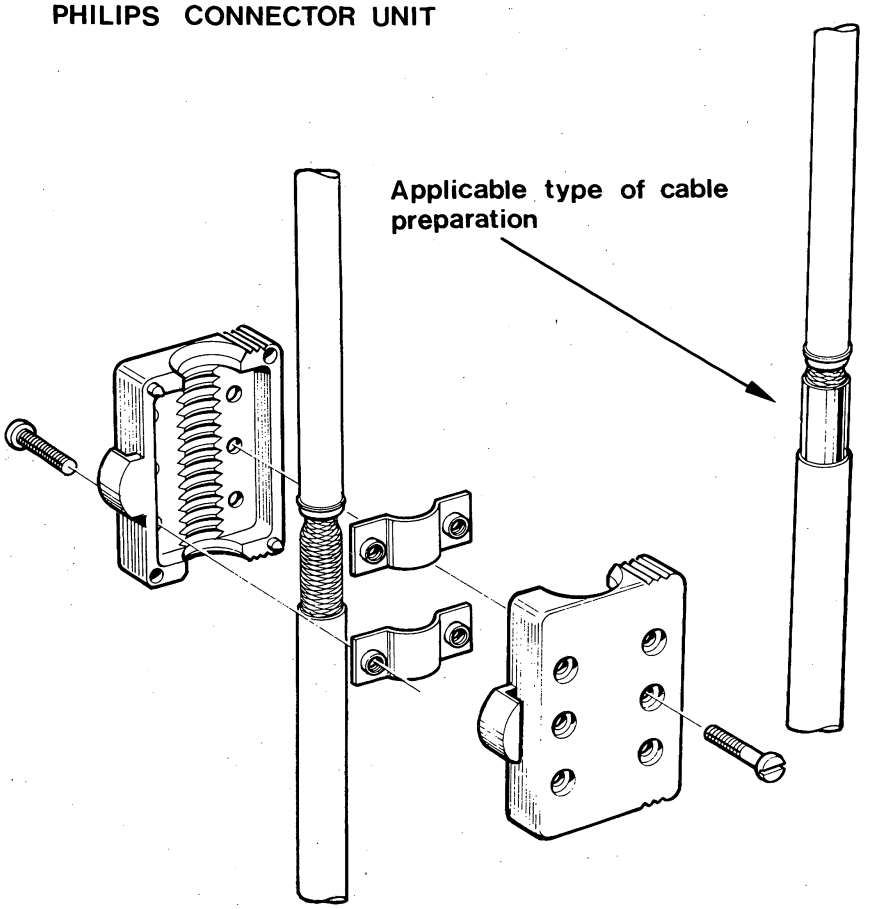


Figure 4.23 PUC KIT WITH BERG CONNECTOR

4.6 INSTALLATION SCHEDULE

You receive:

- pre-wired cabinet
- CPU-box with cards
- devices with cables
- documentation)
- testprogram) to be ordered separately

To be done:

- mount boxes in cabinets according received drawings
- connect remote control, breaks and device cables
- set straps on cards/devices for:
  - interrupt levels and device addresses
  - transfer speed, parity etc.
- connect mains cable
- run testprograms
- fill in the evaluation-form

Note: Normally the system is tested before delivery and so straps and connections are put in a proper working position.

5 TROUBLE SHOOTING

SECTION	5.1	GENERAL	PAGE 5-2
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	5.4	CHECK DEVICE ADDRESS	5-4
	5.5	CHECK BIO LINES	5-4
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5.1 GENERAL

A number of short routines (simple programs) have been added to the various chapters. They can be used if official testprograms give problems or when you want to test only the basic functions of each device or Control Unit.

NAME	CHAPTER	DESCRIPTION
LINE	8,13	Output on Console Typewriter (CTW), or display - V24 CU
ECHO	8,13	Input, Output on Console Typewriter, or display - V24 CU
MEM	10	Memory test, 32K maximum.
DUMP	10	Memory dump on CTW, 32K maximum.
MEM3	10	Memory test, greater than 32KW
MMU2	11	MMU test
WRITE	14	Write Test Pattern on Tape
READ	14	Read Test Pattern from Tape and compare
MTTEST	14	Write and Read all ones on MTCU
ADJF1M	16	Adjust or Check 1M drive on F1MZ
F1SEEK	16	Seek test F1MZ
F1LOOP	16	Write and Read on F1MZ
SEEK	18	Adjust 2.5M or 5M drives X1215/16 on CDDZ
DISCTS	18	Write and Read on CDDZ via IOP
DKPROG	18	Write and Read on CDDZ via Programmed Channel.
LINELP	20	Output on Lineprinter via PC
LPIOP	20	Output on Lineprinter via IOP
CPROGR	20	Read 80 column card into memory via PC
CRTEST	20	Read 80 column card into memory via IOP
ASCU	21	Loop test (output to input check)
ASCU2	21	Input, Output test (input to memory, memory to output)
SALCUT	22	Output test (output to CTW display or oscilloscope)
SALCLA	22	Loop test (output to input and check), asynchronous
SALCLS	22	Loop test (output to input and check) synchronous
HLCUT	23	Output test (output to oscilloscope, data = /FC)
HLCUL	23	Loop test (output to input and check)

Table 5.1 SHORT ROUTINES

5.2 CORRECTIVE MAINTENANCE

The cause of the trouble may be difficult to find because of the great variety, such as:

- Intermittent failures
- Temperature dependant failures
- Software errors
- Design errors (timing e.g.)
- Mains causing problems
- Crosstalk, induction etc.

Philosophy: Card exchange (repair in factory or workshop of the National Organisation).

1. Use your eyes, ears, nose and mouth - ask operator for symptoms.
2. Run microdiagnostic (if possible)
3. Run testprograms: CPU-MEM-I/O devices - terminals
4. Check all strap settings and board locations

If not found:

5. Take out all boards you do not need for the test you are running. Note: PSU must have a min. load of 15%.
6. Load in a few instructions, via hand held panel (if available) with which you can test (instruction by instruction) the system.
   Think of: - straps, U-links on cards and backpanel
   - weak mechanics: fuses, switches, cables, lamps.
7. After repair: run testprograms.

Note: Switch off power before you exchange cards. Bus-transceivers can be blown, which may block the bus.

5.3 CHECK INTERRUPTS

To check if interrupts come in and to verify which level they are, the following small procedures are supplied.
Note: On HHP the switches RTC and LOCK must be off.

Power Failure (level Ø)

1. Depress MCL
2. Connect the bus signal PWFN to ground
3. Depress INST
4. Depress RST
   The 6 ms bits of the displayed word must be zero (i.e. word /ØØ..,/Ø1..,/Ø2.. or /Ø3..)

LKM (level 1)

1. Depress MCL
2. Fill mem address /1ØØ with /28Ø4 (=LKM)
3. Set program counter to /1ØØ
4. Depress INST (2 times)
5. Depress RST
   The 6 ms bits of the displayed wod must be /Ø1 (i.e. word /Ø4..,/Ø5..,/Ø6.. or /Ø7..)

RTC (level 2)

1. Depress MCL
2. Switch RTC on (on HHP)
3. Switch RTC off
4. Depress INST
5. Depress RST
   The 6 ms bits of the displayed word must be /Ø2 (i.e. word /Ø8..,/Ø9..,/ØA.. or /ØB..)

Control Panel Interrupt (level 3)

1. Depress MCL
2. Depress INT
3. Depress INST
4. Depress RST
   The 6 ms bits of the displayed word must be /Ø3 (i.e. word /ØC..,/ØD..,/ØE.. or /ØF..)

I/O Interrupts

- Disc, tape, floppy

1. Depress MCL
2. Load disc pack/tape/diskette
   A ready-interrupt will be generated.
3. Depress INST
4. Depress RST
   The 6 ms bits of the displayed word must contain the expected level. For floppy level 15 = /F the PSW starts with /3C..,/3D..,/3E.. or /3F..

- From other devices

From the short programs on the following pages, key in the program until an INR or OTR instruction is expected. The inhibit instruction (INH) must be replaced by a no-op instruction (=/5700). Execute the program inst-by-inst until I/O or a status interrupt is expected. The program counter displayed on the HHP will show the jump. Now depress RST. The 6 most significant bits of the PSW indicate the interrupt level.

5.4 CHECK DEVICE ADDRESS

To check the device address whether it is available or not, use the following procedure:

1. Fill mem address /1ØØ with CIO halt:
   'Ø1ØØ ØØØ1 1Ø.. ....', where the 6 ls bits contain the device address.
2. Set program counter to /1ØØ
3. Depress MCL, INST
4. Depress RST
   Bit 6 and 7 of the displayed word must be 'Ø Ø' (i.e. word /.Ø..,/.4..,/.8.. or /.C..)
   Bit 6 and 7: '1 1' = address unknown
   'Ø 1' = not accepted
   'Ø Ø' = accepted

5.5. CHECK BIO LINES

To check the BIO lines, the LM function of the FRCP or HHP-panel can be used:

1. Load an excisting memory address, Address + LA on FRCP or LR (reg. A0) on HHP.
2. Load /5555, Data + LM
3. Load /AAAA, Data + LM

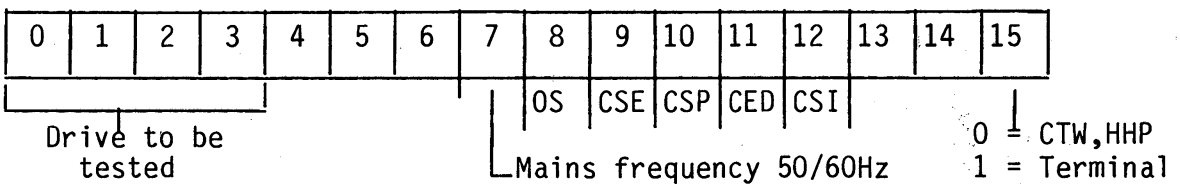
If a short circuit is present, the /5555 or /AAAA will be displayed incorrectly, showing the bit(s) in error.

Note: In the P876 the LR with LM from HHP is not accepted by CP2B and 0,LR with 0,LM must be used (uppercase mode of HHP).

5.6 TEST PROGRAMS

- Program names starting with B.. are original P8ØØ versions. System parameters can be changed by Hand Held Panel. Console Type-Writer may be used.
- Program names starting with T.. are adapted program versions for PTS. In this case, the system parameters can be changed on a terminal keyboard. Register A9 bit 15 = Ø indicates the program that output is on CTW (or no output),
  15 = 1 indicates the program that output is on a terminal.
- As only loading procedure and initial parameter setting are different, the P800 testprogram description is also used for PTS programs.

Testprogram Control - Selection with register A9.



Bit 0 = 1 Drive 0
Bit 1 = 1 Drive 1
Bit 2 = 1 Drive 2
Bit 3 = 1 Drive 3

- "One Shot" (OS)
  Bit 08 = 1: Stop in /5E0 (hexa) after the running of each check, before going to the next one. All there is to be done is depress the RUN button to carry on. PTS systems: depress SOP switch 9.

- "Clear Stop on Error" (CSE)
  Bit 09 = 1: Suppress the stop in /5F0 (hexa) in case of an error.

- "Clear Stop on Program" (CSP)
  Bit 10 = 1: Suppress the stop in /700 (hexa) after the program has been executed (loop again on test).

- "Clear Edition" (CED)
  Bit 11 = 1: Suppress the printing out of error and information messages:
  CSI at 0: stop in /5E0: Information code in A1.
  CSE at 0: stop in /5F0: Error code in A1.

- "Clear Stop on Information" (CSI)
  Bit 12 = 1: Suppress the stop in /5E0 (hexa).

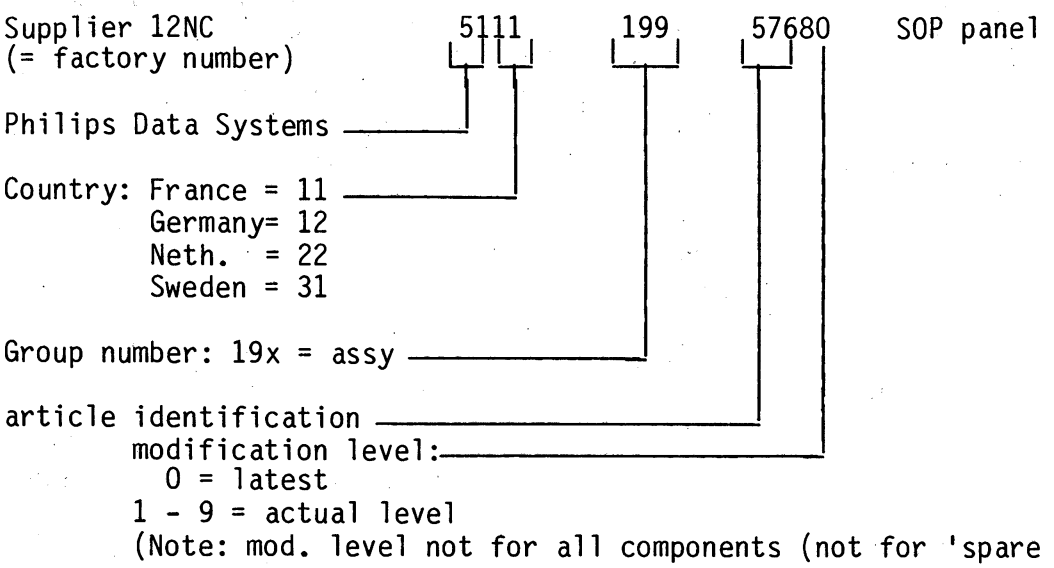
- Main frequency
  Bit 7 = 0: 50Hz
  Bit 7 = 1: 60Hz
  In case of 50Hz, it is possible to set bit 7=1 that will increase by 20% all delays. This permits to determine if the problem is due to a critical timing or a real fault.

To run the testprograms refer to Short Description Testprograms in each chapter.

5.7 12NC NUMBERS

- All parts, used in the Philips organisation are identified by 12NC numbers.

Example:



In this example, the assy consists of sub-assemblies and separate components.
Such as:

2422	128	01772	Push button switch

- Most components have a 'spare part number' and can be ordered from Concern Service.

All 'spare part' (or 'service' numbers begin with code 4822 ... . or 5322 ... .

example:

5322 214 45246	SOP panel	(= 5111 199 57680)
5322 276 14353	Push button switch	(= 2422 128 01772)

6 CONTROL PANELS

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	6.3	TRANSMISSION CODES FRCP	6-4
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6.1 INTRODUCTION FRCP (FIGURE 6.1)

The FRCP provides the controls and indicators that enable a user to operate and monitor the system. The pushbuttons are in two groups: the left-side group is used to select system functions; the right-side group to select hexadecimal address and data digits. The left-side indicator is mainly used to display memory and register addresses, the right-side indicator to display memory and register data. The FRCP is intended for P874/876 computer systems.

6.1.1 IDENTIFICATIONS

The FRCP is available as P843-510/03 (5111 199 59670), mounted on a 4U Front Panel.
Included is also a Kit with small cover-plates.
One of the cover plates can be fitted to the Front-Panel, depending on the system type.

6.1.2 TECHNICAL DATA

PERFORMANCE DATA

Serial Data Interface: V24/28: Transmission Rate = 4.8K baud
Logic Levels : logical 0 = +12V
: logical 1 = -12V

POWER REQUIREMENTS

Voltage	: +5V ± 0.25V	+12V ± 1.2V	-12V ±1.2V
Current (max.)	: 800mA	150mA	20mA

6.2 INTERFACE CONNECTOR FRCP/HHP

Pin No.	Signal	Function
J1-1	LOCK	When LOCK = 1, FRCP is inhibited except for INT
2	SDMP	Serial Data Master to Panel
3	OV(GND)	
4	+5V	
5	+12V	Logic level 0 of serial data
6	SDPM	Serial Data Panel to Master
7	RTCE	Real Time Clock Enable (active at "1")
8	RESETN	Reset Not
9	-12V	Logic level 1 of serial data

Table 6.1 INTERFACE CONNECTOR FRCP/HHP

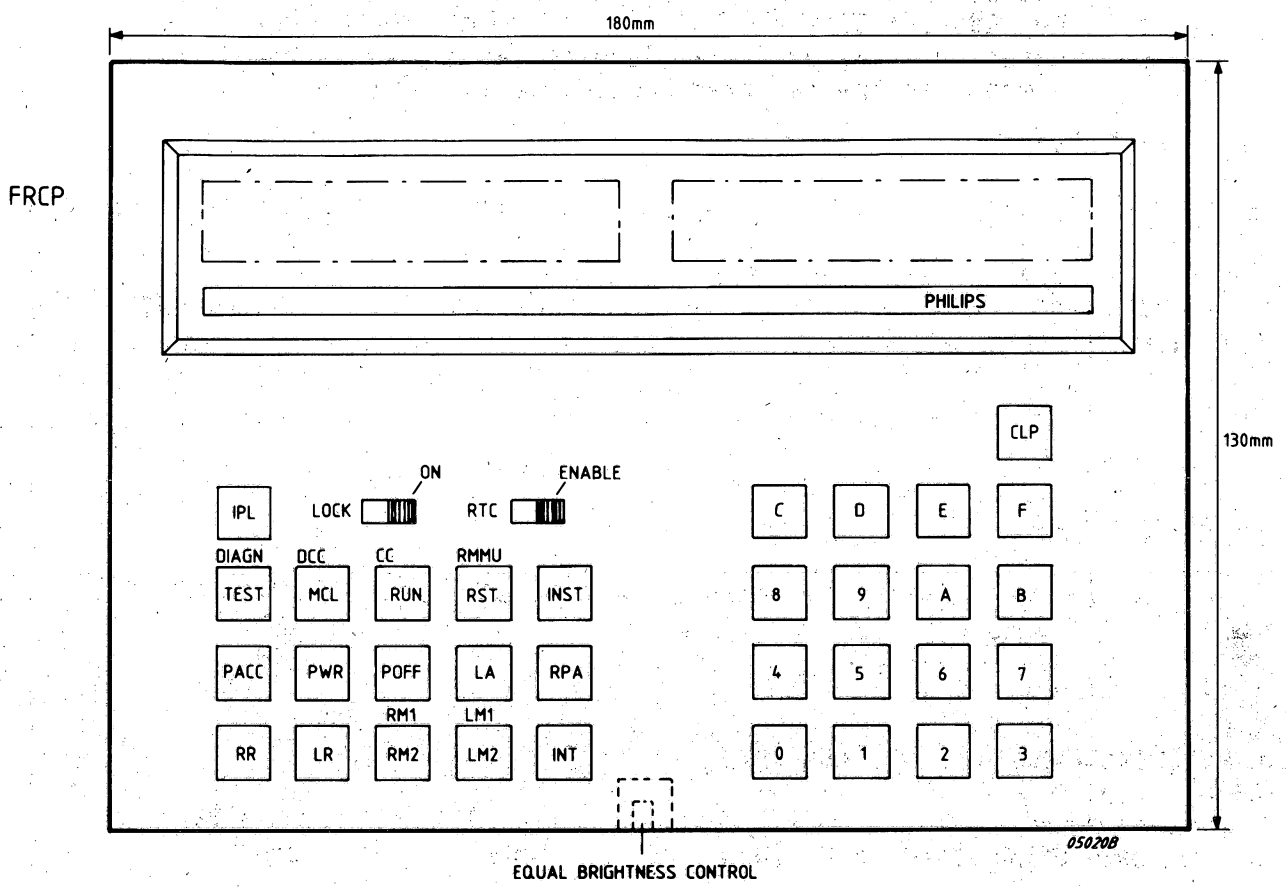


Figure 6.1 FRONT VIEW OF FRCP

SWITCH SELECTION:	HEXADECIMAL CODE:
0 to F	Address: / Bx Bx Bx Bx Bx (leading zeros are not keyed in) Reg Addr. / 3x Data: / 3x 3x 3x 3x (leading zeros are not keyed in) where x is the selected hex. digit in the range 0 to F.
MCL	/40
LR	/41
RR	/42
RST	/43
IPL	/44
LM(1)	/45
LM(2)	/55
INT	/46
RM(1)	/47
RM(2)	/57
LA	/48
INST	/49
RPA	/4A
RUN	/4B
PACC	/4C
PWR	/4D
POFF	/4F
TEST	/4E
0+RST	/5A)
0+RUN	/5C)- (only for P876)
0+MCL	/5D)
Serial Data Panel-to-Master Codes	

Table 6.2 SDPM CODES FRCP

FUNCTION NAME	FUNCTION	HEXADECIMAL CODE
RUNZO	CPU mode changed from RUN to IDLE	/40
RUNZ1	CPU mode changed from IDLE to RUN	/41
TEST	Production testing only	/42

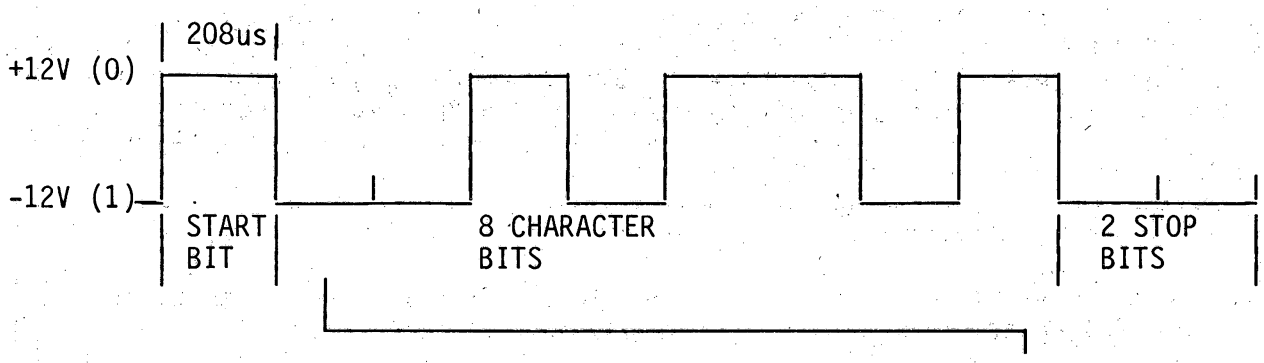
Table 6.3 SDMP CODES

Note: To distinguish between master-to-panel data and hand-entered data, the display of master -to-panel data is preceded by two small zeros e.g.: oo 1625.
When the preset stop-on-address function is operative, the display of master-to-panel data is preceded by 'P' and one small zero e.g.: Po 1625.

HEXADECIMAL CODE FORMAT

1 start bit, 8 character bits, 2 stop bits

EXAMPLE:



CHARACTER 'RUN' = $0100/1011_2$

= $4\ B_{16}$

Note that the least significant bit is transmitted first.

6.4 FUNCTIONS FRCP

The FRCP consists of a microcomputer and switch matrix which operate together to generate serial function and data codes for onward transmission to the CPU. The address and data displays can be energized with the appropriate information, via buffers, registers etc. The FRCP can also receive information from the CPU.

A 40KHz oscillator is used to derive an a.c. drive for the display filaments. The oscillator output is also used to derive a +24V d.c. supply, and a +5V supply (necessary if the line voltage of the remote version is less than +5V).

SWITCH	FUNCTION
0 to F	To select hexadecimal address and data digits.
LOCK	When this switch is pushed rightward, all FRCP functions except INT are inhibited. The automatic restarting facility is enabled.
RTCE	When this switch is pushed rightward, the system Real Time Clock is enabled.
CLD	Clears ADDRESS and DATA displays to all zeros.
IPL	Initial Program Loader: An initial bootstrap program that is located in a hardware read-only-memory is loaded into memory word locations 000 to 255.
TEST	When this switch is operated at the same time as the '0' switch and provided the system microdiagnostic routine is loaded, the CPU will execute the system microdiagnostic routine. When it is operated alone all the segments of the ADDRESS and DATA displays will be lit.
MCL	Master Clear: Clears or resets most hardware logic. Usually activates the bus CLEARN signal.
RUN	Sets the CPU to RUN mode and inhibits all FRCP functions except INST and INT. The word 'run' in small letters is displayed on the DATA display. If the Stop On Preset Address option is being used the letter 'P' will be displayed as the extreme right-hand character of the DATA display. The preset stop address will be displayed on the ADDRESS display.
RST	Read Status: The contents of the program status word are displayed on the DATA display.
INST	Instruction Step: Each time INST is pressed, the CPU performs the one instruction indicated by the program counter and then halts.
PACC	Preset Access: Stop when any memory operation accesses the address that was keyed in before selecting the PACC function.
PWR	Preset Write: Stop when a write memory operation accesses the address that was keyed in before selecting the PWR function.
POFF	Inhibit the preset-stop-on-address function.

Note: The preset-stop-on-address function is optional and is not available on some systems

Table 6.4 CONTROL PANEL SWITCHES FRCP

SWITCH	FUNCTION
LA	Load Address: When this switch is operated, the keyed-in address code is loaded into the Memory Address Register and will be displayed on the ADDRESS display. This address is incremented by successive RM or LM operations.
RPA	Read Preset Address: When this switch is operated, and provided the CPU is in IDLE mode, the preset address will be displayed on the ADDRESS display. When the CPU is in the RUN mode, the INST button should be pressed followed by the RPA button. The RUN button must be pressed to restart the program.
RR	Read Register: When this switch is operated, the keyed-in register no. is displayed on the ADDRESS display and the contents of the register is displayed on the DATA display.
LR	Load Register: When this switch is operated, the keyed-in data is displayed on the DATA display.
RM(1)	Read Memory: When this switch is operated with the '0' switch, the address pointed to by the program counter A0 is displayed on the ADDRESS display and the contents of the address is displayed on the DATA display.
RM(2)	Read Memory: When this switch is operated alone, the contents of the address pointed to by the Memory Address Register is displayed on the DATA display and the memory address +2 is displayed on the ADDRESS display. To read sequential memory locations RM is pushed as required.
LM(1)	Load Memory: When this switch is operated with the '0' switch, the address pointed to by the program counter A0 is displayed on the ADDRESS display and is loaded with the data that is displayed on the DATA display.
LM(2)	Load Memory: When this switch is operated alone, the memory address pointed to by the Memory Address Register and that is displayed on the ADDRESS display is loaded with the data that is displayed on the DATA display and the address is incremented by 2.
INT	Interrupt: When this switch is operated, the FRCP generates an operator's interrupt.
Note:	To distinguish between master-to-panel data and hand-entered data, the display of master-to-panel data is preceded by two small zeros e.g. oo 1625. When the preset-on-address function is operative, the display of master-to-panel data is preceded by 'P' and one small zero, e.g. Po 1625.

Table 6.4 CONTROL PANEL SWITCHES FRCP (CONT'D)

6.5 INTRODUCTION HHP (FIGURE 6.5)

The HHP is a hand held control panel enabling the user to communicate with the P871, P874, P876 computer systems. The panel has similar facilities to the Full Control Panel. Data keys are code '0' - 'F' and the visual display shows 4 hexadecimal digits. The panel is designed around an eight-bit microprocessor 8048 which performs all the major logic functions. These are:

. Reading the keyboard
. Displaying data
. Transmitting and receiving data or address and from the CPU

The asynchronous serial interface with the CPU complies with CCITT (V24) requirements. Successive characters of data/function are transmitted in the form: 1 start bit/8 data bits/2 stop bits.

6.5.1 IDENTIFICATIONS

P843-500/01	HHP	5111 199 69160
P843-501/03	4U-PANEL FOR HHP	5111 199 59660
	Kit with small COVER PLATES	5111 199 59440

Cables:

P843-550/01	Cable HHP-FRONT PANEL (7M)	5111 199 67720
P843-551/01	Cable HHP-FRONT PANEL (3M)	5111 199 67700
P843-552/01	Cable HHP-CPU	5111 199 65410

6.5.2 TECHNICAL DATA

PERFORMANCE DATA

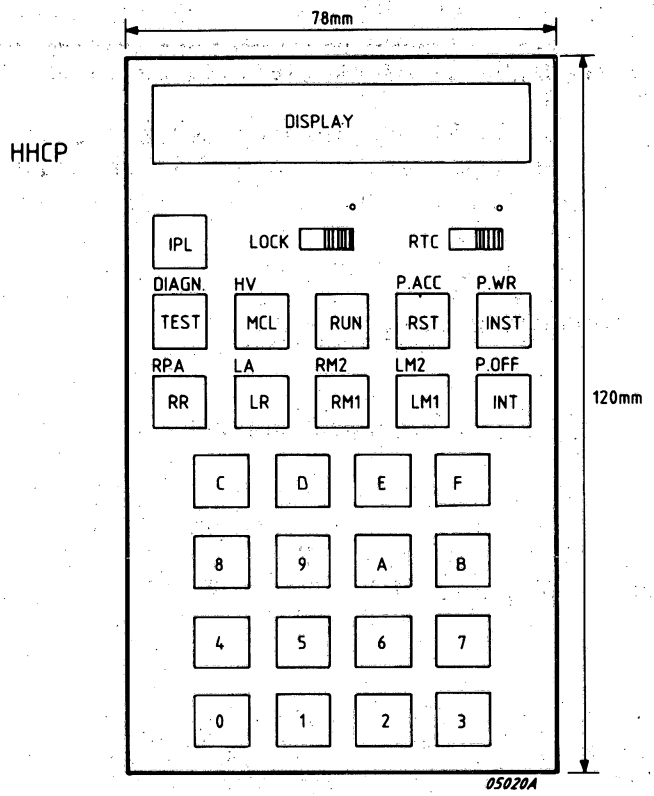
Serial Data Interface: V24/V28: Transmission Rate = 4.8k baud
Logic Levels : logical 0 = +12V
: logical 1 = -12V

POWER REQUIREMENTS

Voltage	: +5V ± 0.25V	+12V ± 1.2V	-12V ± 1.2V
Current (max.)	: 500mA	170mA	23mA

INTERFACE CONNECTOR HHP

For description of interface refer to FRCP, which has exactly the same interface.



MCL	Master Clear	(MCL)	HV	High order digit visualisation
RTC	Enables Real Time Clock			
LOCK	Select Automatic Restart in case of power failure and lock all function buttons except INT.			
RUN	Start CPU			
INST	Execute next instruction only	(INST)	PWRITE	Preset Write
TEST	Test display	(TEST)	TEST	Initiate Diagnostic Test
RST	Read Program Statklus Word	(RST)	PACCESS	Preset Access (address
INT	Initiate Control Panel Interrupt	(INT	POFF	Preset Off
IPL	Initiate Program Load Routine			
LM	Load Memory (pointed by A0)	(LM)	LM2	Load Mem. (pointed by MAR)
LR	Load Register	(LR)	LA	Load Mem. Address reg.
RM	Read memory (pointed by A0)	(RM)	RM2	Read Mem. (pointed by MAR)
RR	Read Register	(RR)	RPA	Read preset Address
0-F	16 Data Keys	(....) : Hold datakey 0 down while pressing function....		

Figure 6.2 FRONT VIEW OF HHP

SWITCH SELECTION:	HEXADECIMAL CODE:
0 to F	Address: / Bx Bx Bx Bx Bx (leading zeros are not keyed in) Reg Addr. / 3x Data: / 3x 3x 3x 3x (leading zeros are not keyed in) where x is the selected hex. digit in the range 0 to F.
MCL	/40
LR	/41
RR	/42
RST	/43
IPL	/44
LM(1)	/45
LM(2)	/55
INT	/46
RM(1)	/47
RM(2)	/57
LA	/48
INST	/49
RPA	/4A
RUN	/4B
PACC	/4C
PWR	/4D
POFF	/4F
TEST	/4E
Serial Data Panel-to-Master Codes	

Table 6.5 SDPM CODES HHP

Note: For SDMP-CODES refer to description of FRCP.

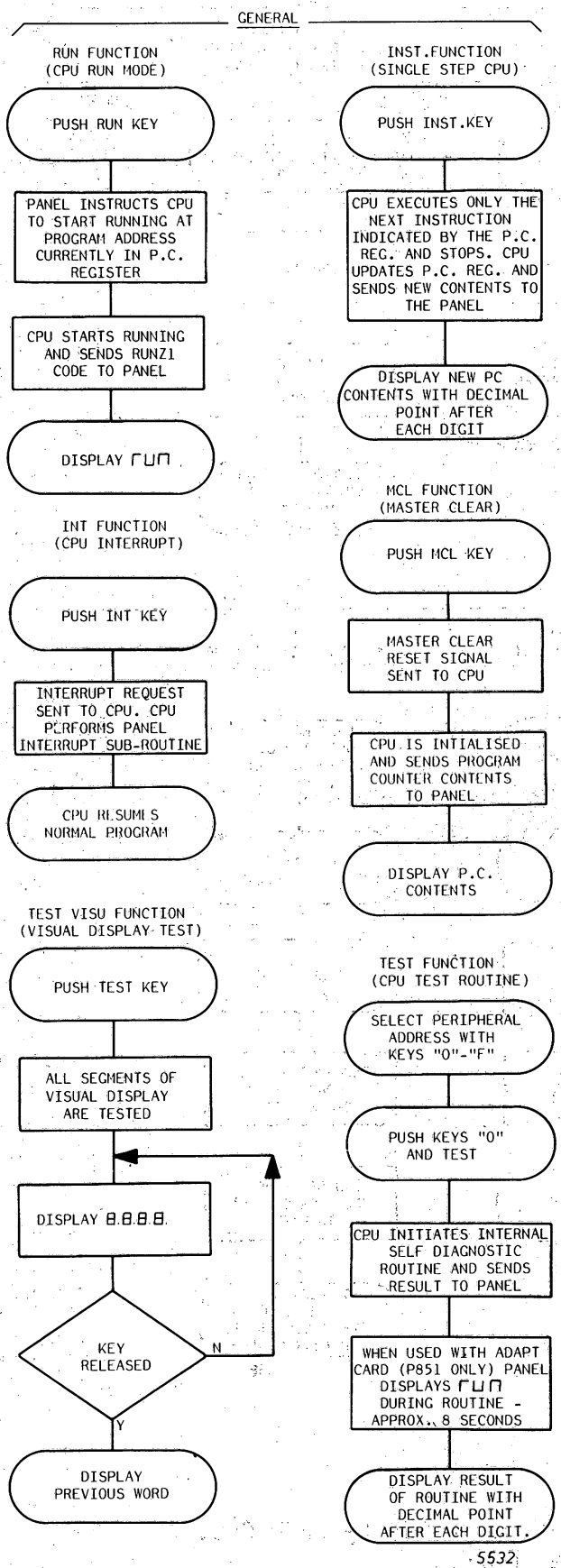
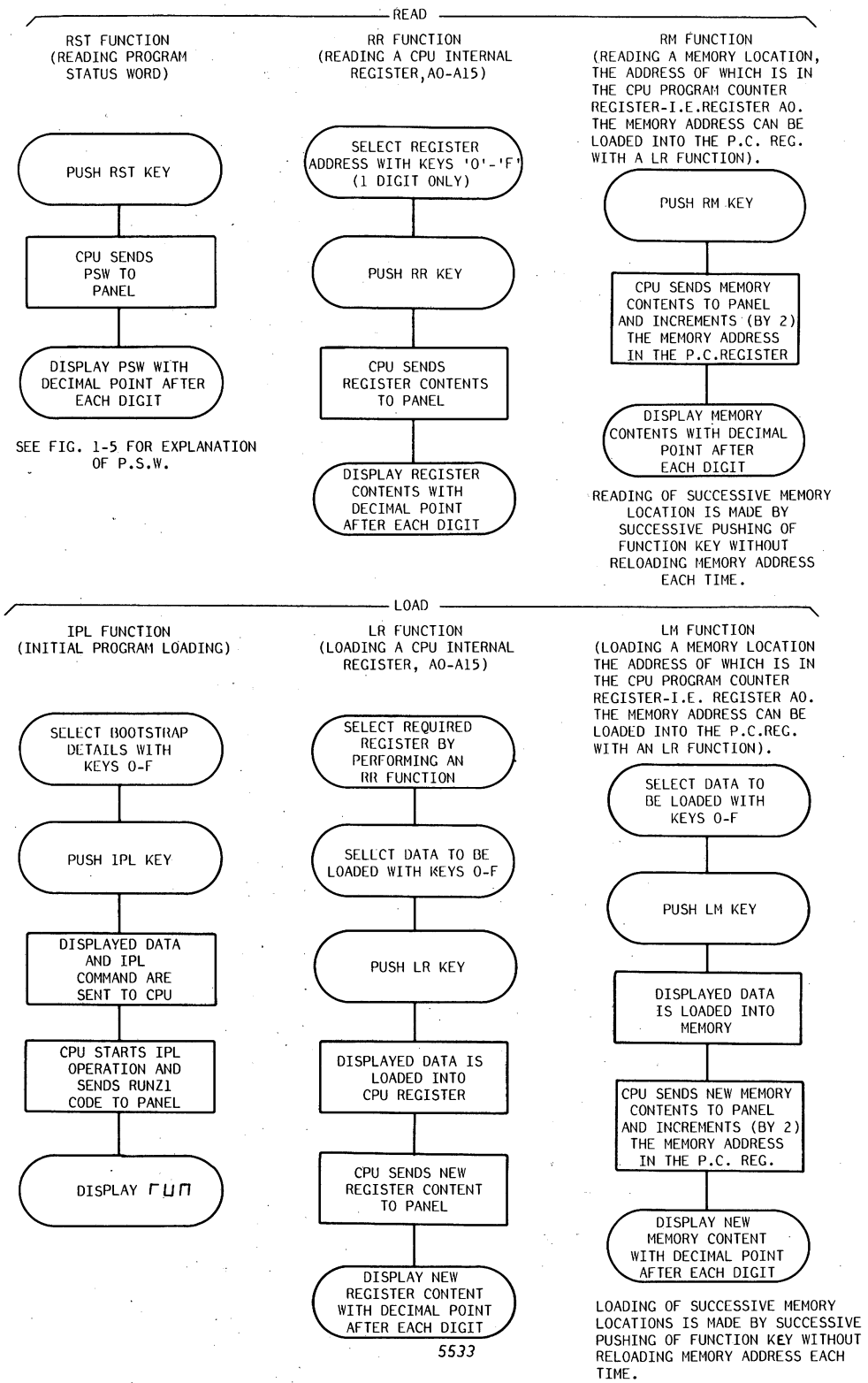


Figure 6.3 H.H.P. FUNCTIONS COMMON TO ALL CPU'S



Note: RM and LM are not accepted by CP2B CPU.
Refer to chapter P876.

Figure 6.3 H.H.P. FUNCTIONS COMMON TO ALL CPU'S (CONT'D)

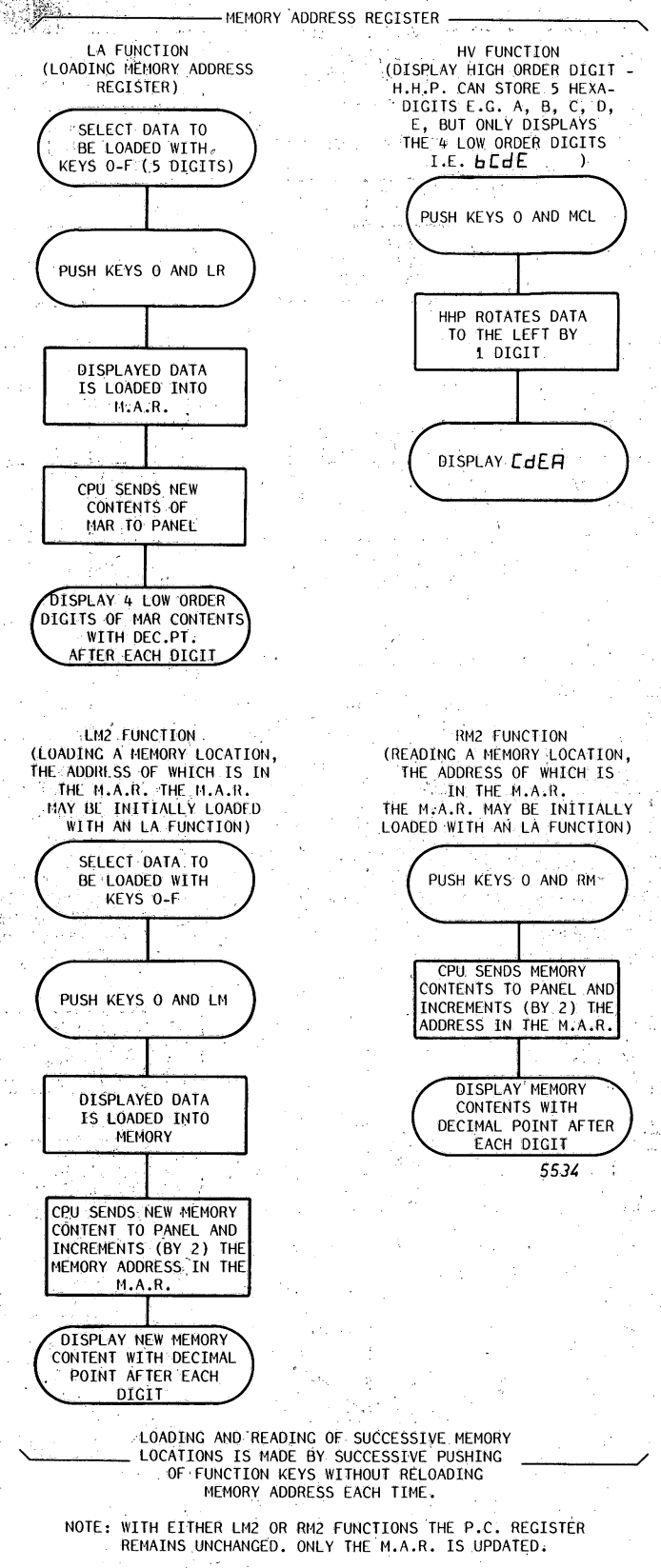


Figure 6.4 H.H.P. EXTENSION FUNCTIONS WITH P874/876

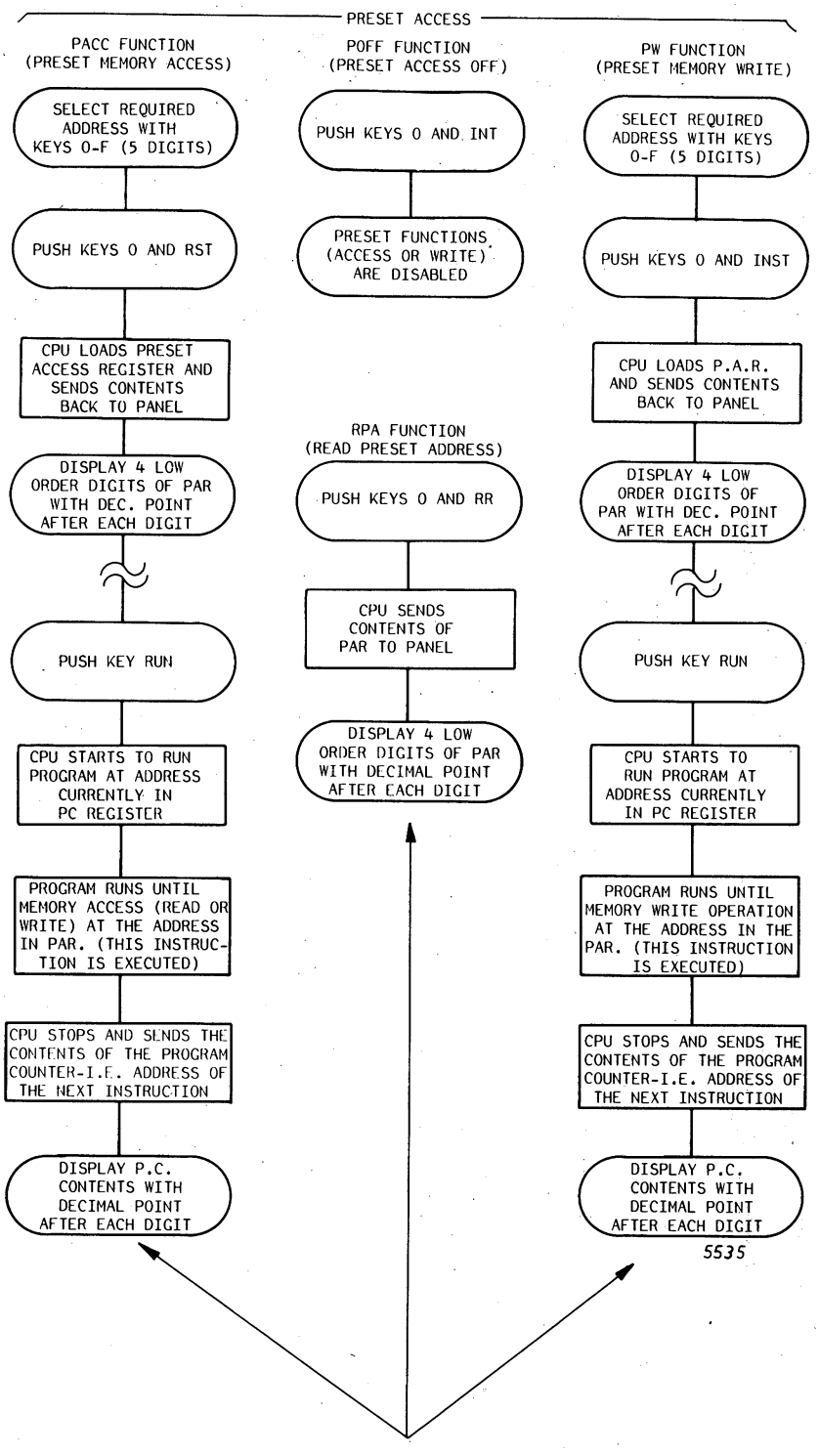


Figure 6.4 H.H.P. EXTENSION FUNCTIONS WITH P874/876 CPU (CONT'D)

6.8 HAND HELD PANEL CABLES

Connection HHCP - CPU

SIGNAL NAME	BERG CONNECTOR	CANNON CONNECTOR	REMARKS
SDPM	A01	6	┐ coax shield
GND	B03	3	┘
LOCK	B01	1	
RTCE	A02	7	
+12V	B05	5	
+5V	B04	4	
-12V	A04	9	
SDMP	B02	2	┐ pair
GND	B03	3	┘
RESETN	A03	8	┐ coax shield
GND	B03	3	┘
SHIELD	At each end: 10 cm wire equipped with a lug		
2m HHCP/C7E2 cable 5111 199 65410			

Connection HHCP-Connector panel

SIGNAL NAME	FEMALE CONNECTOR DE9S	MALE CONNECTOR DE9P	REMARKS
+5V	4	4	2 wires of a pair
+12V	5	5	
-12V	9	9	
RTC	7	7	
LOCK	1	1	
RDV	2	2	┐ pair
GND	3	3	┘
TDV	6	6	┐ coax shield
GND	3	3	┘
RSL	8	8	coax
SHIELD	At each end: 10cm wire equipped with a lug		
3m HHCP extra cable 5111 199 67700 7m HHCP extra cable 5111 199 67720			

Table 6.6 HAND HELD PANEL CABLES

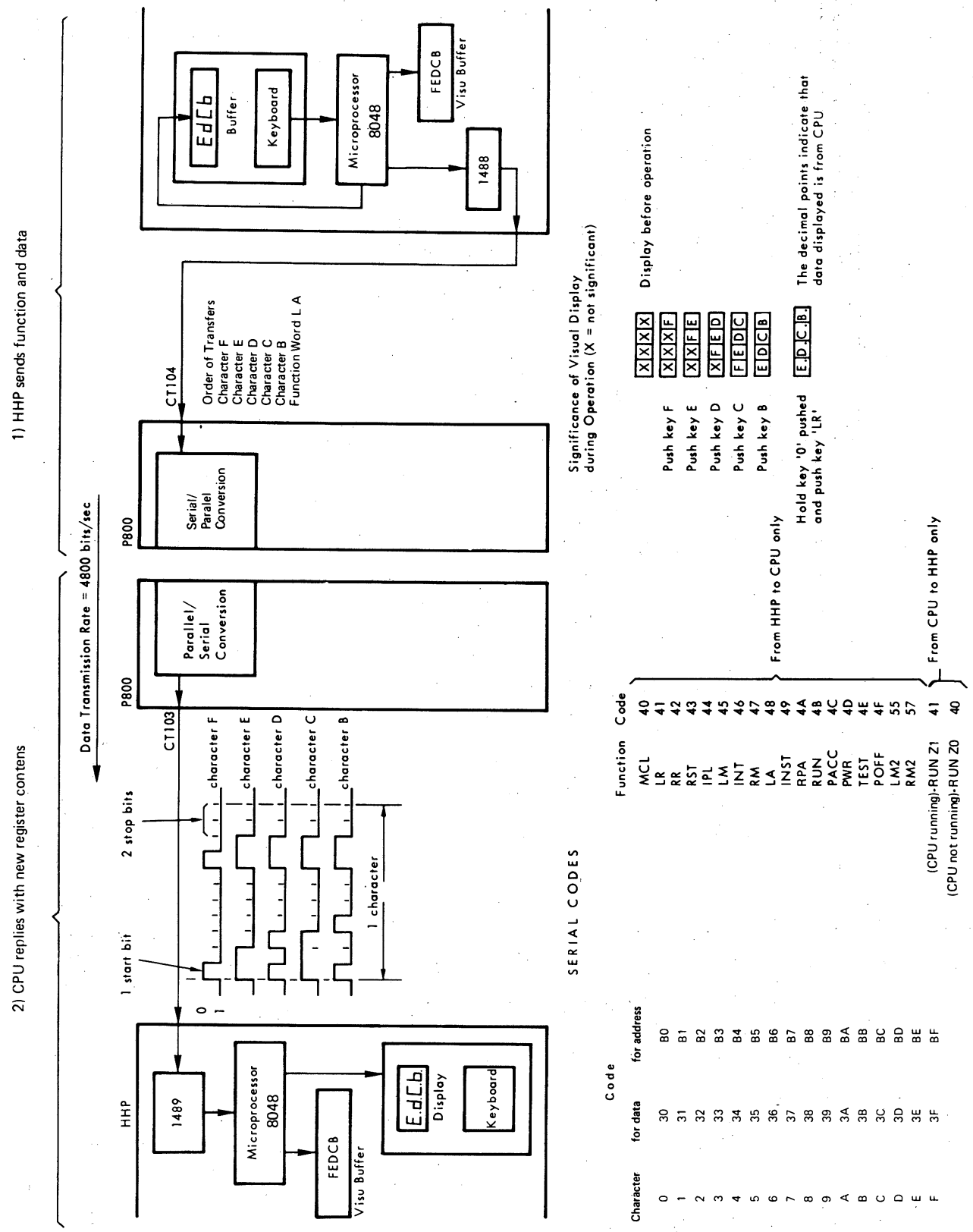


Figure 6.5 EXAMPLE OF INPUT/OUTPUT SEQUENCE - LOADING MEMORY ADDRESS REGISTER WITH CODE FEDCB

7 P871 CPU (CP1BF)

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7.1 P871 CPU IDENTIFICATIONS

Type No: P871-300 (RA12F rack)

Test Programs CPU - CP1/2B
- MMU2B
- PAF2B

Power consumption:

	+5VL	+12VL	-12VL
CP1BF	3.0A	0.02A	0.02A

12NC code on the sticker of the board:

CP1BF 5111 199 5939x (5322 216 21296)

x = modification level

7.2 INSTALLATION

7.2.1 STRAP SETTINGS (FIGURE 7.1)

Before the card is plugged into the rack, the position of the U-links should be checked to see that they comply with the requirements of the system.

SELECTION OF INPUT DEVICE (S9 - S12)

These four U-links enable the selection of the device used during a Remote IPL or Auto-IPL.
If the INCOD lines are controlled by an Operator Panel, these U-links must be in position 1. Shown: Bootstrap address /1F4 selected.

ms ——— ls

U-link No.:

Example:
/5 selected

3	2	1	0	Bootstrap Word	
INCOD3	INCOD2	INCOD1	INCOD0	Hex-Dec.	
0	0	0	0	/1FE	255
0	0	0	1	1FC	254
0	0	1	0	1FA	253
0	0	1	1	1F8	252
0	1	0	0	1F6	251
0	1	0	1	1F4	250
0	1	1	0	1F2	249
0	1	1	1	1F0	248
1	0	0	0	1EE	247
1	0	0	1	1EC	246
1	0	1	0	1EA	245
1	0	1	1	1E8	244
1	1	0	0	1E6	243
1	1	0	1	1E4	242
1	1	1	0	1E2	241
1	1	1	1	1E0	240

Table 7.1 SELECT IPL DEVICE

The contents of the selected word is loaded in CPU register A15 under control of the CPU microprogram.

SELECTION OF BUS TYPE (S07)

This U-link will be in the position P851 mode when a Memory or a P851 CU is present in the configuration, otherwise it will be in the UPL position. Shown: 851 position selected.

SELECTION OF CO-PROCESSOR PRESENCE (S16)

This U-link will be in the ABS position if no co-processor is present in the configuration, otherwise it will be in the other position. Shown: co-processor absent selected.

U-links for (factory) test only:

S1	enable oscillator
S2	enable INCLA (source for INCL)
S3,4	enable oscillator flip-flop
S5	enable clock to FASTR
S6	enable clock to MUM
S8	enable decoders for Firmware mode
S13,14	enable address buffers
S15	enable RDCPIN
S17	enable select INT3N
S18	enable REQCL of BUSLSI

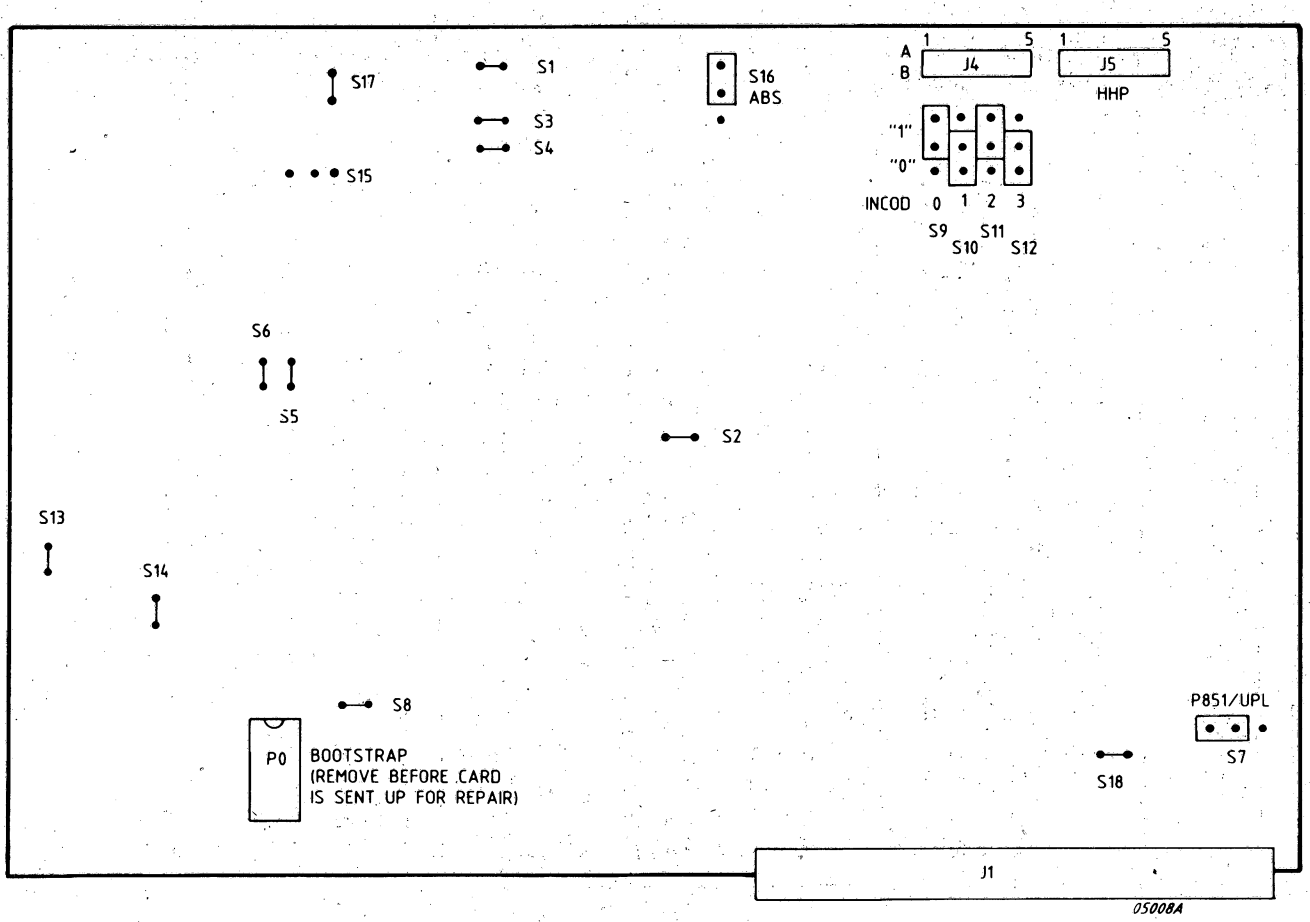


Figure 7.1 CP1BF U-LINKS

7.2.2 CONFIGURATION RULES

- The CP1BF is the Central Instruction Processor in the P871-300 Basic System and must be fitted in slot 1 of the card rack.
- Other Masters follow in the order of their system priority, determined by OKO-OKI links.
- The FPPE can not be used with CP1BF
- The UPL-Bus must not be extended out of the basic Eurorack without the signals being terminated.
- The recommended card location for TUGP is 12.
- A hardware facility is present to connect a Co-Processor e.g. for execution of of floating Point instructions.

7.3 INTERFACES

7.3.1. INTERFACE SIGNALS AND PINS

Note that the principe of numbering the connectors and their pin positions start from connector 1 pin 1 and continues in a clockwise direction around the card.

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01	+12VL	1B01	ERQN	1A01	-12VL
1C02		1B02	BUSRN	1A02	
1C03	BCI	1B03	MSN	1A03	INCL
1C04	*IRAIN	1B04	OV	1A04	*IRALN
1C05	*IRAKN	1B05	BSYN	1A05	*IRAMN
1C06	OV	1B06	OKO	1A06	OV
1C07	PWFN	1B07	* RUNN	1A07	RSLN
1C08	CLEARN	1B08	RTCN	1A08	ACN
1C09	OV	1B09	BAWOFN	1A09	OV
1C10	TMPN	1B10	STOPN	1A10	TSMN
1C11	TMEN	1B11	OV	1A11	TMRN
1C12	OV	1B12	**MADE0	1A12	OV
1C13	MAD00	1B13	**MADE1	1A13	MAD01
1C14	MAD02	1B14	OV	1A14	MAD03
1C15	MAD04	1B15	**MADE2	1A15	MAD05
1C16	MAD06	1B16	**MADE3	1A16	MAD07
1C17	MAD08	1B17	MADE4	1A17	MAD09
1C18	MAD10	1B18	MADE5	1A18	MAD11
1C19	MAD12	1B19	MADE6	1A19	MAD13
1C20	MAD14	1B20	MADE7	1A20	MAD15
1C21	CHA	1B21	OV	1A21	WRITE
1C22	OV	1B22	*IRAAN	1A22	OV
1C23	BIO08N	1B23	*IRABN	1A23	BIO00N
1C24	BIO09N	1B24	*IRACN	1A24	BIO01N
1C25	BIO10N	1B25	*IRADN	1A25	BIO02N
1C26	BIO11N	1B26	OV	1A26	BIO03N
1C27	BIO12N	1B27	*IRAEN	1A27	BIO04N
1C28	BIO13N	1B28	*IRAFN	1A28	BIO05N
1C29	BIO14N	1B29	*IRAGN	1A29	BIO06N
1C30	BIO15N	1B30	*IRAHN	1A30	BIO07N
1C31		1B31	+5VL	1A31	
1C32	+5VL	1B32	+5VL	1A32	+5VL

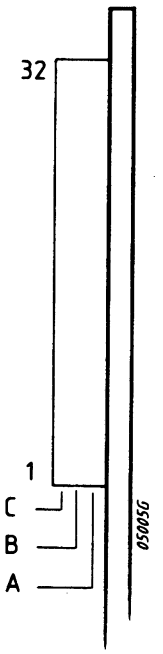
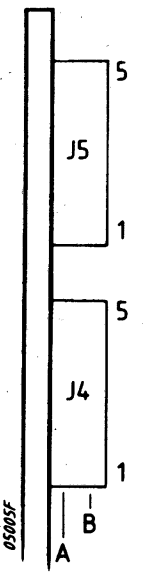


Table 7.2 UPL-BUS CONNECTOR PINNING

* These signals are not connected to the back panel bus.
** MADE0 to 3 have the value 0 when the MAD lines are validated by CP1BF

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
5A01	SDPM (V28)	5B01	LOCK (TTL)
5A02	RTCE (TTL)	5B02	SDMP (V28)
5A03	RESETN (TTL)	5B03	GND
5A04	-12V	5B04	+ 5V
5A05	DUMMY PIN	5B05	+12V

Table 7.3 CONTROL PANEL CONNECTOR PINNING



PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
4A01	INCOD1	4B01	INCOD0
4A02	INCOD3	4B02	INCOD2
4A03		4B03	
4A04	RTCE	4B04	GND
4A05		4B05	LOCK

Note: For INCOD connection, the corresponding U-links must be in the '1'-position.

Table 7.4 LIMITED OPERATOR PANEL CONNECTOR PINNING

Extended Panel:
An Extended Panel (HHP or FRCP) can be connected via J5. Note that a cable with a Berg connector at the CPU side must be applied. The "Extended Panel" should not be connected or disconnected from the CP1BF under power, as the CP1BF may get blocked.

Limited Operator Panel:
A limited Operator Panel can be connected via J4. Note that for IPL either the CP1BF signal "RUNN" at 1B07 must be activated, or power must be switched-on with "LOCK" (at 5B01) and "BAWOFN" (at 1B09) active.

7.3.2 INTERCONNECTIONS

The System Interconnections to be made are:
- Interrupt lines (IRAAN-IRAMN, level 4-15)
- OKO/OKI to the other masters.
  Interconnections are printed wiring on the backpanel from 1BO6 to 1BO7 of all card positions.

INTERRUPT WIRING (See also table 7.2)

Level	Connected	FROM		TO CP1BF
0	Power Failure	(RIT /17)	-	fixed
1	Progr.Int. (LKM, Stack Overflow)	(RIT /1D)	-	fixed
2	Real Time Clock	(RIT /1B)	-	fixed
3	Control Panel (HHP/FRCP)	(RIT /OF)	-	fixed
4	HLVCUZ rec (example)	1CO4		1B22
5	HLVCUZ trx	1CO5		1B23
6	.....	....		1B24
7	.....	....		1B25
8	.....	....		1B27
9	.....	....		1B28
10	.....	....		1B29
11	.....	....		1B30
12	.....	....		1C04
13	.....	....		1C05
14	.....	....		1A04
15	.....	....		1A05
16	.....	(1B03)	BCI	(1B03)
17	.....		BCI	
18	.....		BCI	
19	.....		BCI	
20	.....		BCI	
21	.....		BCI	
22	.....		BCI	
23	.....		BCI	
24	.....		BCI	
25	.....		BCI	
26	.....		BCI	
27	.....		BCI	
28	.....		BCI	
29	.....		BCI	
30	.....		BCI	
31	.....		BCI	
etc.			etc.	
60				

Table 7.5 INTERRUPT WIRING

7.4 FUNCTIONAL BLOCKDIAGRAM (Figure 7.2)

Connection to other elements of the system is made via the UPL-BUS.

The microprocessor FASTB takes care of program execution. The scratchpad (SPAD) registers A1 up until A14 are for general purpose use.
A15 is the dedicated stackpointer and A0 is the program counter.

The FIRMWARE ROM contains a microprogram extension for handling of control panel functions, microdiagnostics, auto restart, IPL, etc.
The firmware, program is started when the FASTB receives a special, internal interrupt called CPIN. FASTB switches to firmware mode and selects the firmware memory.
Firmware instructions are written in normal P800 machine code. Note that some special instructions (store, read and return from firmware) are reserved for firmware mode only.

The BOOTSTRAP ROM, necessary for Inital Program Load contains a program, which depends on the application.

Example: P800 system : (P)ROM 4063
PTS6900 system : (P)ROM 5514

INCODE is the circuit, which selects a code, either from the U-links on the CP1BF or from an external thumbwheel switch, connected to J4, which can be used by the Bootstrap for IPL device selection.

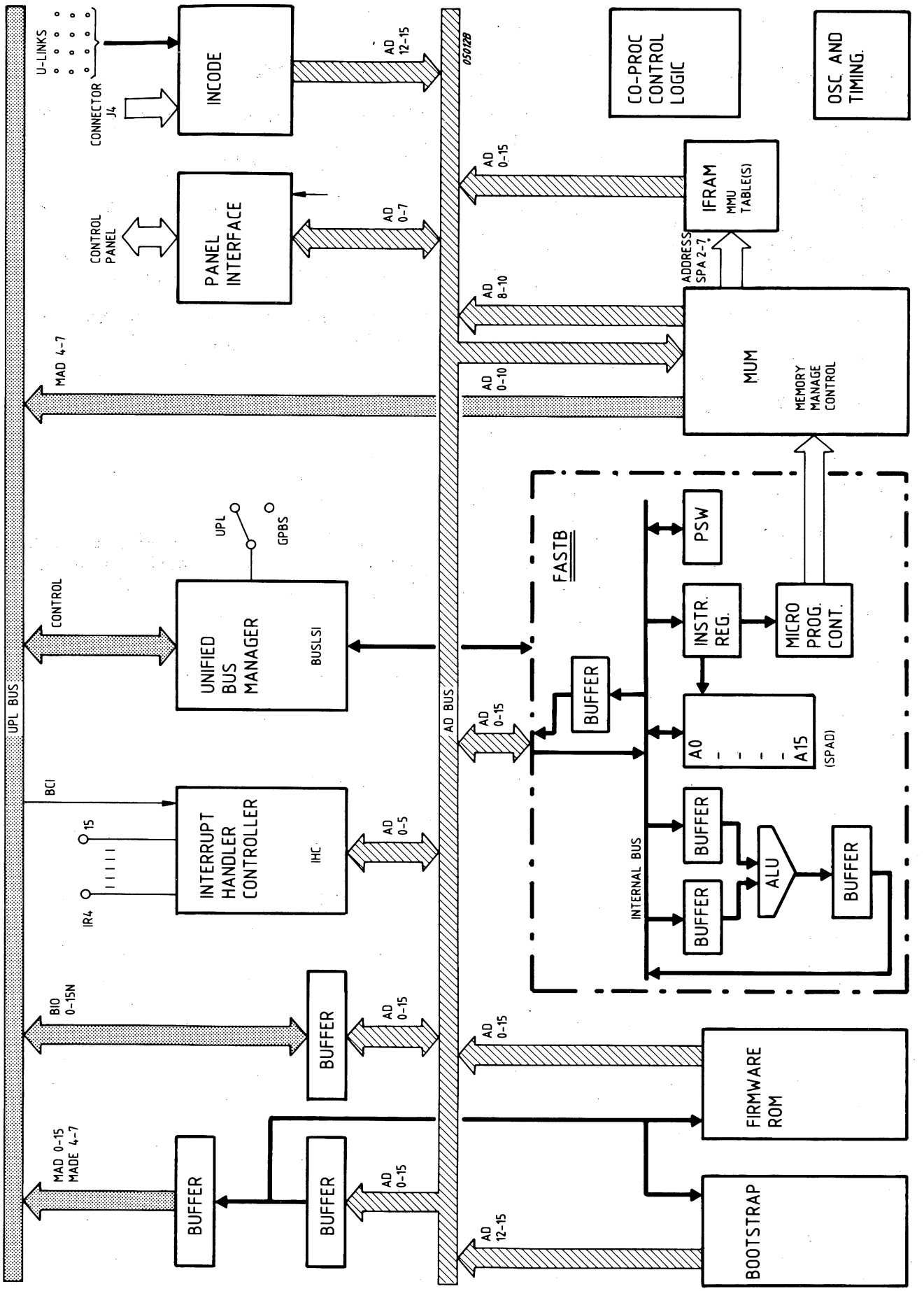


Figure 7.2 BLOCKDIAGRAM CP1BF

7.5 POWER-ON SEQUENCE

GENERAL

With Power-On the power supply initiates the standard sequence:

- DC voltages on
- Reset becomes inactive (RSLN = 1)
- Power Failure becomes inactive (PWFN = 1)

The following flowchart indicates what happens depending on the signals LOCK and BAWOFN when power is switched on.

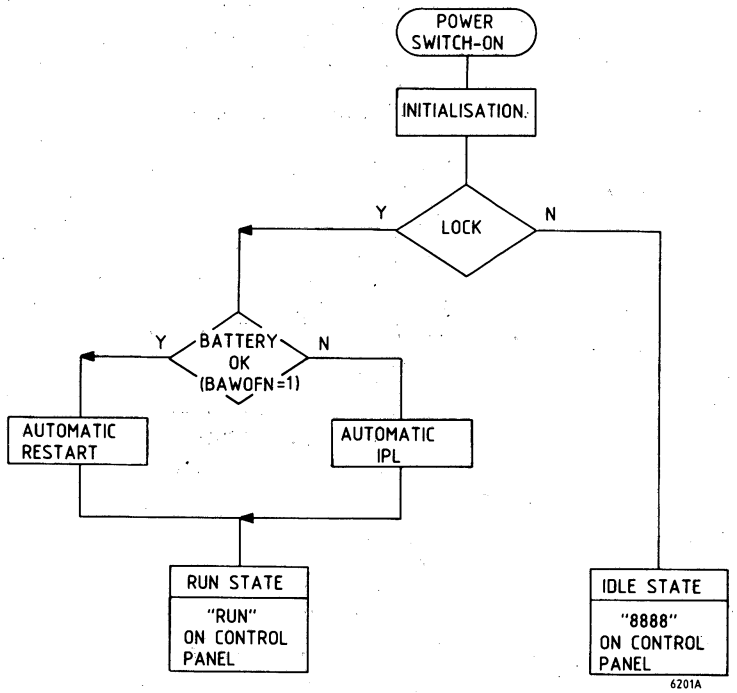


Figure 7.3 POWER-ON SEQUENCE GENERAL

THE CIP STATES

There are three CIP states:

INIT state - This is a transient state situated between the starting sequence after a Power ON sand either the IDLE or RUN states.
IDLE state - No program is running and the CIP is waiting for an operator command.
RUN state - A program is running.

INIT STATE .

The CIP enters this state after POWER ON, when RSLN=1.

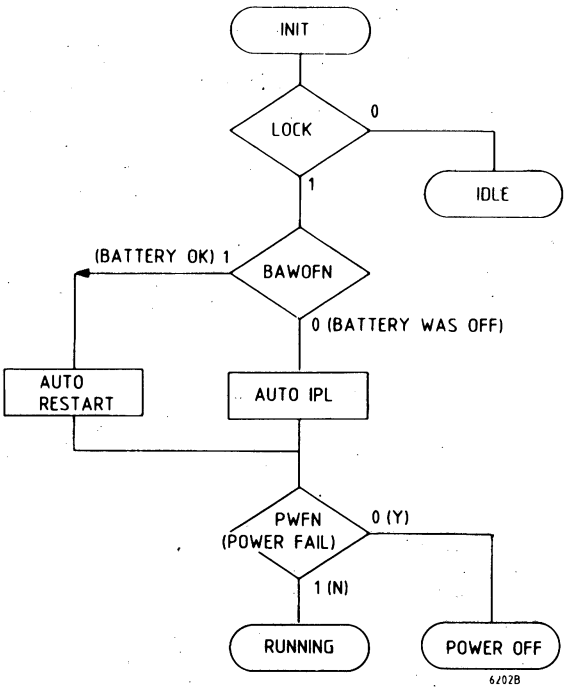


Figure 7.4 CIP INIT STATE

Notes: BAWOFN = 1 means that battery was normally supplying the memories since the latest power off.

LOCK can be set to '0' from either the HHP/FRCP or from an operator panel, which has a corresponding switch. Without a panel, LOCK is '1'.

Check of Auto-IPL: When LOCK is '1' and the battery is disconnected to force BAWOFN = '0' an Automatic IPL is done in stead of Automatic Restart, which is normally done.

IDLE STATE

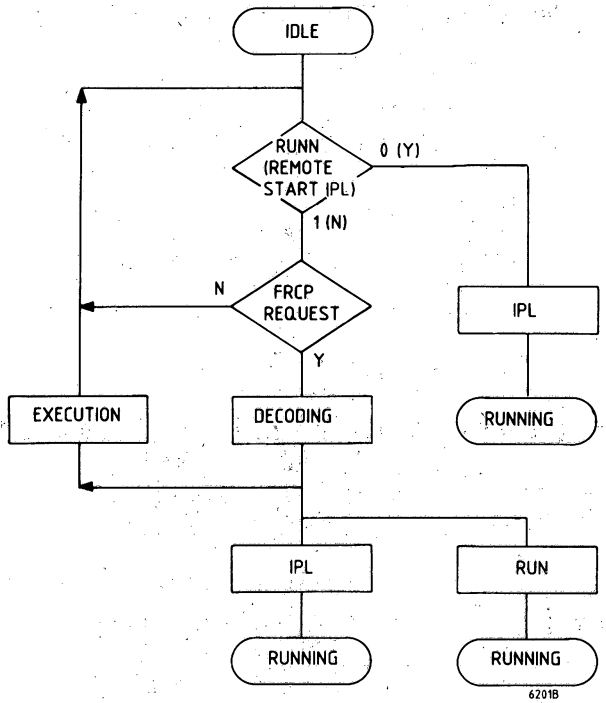


Figure 7.5 CIP IDLE STATE

RUN STATE

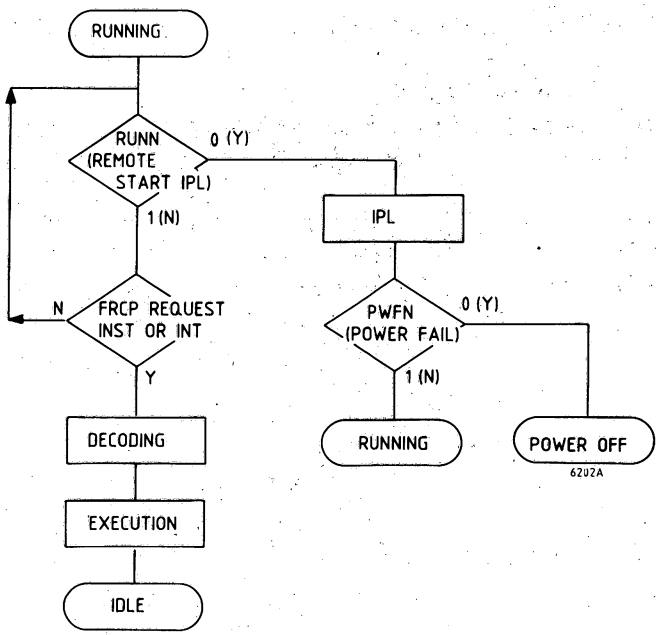


Figure 7.6 CIP RUN STATE

7.6 MICRODIAGNOSTICS

The MICRODIAGNOSTICS are initialized by using the HHP/FRCP.
Key in an existing CU-address, followed by key 'Ø' and TEST simultanously.
A code is displayed, meaning either the correct end of test or an error detected.

These codes are:

OKAY	code /0004	
CPU error	/0001	
CU or BUS error	/0002	
RAM or BUS error	/0003	(test up until 64kb)

Notes:
- OKAY /0004 : CPU registers contain their register number:

```
AØ =  /0000
A1 =  /1111
A2 =  /2222
   :
A15 =  /FFFF
```

Memory locations contain their address value:

```
/0000 =  /0000
/0002 =  /0002
/0004 =  /0004
   :
/FFFE =  /FFFE
```

- RAM (MEMORY) error /0003:
  CPU register AØ = address of erronous location
  A1 = expected pattern
  A2 = read pattern (wrong data)

7.7 SHORT DESCRIPTION OF TESTPROGRAMS

For the CP1BF the same testprograms as for the CP2B are used:
Refer to the P876-CPU description in chapter 9

7.8 P870-570 TESTTOOL SBC (TSBC)

7.8.1. IDENTIFICATIONS TSBC

- Type no. P870-570: 5111 199 63400 TEST CONN. C5
  5111 199 63410 TEST CONN. C3
  5111 199 63430 TEST CONN. C6-1
  5111 199 63520 CABLE HHP, 0,5m
  5111 199 63970 CABLE SBC-TSBC
  5111 199 66190 P.C.B. TSBC

Note: For P871 the P.C.B (5111 199 66190) is to be used for execution of Control Panel Functions POFF, PACC and PWR on the CP1BF.
The other parts (connectors and cables) are not used with P871.

- Power Consumption:

	+ 5VL	+12VL	-12VL	
TSBC	1.8A	0.04A	0.04A	*

* HHP or FRCP control panel is not connected.

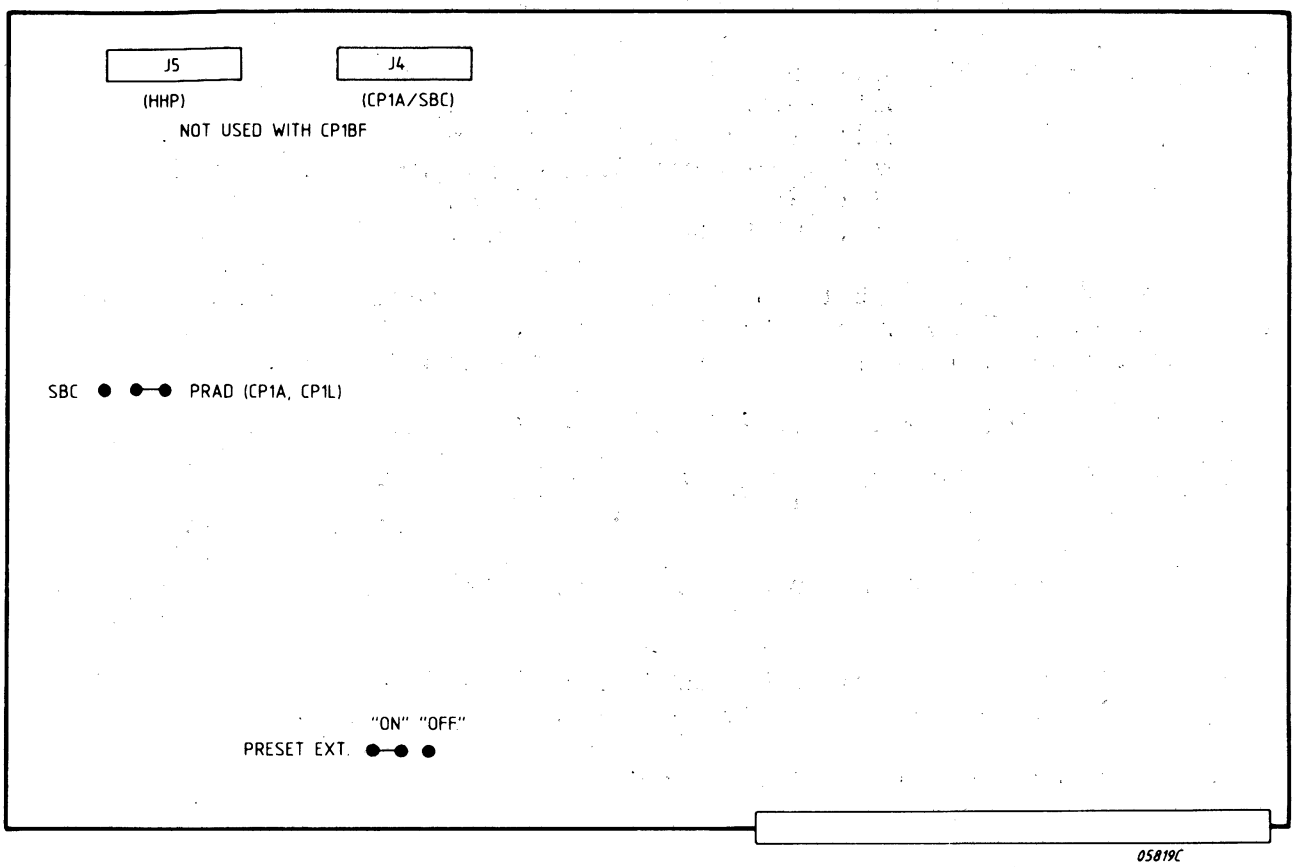
Table 7.6 POWER CONSUMPTION TSBC

- 12 NC code on the sticker of the board:

TSBC : 5111 199 6619x

x = modification level.

7.8.2 INSTALLATION TSBC



PRESET EXTENSION: ON = Preset Address with 24 bits
OFF = Preset Address with 16 bits

Figure 7.7 TSBC U-LINKS

After the U-links have been placed in the correct position the TSBC card can be inserted in any free slot of the system rack (RA12F).
No other connections to the TSBC card must be made.
The HHP or FRCP control panel must be normally connected to the CP1BF CPU card.

7.8.3 INTERFACES TSBC

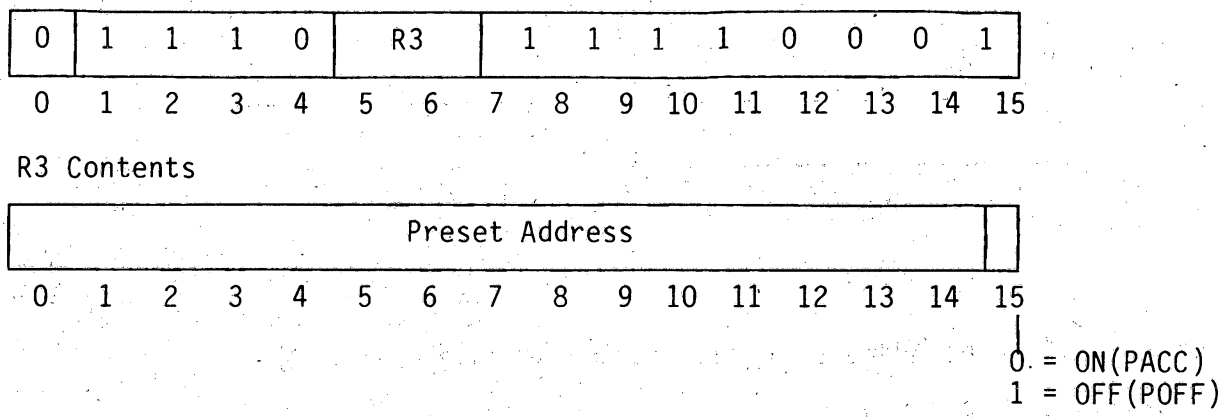
The two connectors J4 and J5 are not used with P871.
The cables and testconnectors, supplied with P870-570 are also not used.

The TSBC uses the normal UPL interface signals.
The signals STOPN is activated (low) by TSBC if the PRESET-function was active and a preset on address was detected.
The CP1BF will, switch to firmware mode and so stop the execution of a program, completing the instruction that caused the PRESET-STOP on address.

7.8.4 HARDWARE-SOFTWARE INTERFACE TSBC

The CP1BF firmware executes the panel functions PACC, PWR and POFF with the following WER instructions to the TSBC.

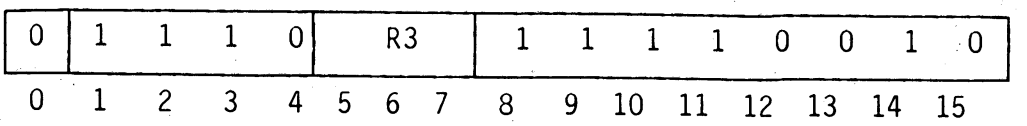
- PACC : WER /F1
- POFF : This command is used to write the Preset Address and the ON/OFF bit.



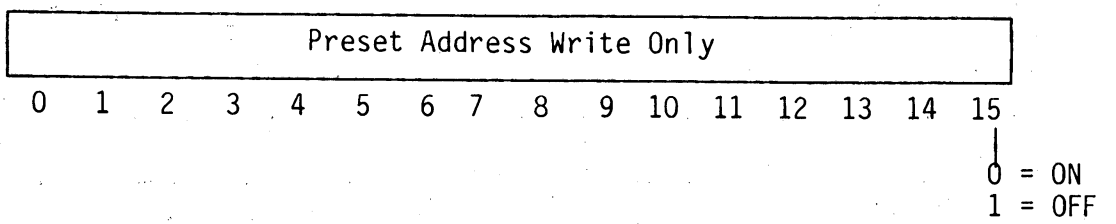
Where: R3 = The address of the Operand Register (1 to 7).

- PWR : WER /F2

This command is used to access the Preset Address on Write functions only and the format is:



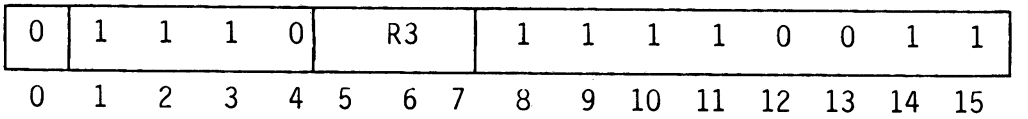
R3 Contents



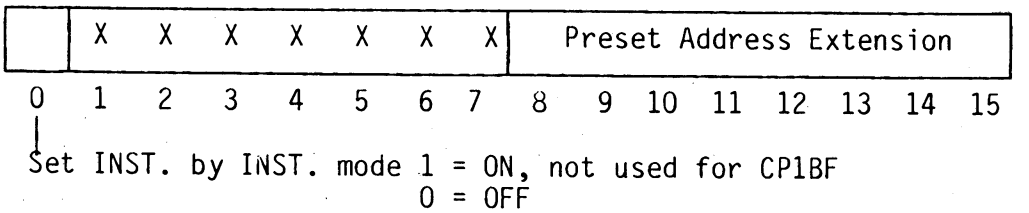
Where: R3 = The address of the Operand Register (1 to 7).

- PACC/PWR : WER /F3

This command is used for access to an extension of the Preset Address and the format is:



R3 Contents



Where: R3 = The address of the Operand Register (1 to 7).

X = Don't care.

Notes: - With PACC or PWR first WER /F1 or WER /F2 are executed, in both cases followed by WER /F3.
- These WER instructions for address /F1-/F3 could also be given by software.
In this case the TSBC card could be used even with the CP2B or CP7E to program a stop on preset address.

8 P874 CPU CP7E (C7E2, C7E1, MIOP)

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8.1 P874 CPU IDENTIFICATIONS

Type no.	P874-300	(RA12F Rack)
	P874-400	(RAL22F Rack)
Test Programs	CPU	- CP57RE
	MIOP	- see Chapter: - 12 (IOP commands words)
		11 (MMU)
	Integr. CU:	
	ASR/PER31ØØ	- BBSER1
	VDU	- BBDISP
Devices	Per31ØØ	- P842-ØØ1
	VDU	- P817-ØØ2
		- P816-Ø10
		- P816-Ø20
		- P818-Ø10
		- P818-Ø20

Power consumption:	+5VL	+12VL	-12VL
C7E1	4A		
C7E2	2.5A	5ØmA	5ØmA
MIOP	2.6A		

12NC code on the sticker on the board:

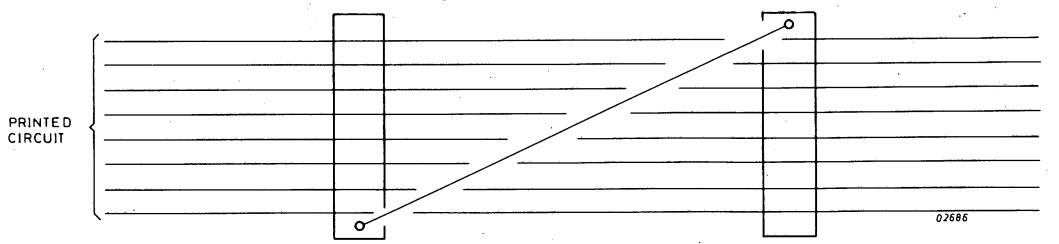
C7E1A	5111 199 6377x (5322 216 25725)
C7E2A	5111 199 6376x (5322 216 25724)
MIOPA	5111 199 6375x (5322 216 25723)
C7E1B	5111 199 6198x (5322 216 21Ø81)
C7E2B	5111 199 6199x (5322 216 21Ø82)
MIOPB	5111 199 62ØØx (5322 216 21Ø83)
BACK PANEL	5111 199 6006x

x = modification level

8.2 INSTALLATION

The following instructions are only intended to highlight the important aspects of installing this systeem.

. Insert the Eurorack into the front of the cabinet and screw into position.
. Ensure that the mains are connected in accordance with the specification (this may differ depending upon the country of installation.
. Check the card links before inserting cards into the Eurorack.
. Ensure that the cables between Control Units and Devices are firmly secured and that the screens of these cables are connected in accordance with the Grounding Rules.
. Interrupts and Breaks must be wired so that they run across the printed circuit wires and NOT parallel to them (see below).



WIRED CONNECTION RUNNING ACROSS THE PRINTED CIRCUIT

Figure 8.1 INTERCONNECTION WIRING

8.2.1. U-LINK SETTINGS

There are u-links fitted to all 3 cards but only C7E2B houses the U-links that are selectable by the user:

. IPL links to select the IPL and program loading device for remote and/or auto IPL.
. CT133 link
. Speed Selection Links for the V24 peripheral interface. All cards must be checked to ensure that the workshop test links are in position.

Interrupt and Break wiring can be found in the CPU chapters.

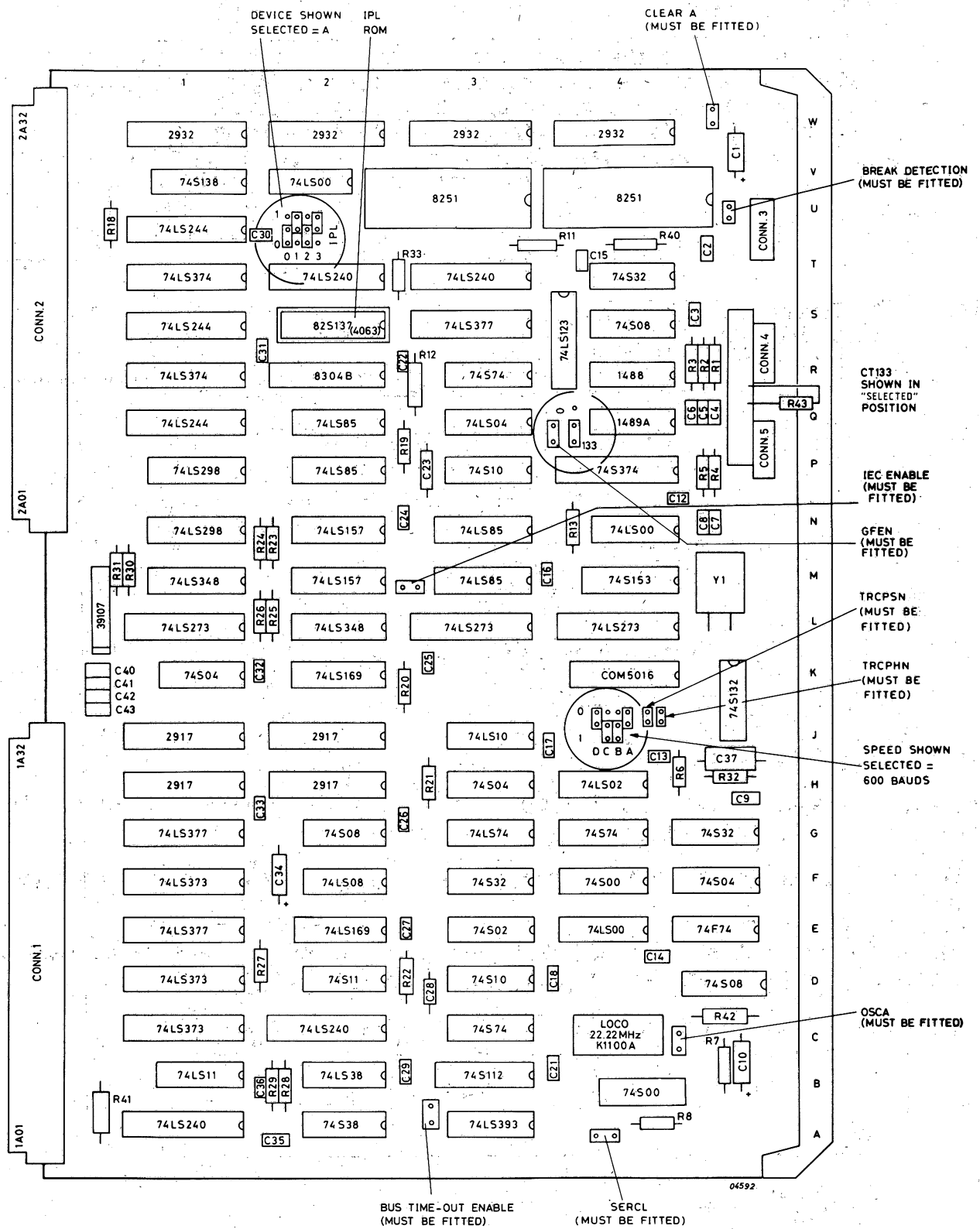


Figure 8.2 C7E2B COMPONENT LAYOUT AND LINKS

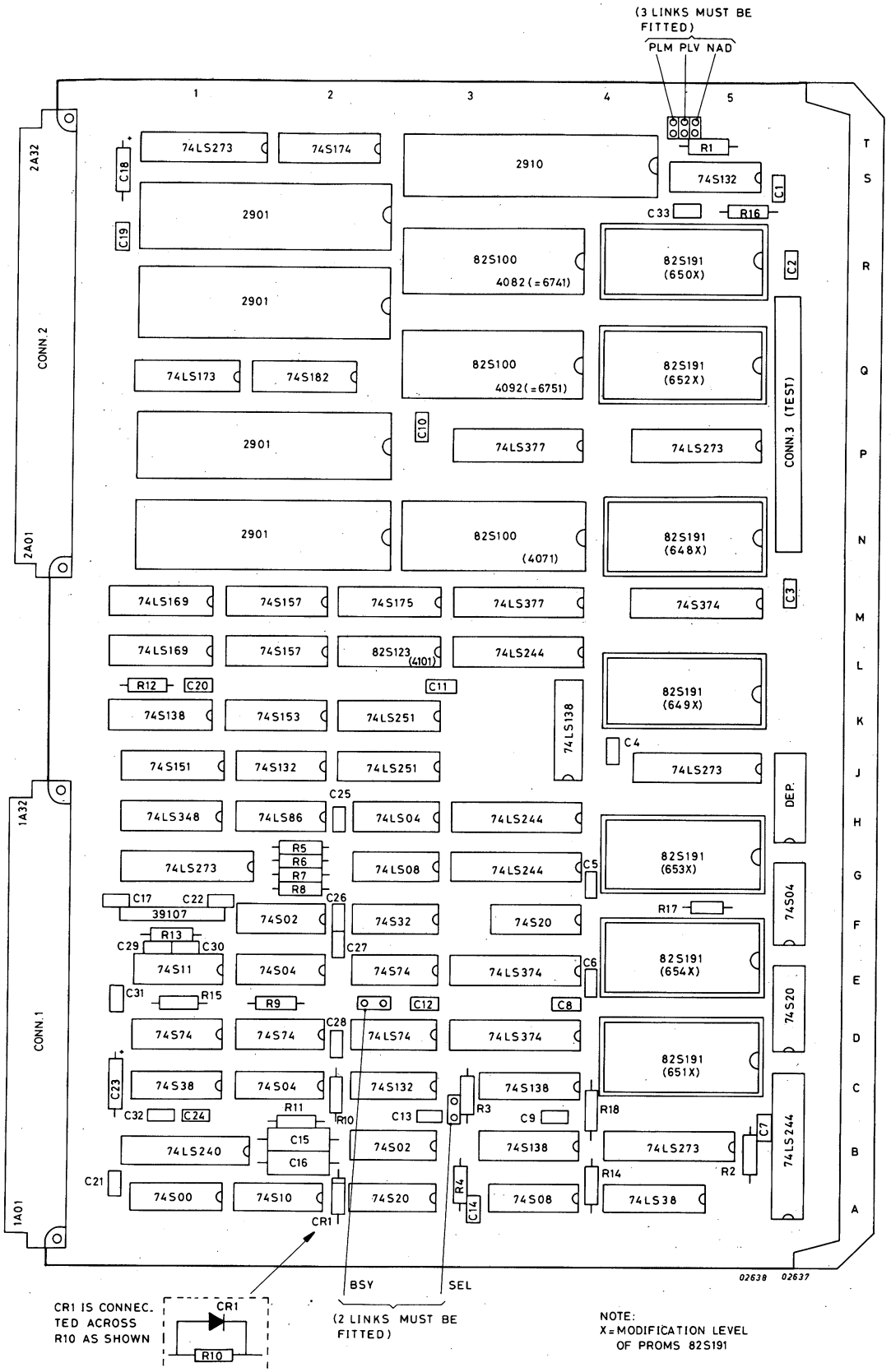


Figure 8.3 C7E1B COMPONENT LAYOUT AND LINKS

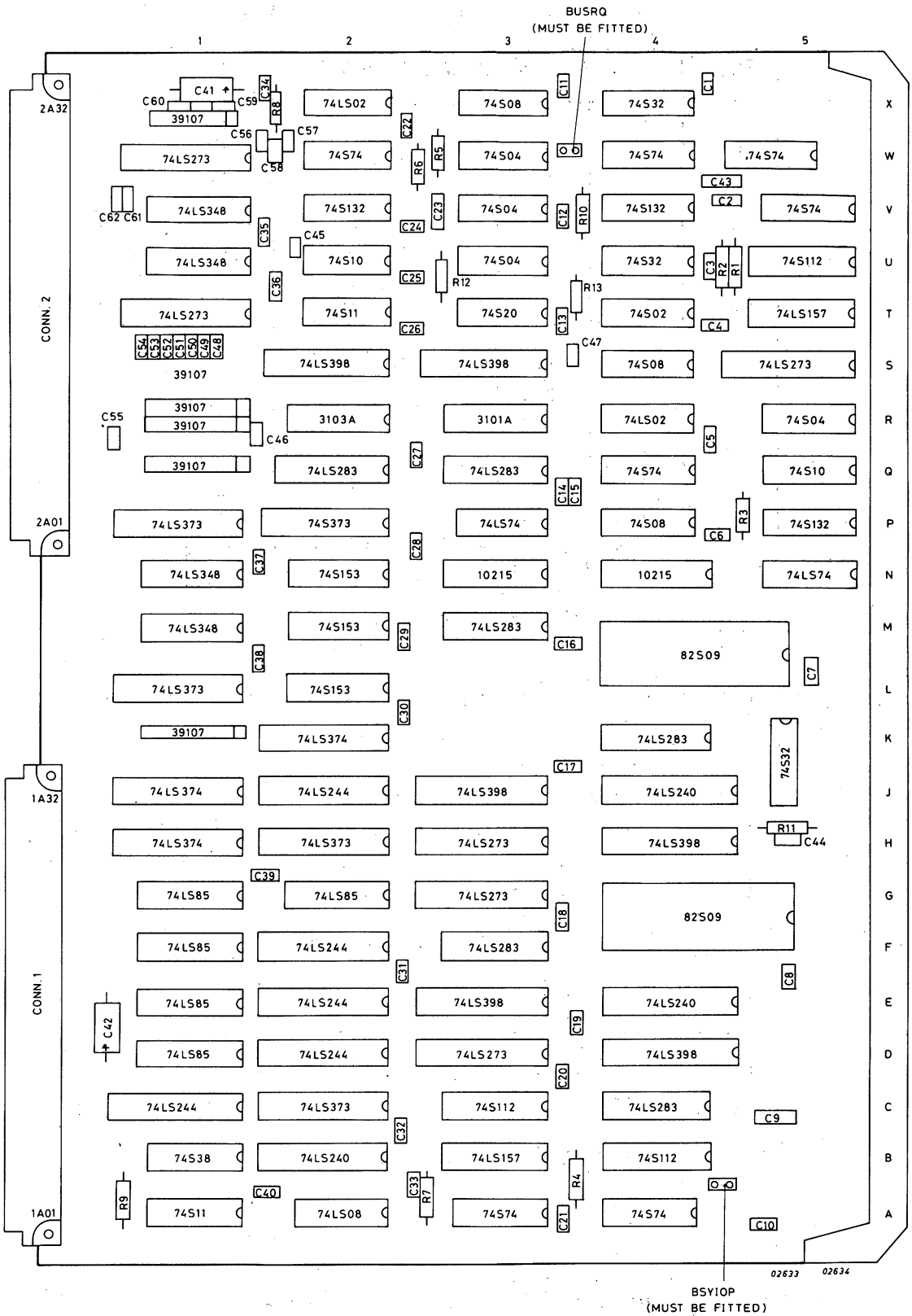
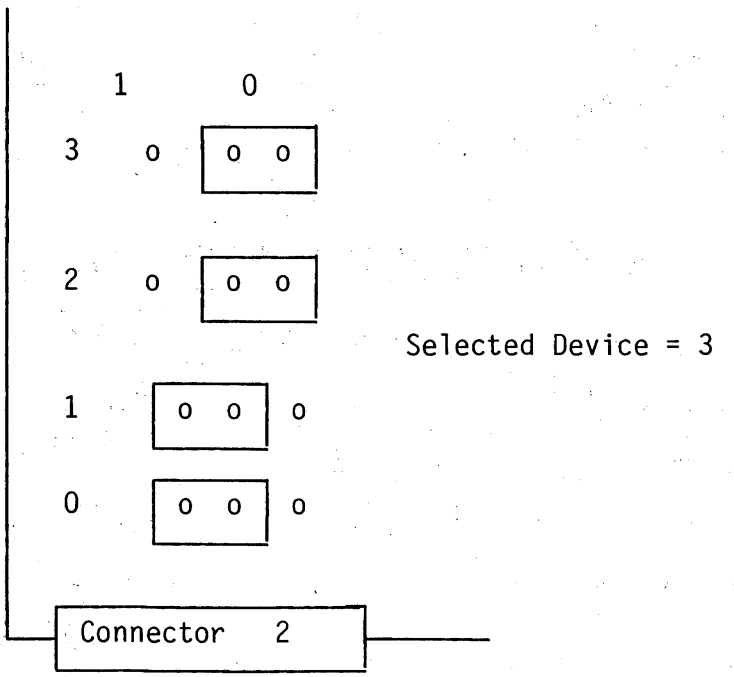


Figure 8.4 MIOPB LAYOUT AND LINKS

3	2	1	0		MEMORY ADRESS
OPS3N	OPS2N	OPS1N	OPSON	WORD	HEX
0	0	0	0	0	1FE
0	0	0	1	1	1FC
0	0	1	0	2	1FA
0	0	1	1	3	1F8
0	1	0	0	4	1F6
0	1	0	1	5	1F4
0	1	1	0	6	1F2
0	1	1	1	7	1F0
0	0	0	0	8	1EE
1	0	0	0	9	1EC
1	0	1	0	10	1EA
1	1	0	1	11	1E8
1	1	0	0	12	1E6
1	1	0	1	13	1E4
1	1	1	0	14	1E2
1	1	1	1	15	1E0

Table 8.1 SELECT -IPL (REMOTE LOAD)

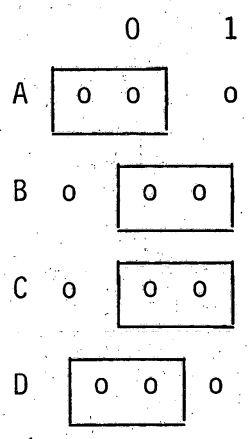
The following diagram shows the identification that is silkscreened on the card and an example of word selection.



Transmit/Receive U Link Positions				Baud Rate
D	C	B	A	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134,5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1.200
1	0	0	0	1.800
1	0	0	1	2.000
1	0	1	0	2.400
1	0	1	1	3.600
1	1	0	0	4.800
1	1	0	1	7.200
1	1	1	0	9.600
1	1	1	1	19.200

Table 8.2 V24 - PERIPHERAL INTERFACE - SPEED SELECTION

The following diagram shows an identification that is silkscreened on the card, and an example of speed selection:



Selected speed is 600 bauds (PER 3100)

8.2.2 CONFIGURATION RULES

When the P874 configuration is being assembled the following rules must be taken into account.

. Cards C7E2, C7E1 and MIOP must be in rack position 1, 2 and 3 respectively.
. Other Masters follow in order of their system priority, determined by links OKO and OKI.
. Card MIOP contains 2 IOP's IOPA and IOPB. IOPA must always have a higher priority than IOPB (determined by links OKOA/B and OKIA/B).
. Control Unit addresses for connection with MIOP less than or equal to /F, without MIOP connection any address may be used.
. The UPL Bus must not be extended out of the basic Eurorack without the signals being terminated.

- When present, the Floating Point Processor (FPPE) must be located at the cardposition 4 and 5.
  Dedicated wiring is necessary between the CPU cards and the FPPE (2 slots backpanel).
- The recommended cardposition for TUGP is 12 (RA12F rack) or 23 (RAL22F rack).

8.3 INTERFACES

Figure 8.2 shows the system of pinning and numbering for card C7E2. In general the same principe applies for all double EURO-CARDS connector 1 and 2.

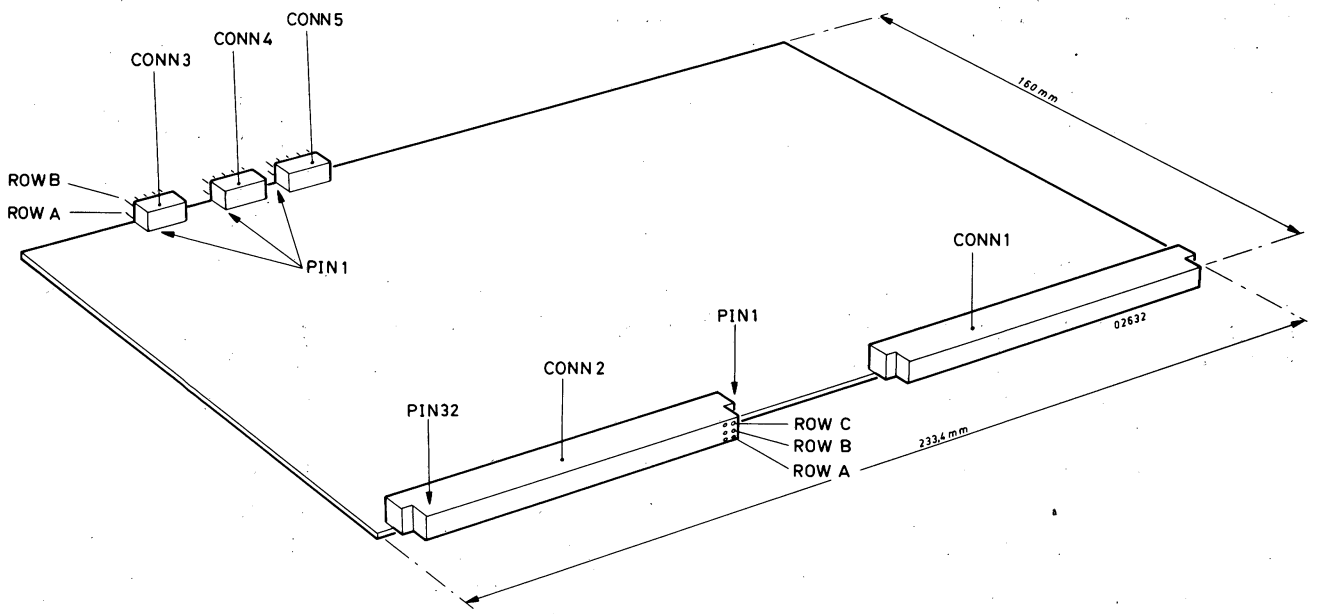


Figure 8.5 EUROCARD FORMAT (C7E2)

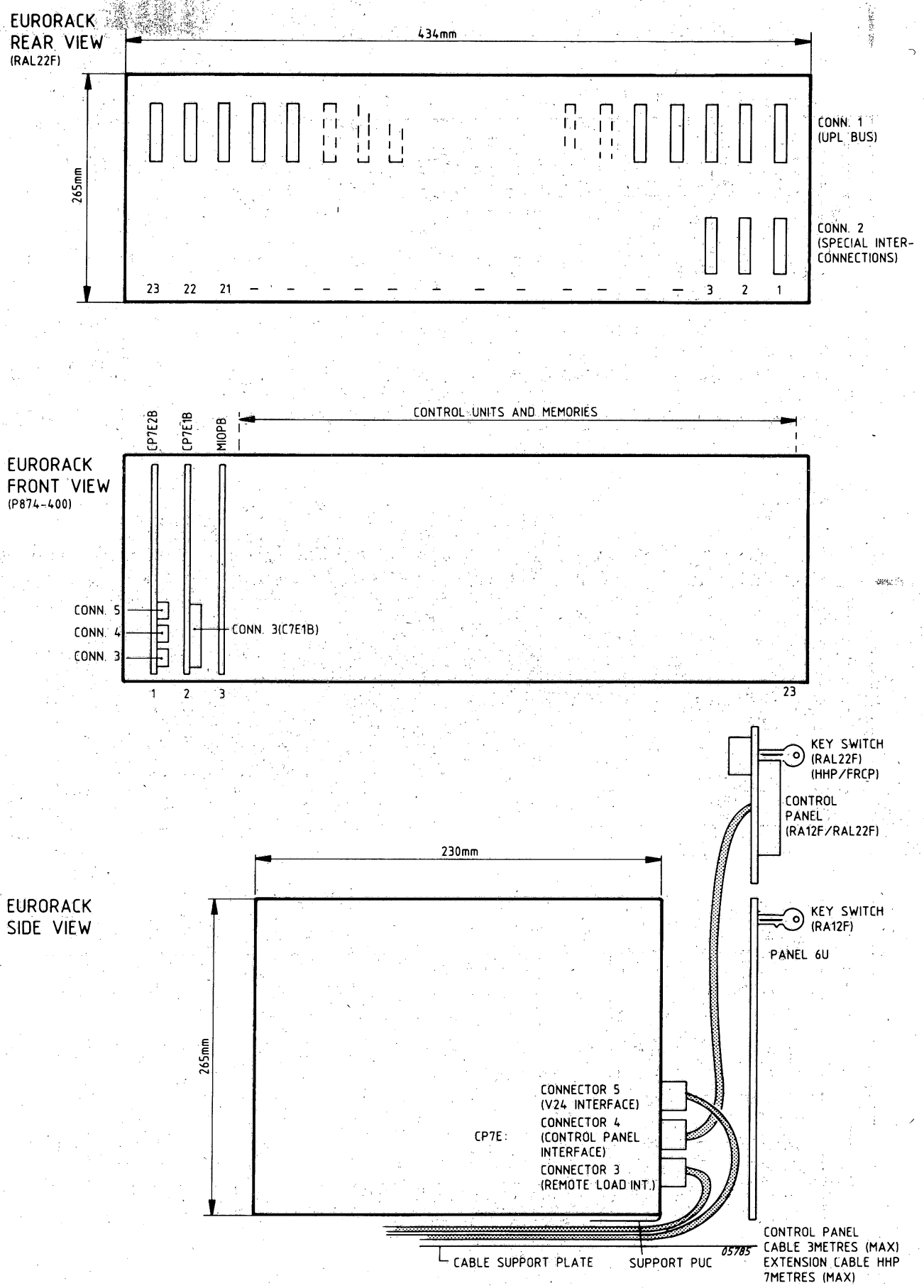


Figure 8.6 EURORACK

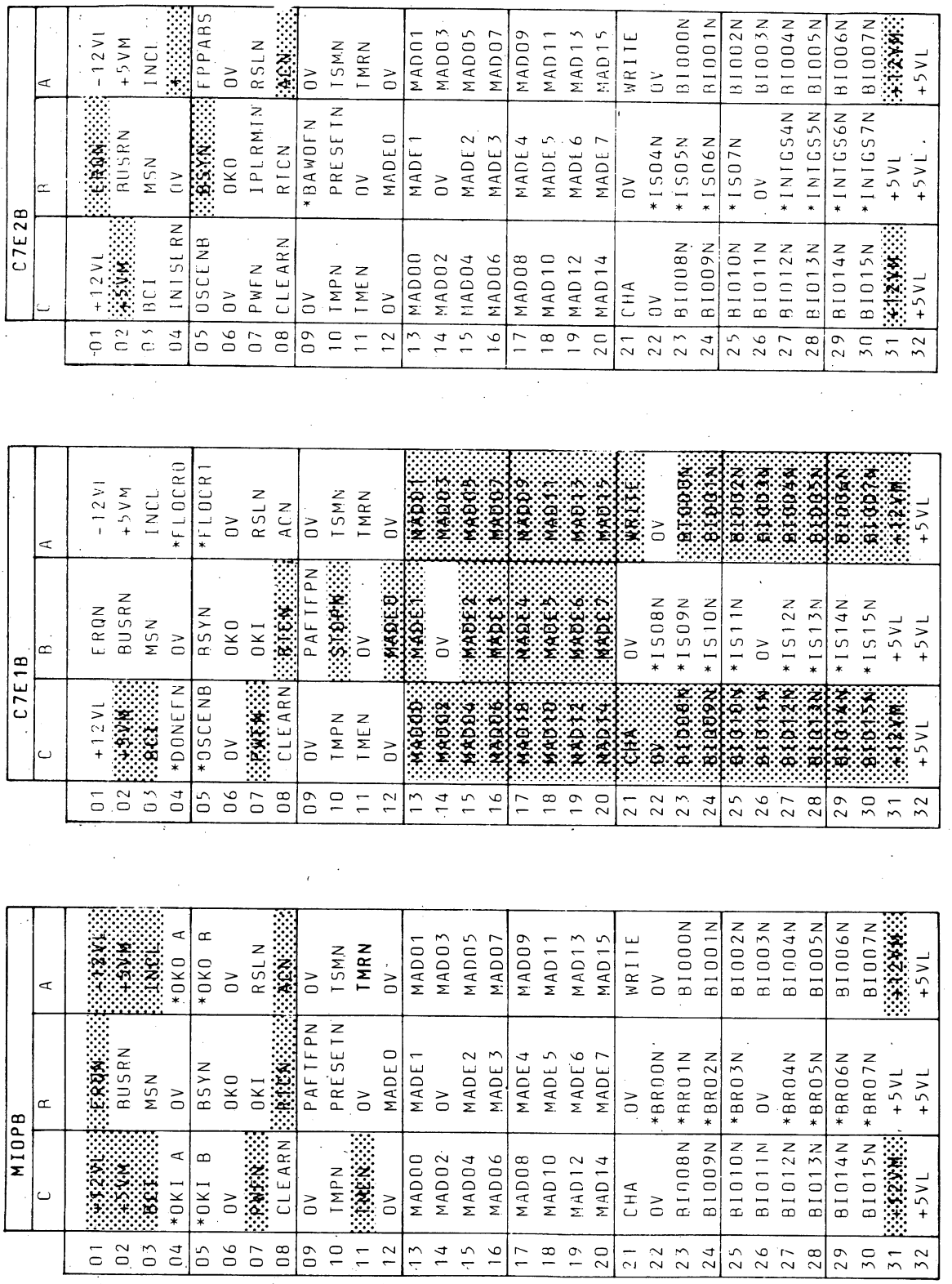


Figure 8.7a CONNECTOR 1 - C7E2, C7E1, MIOP

	MIOPB		
	C	B	A
01	APN	BR08N	OSC
02	GPRESETN	BR09N	MADS00
03	BSYCPUEXN	BR10N	MADS01
04	BSYCPUN	BR11N	MADS02
05	TMRENB	BR12N	MADS03
06		BR13N	OV
07	OV	BR14N	ALU10
08	D00	BR15N	ALU11
09	D01	ALU04	ALU12
10	D02	PRESETN	ALU13
11	D03		ALU14
12	D04		ALU15
13	D05	ALUCIN	
14	D06	IS16N	SELR2
15	D07	IS17N	OKMMU
16	D08	IS18N	FLAGCW3N
17	D09	IS19N	BIORECN
18	D10	IS20N	PAFN
19	D11	IS21N	SELSPBUFN
20	D12	IS22N	
21	D13	IS23N	IEC3
22	D14	IS24N	IEC4
23	D15	IS25N	IEC5
24	ENBIOP	IS26N	INTGS2N
25	FUN	IS27N	INTGS3N
26	IOPN	OV	GPSPN
27		IS28N	INTE3N
28		IS29N	INTE1N
29		IS30N	RUNN
30	+5V **	IS31N	GFETCH
31		BSYCN	WAIT
32	WRITEM		MIOPABS

	C7E1B		
	C	B	A
01	APN	DONEFCPN	GPCHAN
02	GPRESETN	GPLRLDN	
03	BSYCPUEXN	ALU00	GPMADN
04	BSYCPUN	ALU01	SELIPIN
05	TMRENB	ALU02	TMFN
06	FPABS	ALU03	IRUNA
07	FEN	ALU04	ALU10
08	D00	ALU05	ALU11
09	D01	ALU06	ALU12
10	D02	ALU07	ALU13
11	D03	ALU08	ALU14
12	D04	ALU09	ALU15
13	D05	ALUCIN	PUPF
14	D06	ALUI1	SELR2
15	D07	ALUI7	OKMMU
16	D08	ALUMADP1	GROUND (Back Panel)
17	D09	CR0	FLOACT
18	D10	CR1	PAFN
19	D11	NAD03	SELSPBUFN
20	D12		RUNIRN
21	D13	NAD08	IEC3
22	D14	NAD09	IEC4
23	D15	NAD10	IEC5
24	ENBIOP	SELCONSIN	INTEON
25	FUN	BSYCN	GPSPN
26	PCI3	DENB	INTGS1N
27	PCI2	BOFFN	SEL8251N
28	PCI1	TIMEOUT	INTE1N
29	PCI0	TMRZON	MIOPABS
30	PCCI	SELD2	GFETCH
31	LOADSN	SELD1	SEQCPU1
32	WRITEM	SELD0	SEQCPU0

	C7E2B		
	C	B	A
01	APN	DONEFCPN	OSC
02	GPCHAN	GPLRLDN	MADS00
03	BYSCPUEXN	ALU00	MADS01
04	BSYCPUN	ALU01	MADS02
05	GPMADN	ALU02	MADS03
06	OV	ALU03	IRUNA
07	FEN	ALU04	ALU10
08	D00	ALU05	ALU11
09	D01	ALU06	ALU12
10	D02	ALU07	ALU13
11	D03	ALU08	ALU14
12	D04	ALU09	ALU15
13	D05	ALUCIN	PUPF
14	D06	ALUI1	SELIPIN
15	D07	ALUI7	OKMMU
16	D08	ALUMAIP1	FLAGCW3N
17	D09	CR0	BIORECN
18	D10	CR1	PAFN
19	D11	NAD03	SELSPBUFN
20	D12	IOPN	RUNIRN
21	D13	NAD08	IEC3
22	D14	NAD09	IEC4
23	D15	NAD10	IEC5
24	ENBIOP	SELCONSIN	INTGS2N
25	FUN	SELQICN	INTGS3N
26	PCI3	DENB	INTGS1N
27	PCI2	BOFFN	INTEON
28	PCI1	TIMEOUT	SEL8251N
29	PCI0	TMRZON	RUNN
30	PCCI	SELD2	WAIT
31	LOADSN	SELD1	SEQCPU1
32	WRITEM	SELD0	SEQCPU0

** NOTE: SI P854-M-022 MIOP A

Figure 8.7b CONNECTOR 2 - C7E2, C7E1, MIOP

C7E2E Pin No.	Signal Name	Description	Source	Destination
3B03	OPS0N	Address Lines from a Remote Device to address the last 16 words of the Bootstrap Key position	Remote Device	C7E2
3B02	OPS1N			
3B04	OPS2N			
3B01	OPS3N			
3A05	not connected			
3A01-04	0V			
3B05	0V			

Table 8.3 IPL REMOTE LOAD INTERFACE - CONNECTOR 3

C7E2B Pin No.	Signal Name	Description	Source	Destination
4B01	LOCK	= 0 Control Panel functions are enabled. = 1 Control Panel functions (except INT) are inhibited.	FRCP	C7E2
4B03	0V			
4A01	SDPM	Serial Data (CT104)	FRCP	C7E2
4B02	SDMP	Serial Data (CT103)	C7E2	FRCP
4A02	RTCE	= 0 inhibit Real Time Clock = 1 enable Real Time Clock	FRCP	C7E2
4A03	RESETN	Master Reset	C7E2	FRCP
4B04	+5V			
4A04	-12V			
4A05	not connected	Key Position		
4B05	+12V			

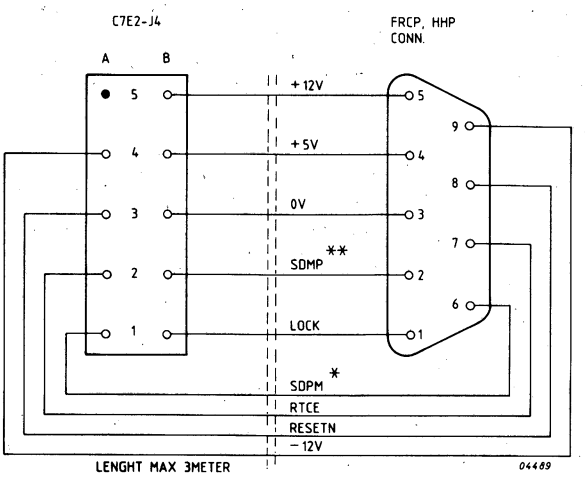
Table 8.4 CONTROL PANEL INTERFACE (FRCP) - CONNECTOR 4

C7E2B	Signal Name	Description	Source	Destination
5B02	CT103	Serial Data	C7E2	D.T.E.
5A01	CT104	Serial Data	D.T.E.	C7E2
5A02	CT107	Modem Ready	D.T.E.	C7E2
5B03	CT108	Connect Modem to Line	C7E2	D.T.E.
5A03	CT133	Ready for Receiving	D.T.E.	C7E2
5B01	0V			
5A04	0V			
5A05	0V			
5B04	0V			
5B05	not connected	key position		

Table 8.5 V24 PERIPHERAL INTERFACE - CONNECTOR 5

Pin	Signal Name	Description
3A01	ROMAD08	Microprogram ROM Address Lines, note that only 9 of the 11 lines are available here, for ROMAD09 and 10 see pins 3B17 (C7E1).
02	07	
03	06	
04	05	
05	04	
06	03	
07	02	
08	01	
09	ROMAD00	
10		
11	BSYCPU	Indicates CPU busy with Bus (C7E1).
12	TMPN	Indicates Transfer Master to Peripheral (C7E1).
13	TMRN	Indicates Transfer Master to Memory (C7E1).
14	OSCENB	Enables the internal clock (C7E1).
15		Not Used.
16		Not Used.
17	RSLAN	Simulates RSLN from the Power Supply (C7E1).
18	APTEST	Enables an external test of the CPU Sequensor signal AP (C7E1).
19	5V	
20	5V	
3B01	D00	3-state internal CPU Bus (C7E1).
02	01	
03	02	
04	03	
05	04	
06	05	
07	06	
08	07	
09	08	
10	09	
11	10	
12	11	
13	12	
14	13	
15	14	
16	D15	
17	ROMAD10	See pin nos. 3A01-3A09.
18	ROMAD09	
19	0V	
20	0V	

Table 8.6 TEST CONNECTOR FOR TESTTOOL (CARD C7E1B)



* SDPM= SERIAL DATA PANEL TO MASTER
RTCE= REAL TIME CLOCK ENABLE
RESETN= RESET FOR PANEL (RSLN LINE FROM POWER SUPPLY)
** SDMP= SERIAL DATA MASTER TO PANEL
LOCK= INHIBIT CONTROL PANEL FUNCTIONS EXCEPT "INT"
* SDPM: 1 STARTBIT 8 DATABITS 1 STOPBIT } 4800 BAUD
** SDMP: 1 STARTBIT 8 DATABITS 2 STOPBITS }

Figure 8.8 CABLE PANEL INTERFACE

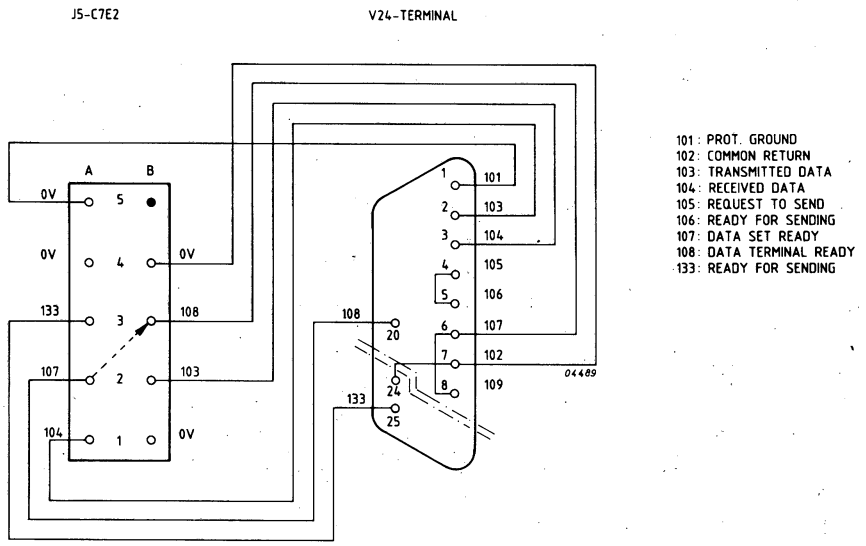


Figure 8.9 CABLE V24 INTERFACE

8.3.2 INTERCONNECTIONS

INTERRUPT AND BREAK WIRING

Interrupt wiring:

C7E2 pin:	CU	int. level:	Loc:	Pin:
1B22	.....	4	...	....
23	.....	5	...	....
24	.....	6	...	....
25	.....	7	...	....

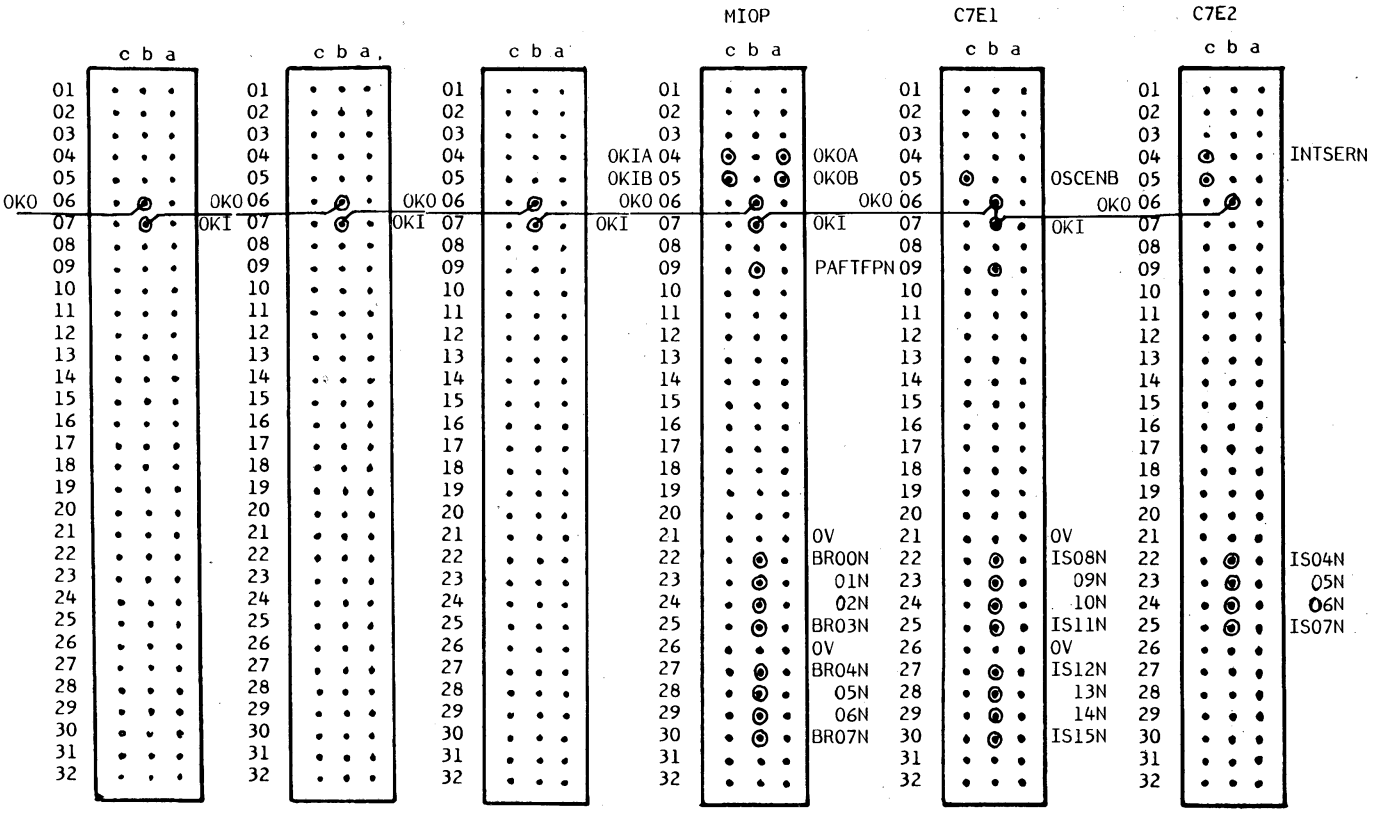
Note: Fixed (internal) interrupts are:
level Ø - power fail/auto restart
1 - program int.
2 - Real Time Clock
3 - control panel

C7E1 pin:	CU	int. level:	Loc.	Pin:
1B22	.....	8	...	....
23	.....	9	...	....
24	.....	1Ø	...	....
25	.....	11	...	....
27	.....	12	...	....
28	.....	13	...	....
29	.....	14	...	....
30	.....	15	...	....

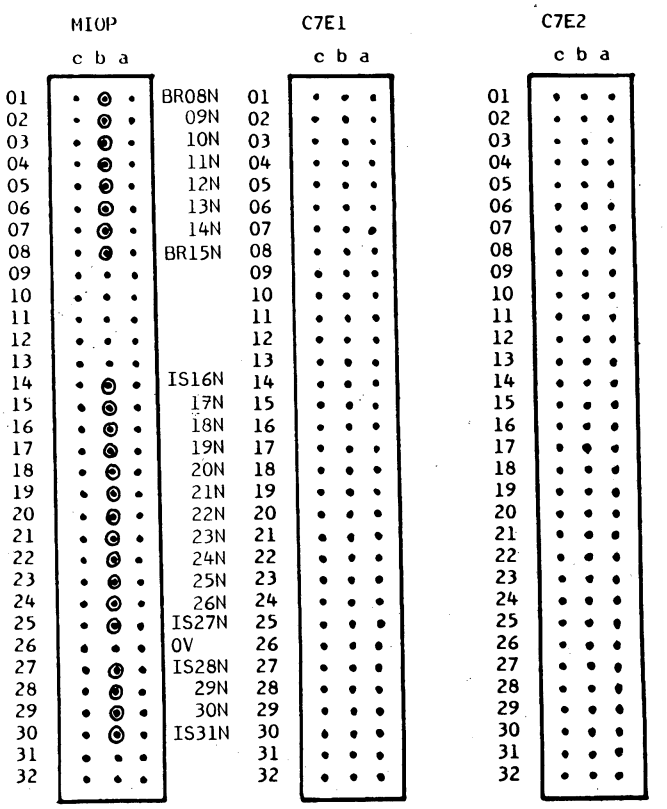
Break wiring:

MIOP pin:	CU	int. level:	Loc.	Pin:	pin:	CU	break level:		Loc	Pin
2B14	.....	16	...	....	1B22	.....	Ø	(=A-Ø)	...	....
15	.....	17	...	....	23	.....	1	1	...	....
16	.....	18	...	....	24	.....	2	2	...	....
17	.....	19	...	....	25	.....	3	3	...	....
18	.....	2Ø	...	....	27	.....	4	4	...	....
19	.....	21	...	....	28	.....	5	5	...	....
2Ø	.....	22	...	....	29	.....	6	6	...	....
21	.....	23	...	....	3Ø	.....	7	7	...	....
22	.....	24	...	....	2BØ1	.....	8	(=B-Ø)	...	....
23	.....	25	...	....	2	.....	9	1	...	....
24	.....	26	...	....	3	.....	1Ø	2	...	....
25	.....	27	...	....	4	.....	11	3	...	....
27	.....	28	...	....	5	.....	12	4	...	....
28	.....	29	...	....	6	.....	13	5	...	....
29	.....	3Ø	...	....	7	.....	14	6	...	....
3Ø	.....	31	...	....	8	.....	15	7	...	....

Table 8.7 INTERRUPT AND BREAK WIRING LIST



CONNECTOR 1



CONNECTOR 2

WIRING SIDE

Figure 8.10 BREAK AND INTERRUPT WIRING PINS

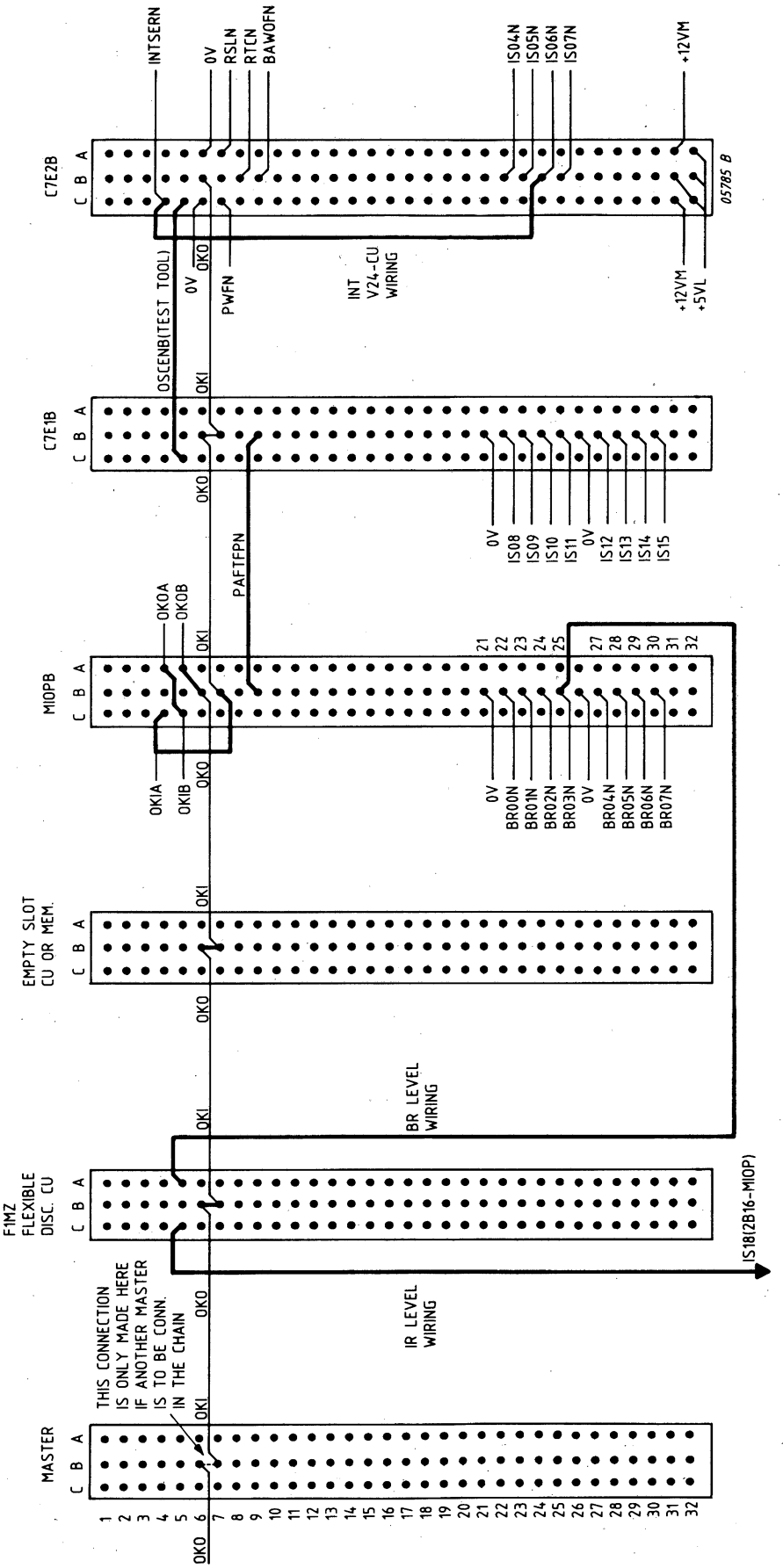


Figure 8.11 EXAMPLE OF BREAK, INTERRUPT, OKO-OKI WIRING

8.4 V24 CONTROL UNIT

8.4.1 GENERAL

An USART 8251 is used as interface between Console Typewriter and CU.
The type 8251 is also used for the interface Control Panel - CPU.

USART : Universal Synchronous Asynchronous Receiver Transmitter.

CTW : Selectable baudrate : 50 - 19.200 baud.
Panel : Fixed baudrate : 4800 baud.

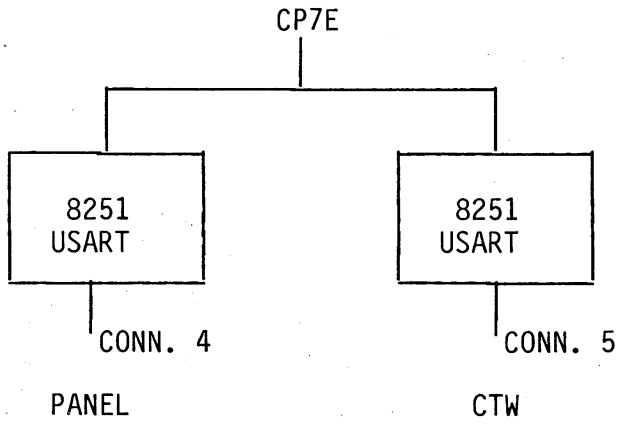


Figure 8.12 V24 CU AND PANEL INTERFACE

Straps : 5 straps total (baudrate and CT133)
CU address : /10 (fixed)
Int level : 6
HSI : see section 8.4.4

8.4.2 FACILITIES

I/O DEVICE INTERFACE

* Connection to an I/O device having V24/28 interface according CCITT.
* Programmed channel with or without using interrupt handling.
* The CU is working in half duplex mode. However, the line to an I/O device may be a so called 4 wire connection. 4 Wire line connection allows echo mode (software selection).
* The V24 line 'Ready For Receiving' CT133/CT119 may control the throughput during the output mode. (Used by PER3100). To be selected by a strap.
* Used V24 lines: CT101, 102, 103, 104, 107, 108, 109, 133. CT 107/108 must be controlled by CU/CTW.
* Break detection in order to set control panel interrupt.
* Transfer rate 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19.200 bits/sec.
* Character of line composed of:
  - 1 Start bit, rec. 1 or 2 Stop bits, trx. 2 Stop bits (normally).
  - 8 Data bits (no parity), or 7 data bits (with parity bit).
  - Software selectable (parity bit) (number of stop bits).

PANEL INTERFACE

* A-synchronous interface according CCITT V28 for serial transmission and reception.
* Transfer rate 4800 bits/sec.
* Character on line composed of:
  - 1 Start bit, (at least) 2 Stop bits.
  - 8 Data bits
  - no parity

8.4.3 CONTROL UNIT STATES

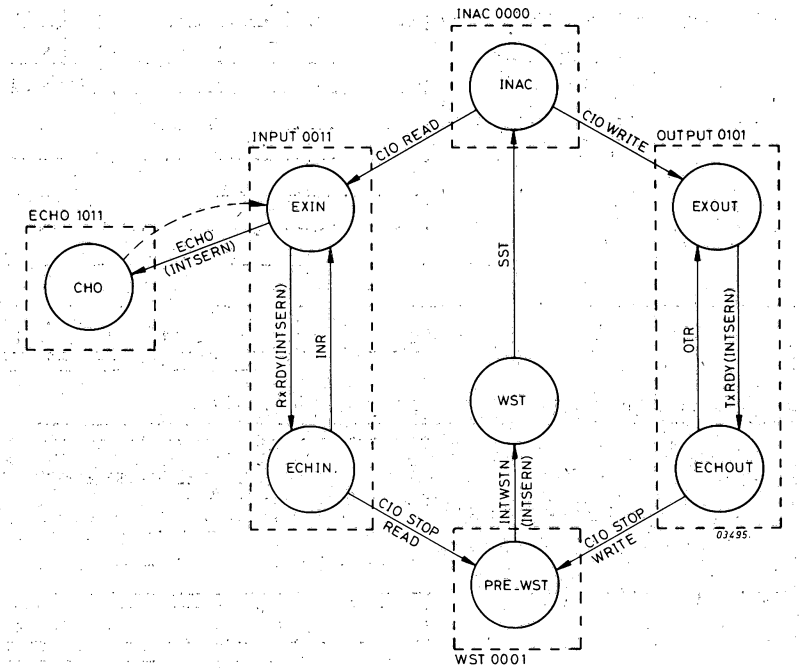
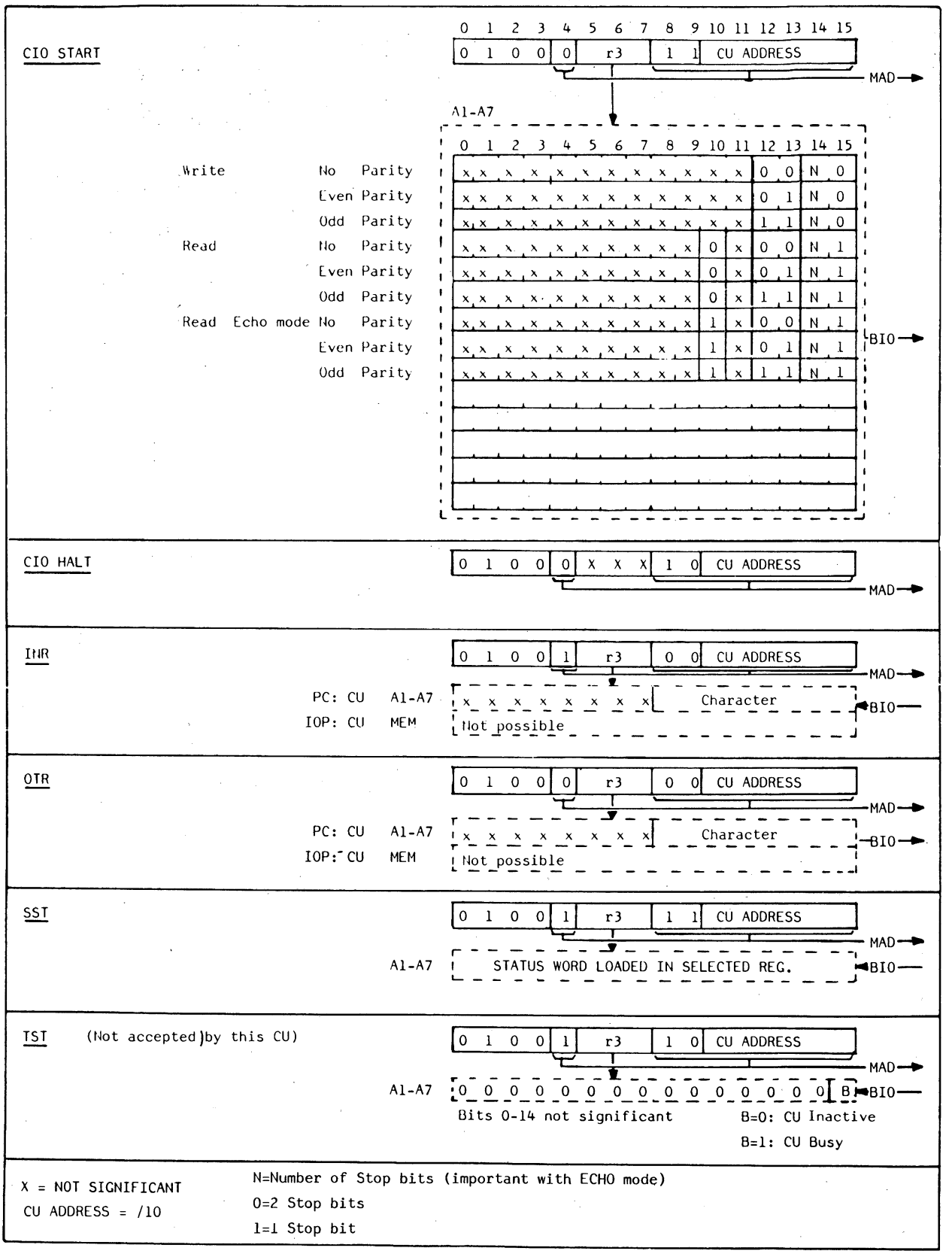


Figure 8.13 V24 INTERFACE STATES

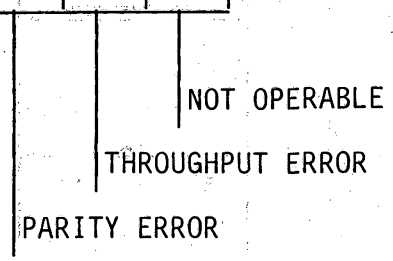


Note: * Bit 14 = 1: only one stop bit (necessary if terminal operates with one stop bit)

Figure 8.14 INSTRUCTION-/COMMAND-WORD FORMATS

8.4.4.1 STATUS WORD

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0			



NOT OPERABLE

Bit 15 is set if the device is not connected or not operable.

THROUGHPUT ERROR

Bit 14 is set during input mode, if the interrupt is not yet answered by the CPU (INR) and the next input character arrives.

PARITY ERROR

Bit 13 is set when during input mode the received character has incorrect parity

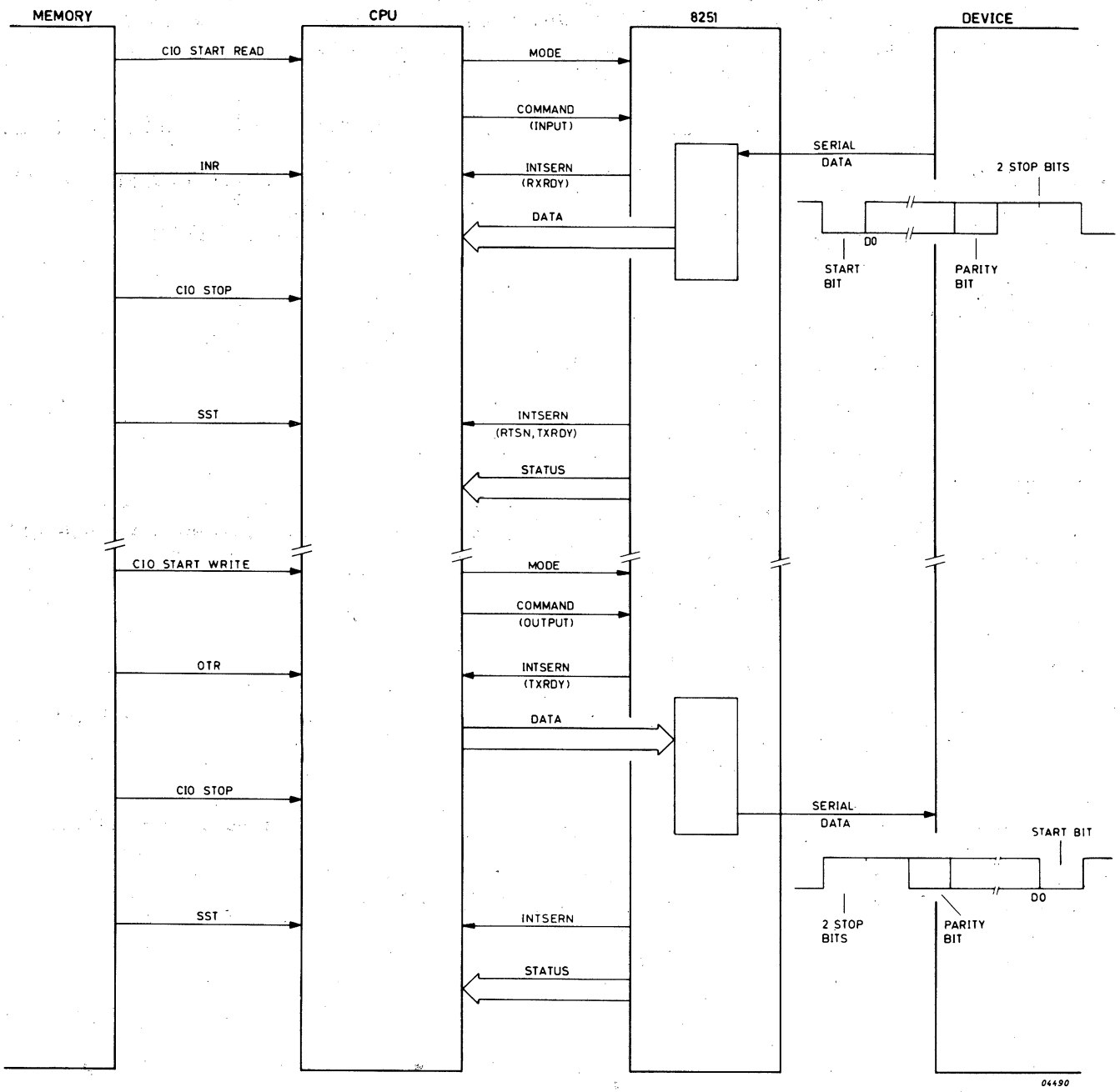


Figure 8.15 V24 PERIPHERAL INTERFACE DIALOGUES

8.5 CPU ARCHITECTURE CP7E (FIGURE 8.14)

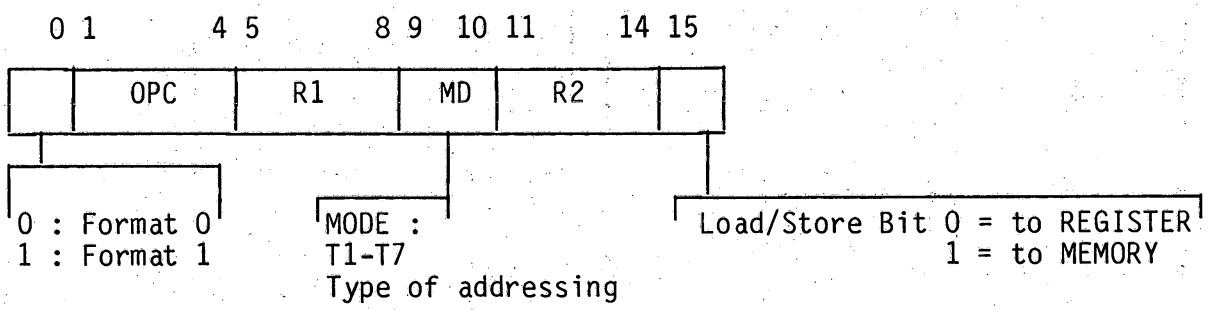
The CPU consists of three microprocessors linked together via internal busses, multiplexers etc. and by the microprogram.

4x MP 2901A: 4 bits microprocessor specially used for arithmetic operations.
Contains SCRATCHPAD registers: A1-A15 (reg. 0 for internal use in microprogram).
Q register: used for SHIFT instructions.

4x MP 2932 : 4 bits microprocessor used for PROGRAM COUNTER, A0 register.

1x MP 2910 : Used for microprogram control. Contains MICROPROGRAM COUNTER.
RCT COUNTER: for creating delay times, repeating certain actions a number of times.

Instruction format (on "D" bus and in K register):



MADE : MAD Extension 8 bits
PLACR : Programmable Logic Array controlling Condition Register
PSW : PLR Program Level Register
CR Condition Register
GF General Field
ALUX : 16-Bits Register (2x 8 bits)
Exchange of two bytes in one word: e.g. Character Exchange Instruction
PLAMAP : Decoding of instruction types and format 0 OPC's
PLAVEC : Decoding format 1 instructions : OPERATION CODE

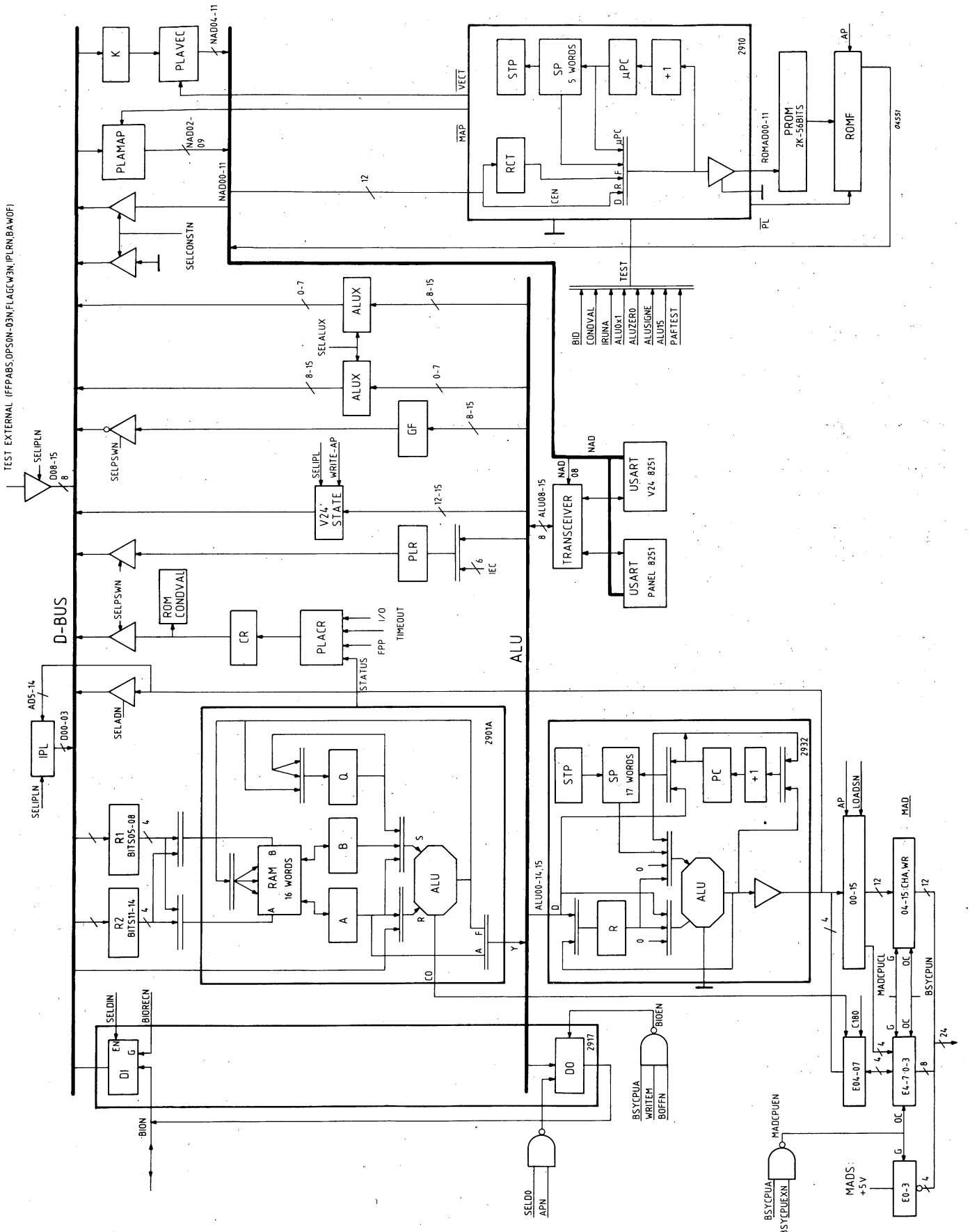
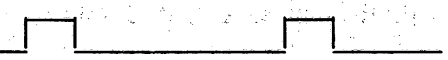


Figure 8.16 CPU BLOCKDIAGRAM

8.6 CPU TIMING

CPU TIMING

Each AP puls is the start of the next micro-instruction.

AP 

The sequensor has 3 fixed cycle lengths and a wait cycle.

CY 225 : 225 n/sec.
CY 270 : 270 n/sec.
CY 360 : 360 n/sec.

WAIT CYCLE

If a WAIT cycle is ordered the time between 2 AP pulses is undefined. This wait cycle is only effective when dealing with a bus transfer e.g. waiting for signal TSM which starts sequencer again.

AP 

WAIT CYCLE (max. 11.5 uS)

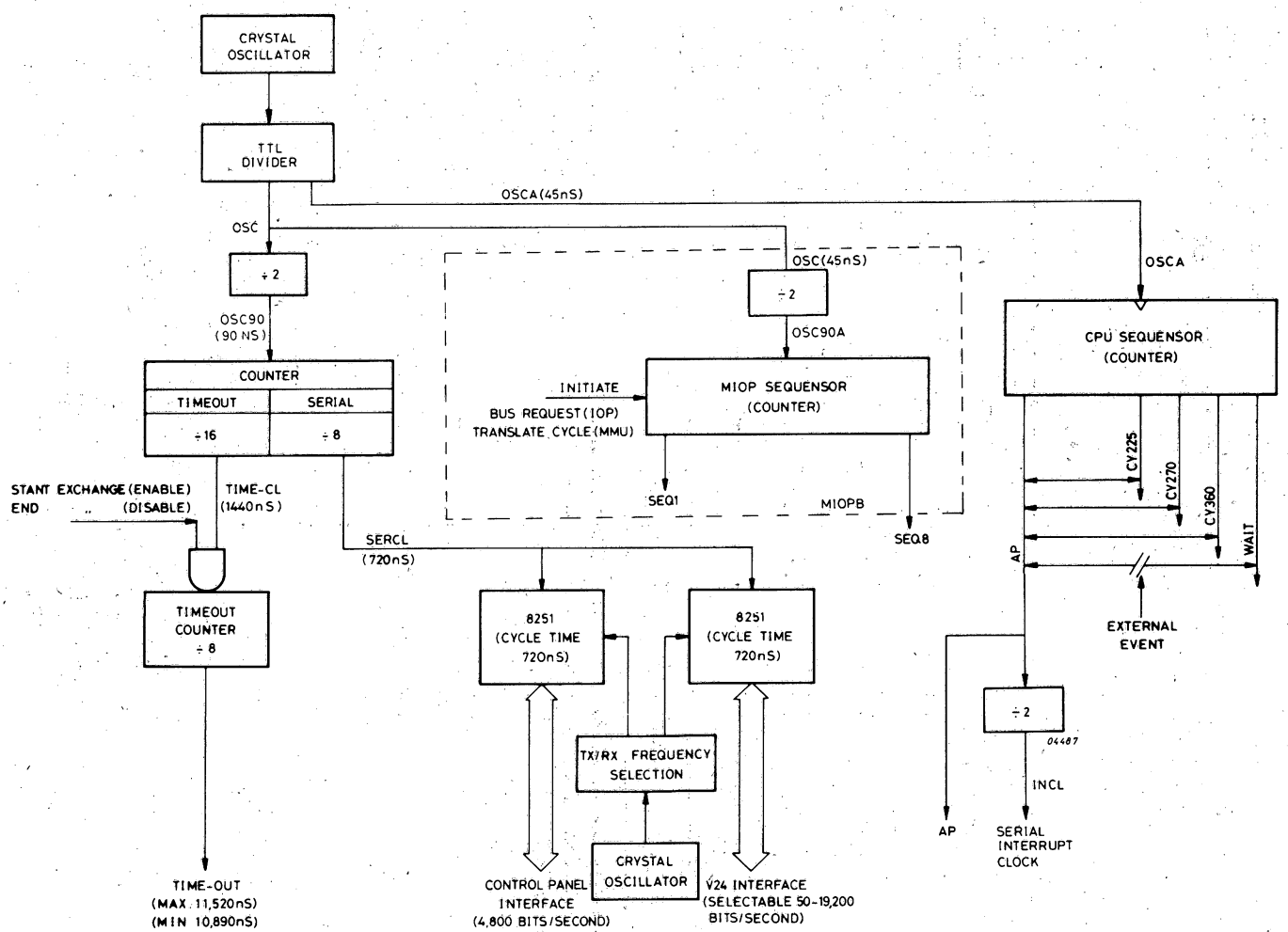


Figure 8.17 P857E SYSTEM CLOCKS

8.7 POWER SWITCH ON AND TEST

At switch-on a sequence of events takes place before the system is ready to go. This sequence of events may be considered as three separate phases.

. Phase 1 Automatic Test
. Phase 2 Microdiagnostic Test (only necessary if problems are expected)
. Phase 3 Load IPL (Initial Program Loader)

The hexadecimal codes of the HHCP and FRCP that are displayed after an event are indicated in the following flowcharts.

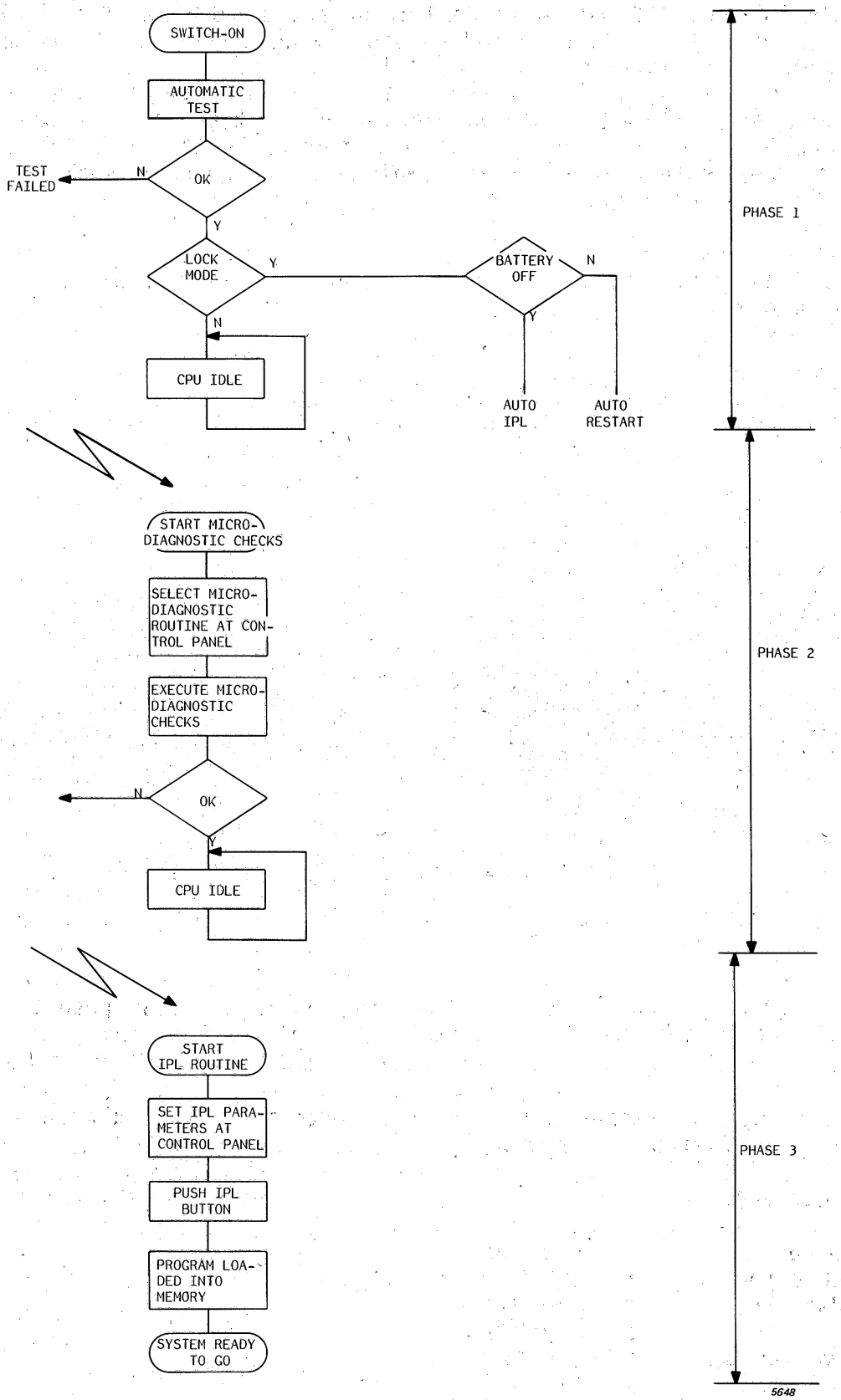


Figure 8.18 START PROCEDURE

8.7.1 AUTOMATIC TEST

An automatic test is executed at the power-on time. It tests the major part of the C.P.U., the Control Panel Interface, a part of the Control Panel itself and its cable. This test is terminated by displaying a code (FFFC) if the panel was not in LOCK state and if the test was O.K.

This automatic part of the test is of "go-no go" type. If the expected code is not displayed it is not possible to distinguish if the problem is due to the C.P.U., to the Control Panel or its cable and it is not possible to run further tests.

But if this first phase runs well and if displaying is possible and correct, in the second phase the C.P.U., C.U. and Memory failures could be distinguished from one another.

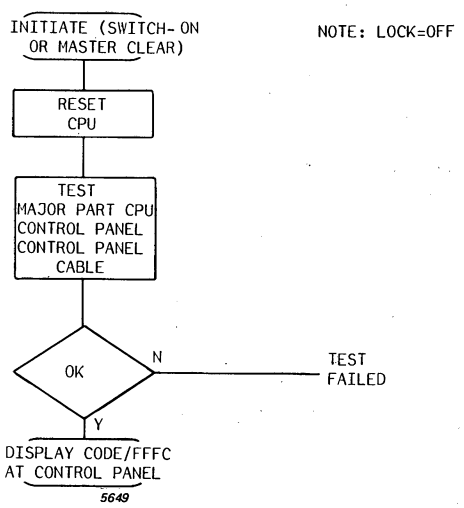


Figure 8.19 AUTOMATIC TEST

8.7.2 MICRODIAGNOSTIC TEST

The second phase is initialized by pressing the Ø and TEST push buttons on the Control Panel and it consists of the end of the C.P.U. test, RAM test (up to 32K), CPU-CU V24 (Address /10) dialogue test and MMU/IOP (MIOP) test.

At the end of this second phase, another code is displayed meaning either the correct end of test or an error.

These codes are:

C.P.U. error : Code 0001
BUS or CU error : Code 0002 or YY02
BUS or RAM error : Code XX03
O.K. : Code YY04
MIOP error or absent : Code YY10

XX = Most significant 8 bits of the memory address causing the error.
YY = Most significant 8 bits of the last memory address.

The operator can read the address causing the error in A1, and the contents of this address read by the CPU in A2.

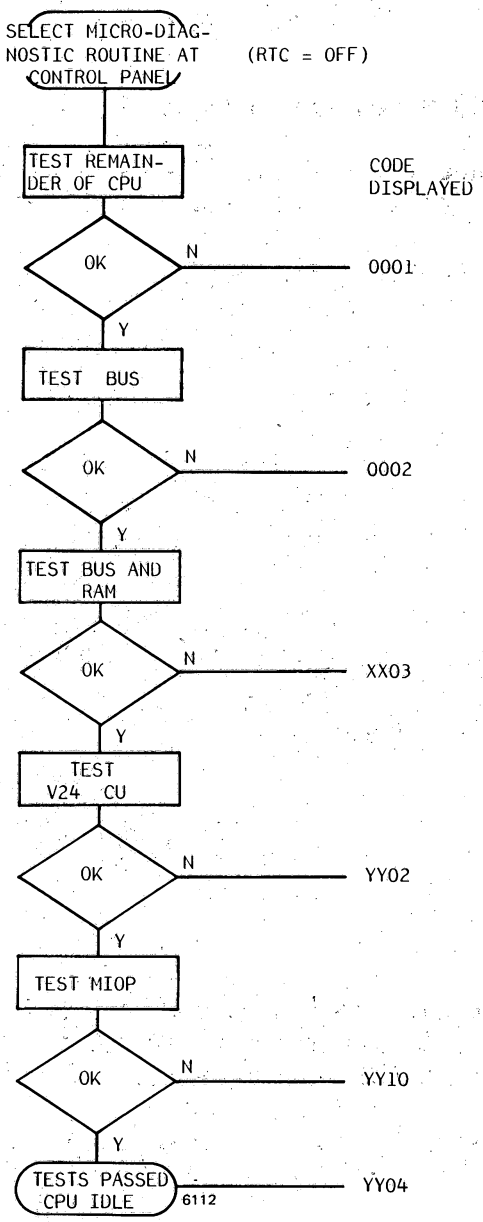


Figure 8.20 MICRODIAGNOSTIC TEST

8.8 SHORT DESCRIPTION OF TESTPROGRAMS

Testprogram CP 57 RE

Mem. size 8 Kw.
No output on CTW.
No power failure - or - RTC allowed.

Procedure:

. IPL

- Program stops on /0300 = restart address
- MCL, RUN
- Program loops continuously. Address /024A contains the number of passes.
- Error: program stops. Halt address indicates faulty instruction in listing.

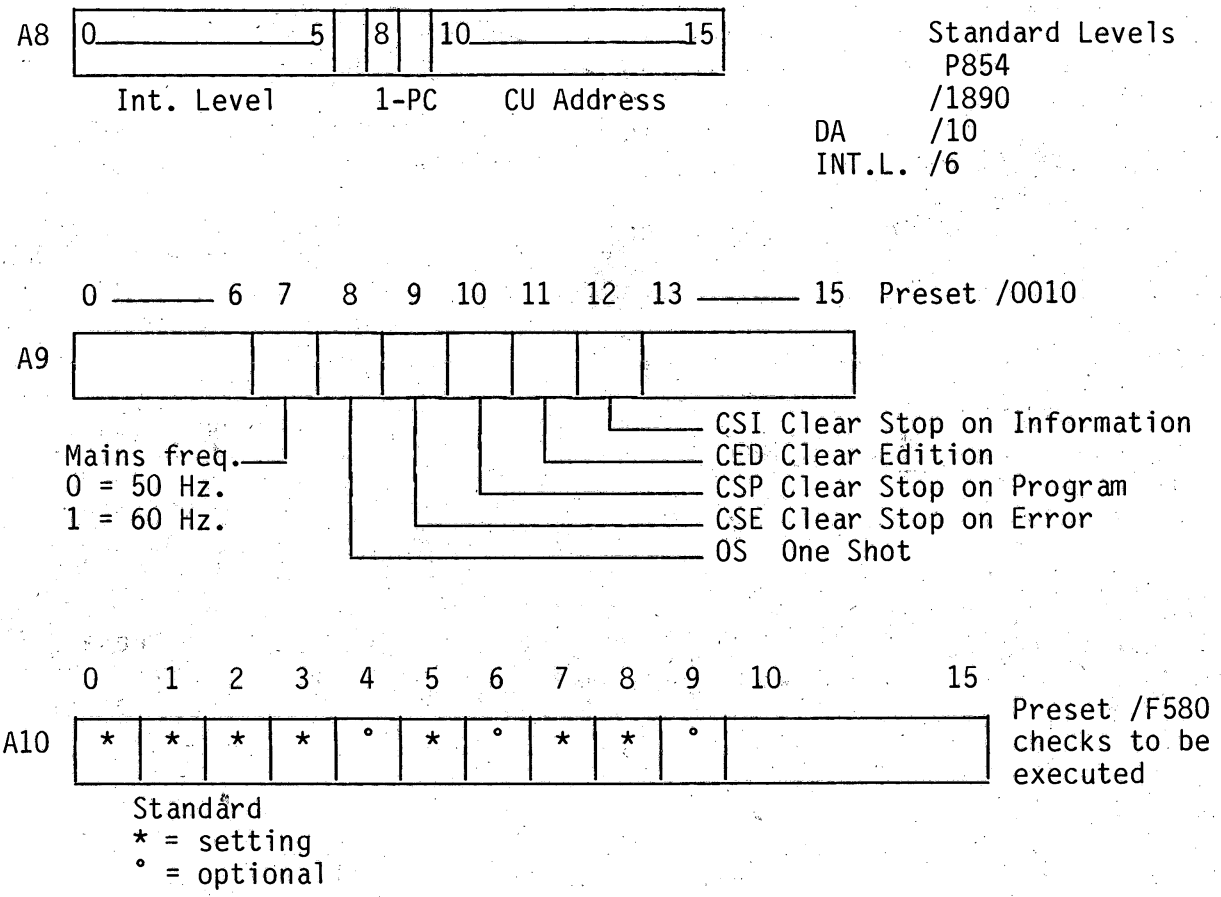
One complete CPU test lasts 2 - 4 seconds.

1. IPL

   Program stops at /700 = restart address and normal end.

2. Switch on RTC (PF/AR also possible).

3.



4. Clear bit 11 of A9 (check no written on DA/10).
   Depress MC, RUN
   Interrupts return to address /700
   Error stop /5F0
   Restart after power off /6EE

   Special operator actions:
   IF0001 type in a character within 10 seconds
   IF0003 type in characters begin with LF, CR, end with $
   IF0005 type in 2 characters within 3 seconds

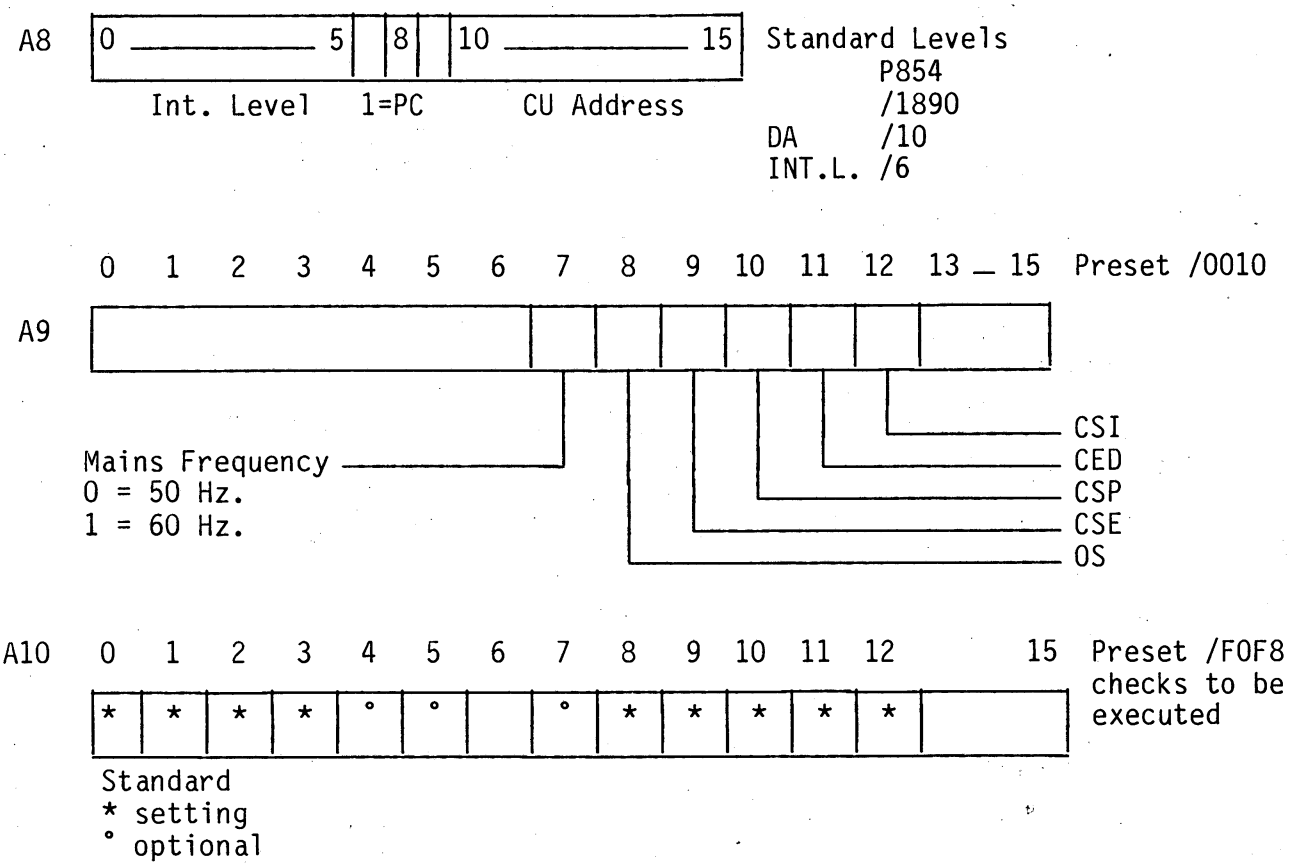
For more information see official description of testprogram.

1. IPL

   Program stops at /700 = restart address and normal end.

2. Switch on RTC (PF/AR also possible).

3.



4. Clear bit 11 of A9 (check no written on DA/10).
   Depress MC, RUN

   Error stop /5F0
   Restart after power off /6EE
   Interrupts return to /700
   Special operator actions:
   IF0001 type in a character within 10 seconds
   IF0003 type in characters begin with LF, CR, end with $.

For more information see official description of testprogram.

8.9 SHORT ROUTINES

ASR, PTS 3100 AND DISPLAY

These peripherals and their CU's can be checked with the aid of two small programs called Line, and Echo, if the standard test program either cannot be loaded or if it will not run.

PROGRAM LINE

MEMORY ADDRESS	DATE	PROGRAM INSTRUCTION		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0200		LDK	A2, 0
008A	4BD0		SST	A3,/10
008C	42D0		CIO	A2,1,/10
008E	5C04		RB(NA)	* -2
0090	8520	OUTCR	LDKL	A5,/0A0D
0092	0A0D			
0094	4510	OUT	OTR	A5,0,/10
0096	5C04		RB(NA)	* -2
0098	3D68		SRL	A5,8
009A	5C08		RB(NZ)	OUT
009C	4610	OUTCH	OTR	A6,0,/10
009E	5C04		RB(NA)	* -2
00A0	1201		ADK	A2,1
00A2	EA1C		CWR	A2,A7
00A4	5C0A		RB(NE)	OUTCH
00A6	0200		LDK	A2,0
00A8	5F1A		RB	OUTCR

* Load the ASCII character in register A6
* Load the number of times you wish the character to be repeated into register A7.
* Load the start address of the program into register A0 (/0086).
* Push the MCL and RUN button

MEMORY ADDRESS	DATA	PROGRAM INSTRUCTIONS		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0221	IN	LDK	A2,/21
008A	42D0		CIO	A2,1,/10
008C	5C04		RB(NA)	* -2
008E	4B10		INR	A3,0,/10
0090	5C04		RB(NA)	* -2
0092	4290		CIO	A2,0,/10
0094	4CD0		SST	A4,/10
0096	5C04		RB(NA)	* -2
0098	0200		LDK	A2,0
009A	42D0		CIO	A2,1,/10
009C	5C04		RB(NA)	* -2
009E	4310		OTR	A3,0,/10
00A0	5C04		RB(NA)	* -2
00A2	4290		CIO	A2,0,/10
00A4	4CD0		SST	A4,/10
00A6	5C04		RB)NA)	* -2
00A8	5F24		RB	IN

Program Echo:

Once loaded and started any input character from the keyboard will be printed, displayed or executed on the device.

9 P876 CPU CP2B (CIPC, CIPA, CIPB, CIPG, CIPF)

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9.1 P876 CPU IDENTIFICATIONS

- Type No.: P876-400 (RAL22F rack)

- Test Programs CPU - CP1/2B
  - MMU2B
  - PAF2B

- Power Consumption:

Technology:	+5VL F/S	+12VL	-12VL
CIPC	2.5A/3.4A	0.06A	0.035A
CIPA	4.4A/5.7A		
CIPB	3.9A/6.1A		
CIPG	3.5A/4.6A		
CIPF	3.3A/4.7A		

12 NC code on the sticker of the board:

CIPC	5111 199 5834x	(5322 216 21293)
CIPA	5111 199 5839x	(5322 216 21295)
CIPB	5111 199 5835x	(5322 216 21294)
CIPG	5111 199 5805x	(5322 216 21315)
CIPF	5111 199 5753x	(5322 216 21314)

5 slots Back Panel 5111 199 5757x

Interconn. Cables 6x 5111 199 5635x (5322 321 20884)

x = modification level

9.2 INSTALLATION

The following instructions are only intended to highlight the important aspects of installing this system.

- Insert the Eurorack into the front of the cabinet and screw into position.
- Ensure that the mains are connected in accordance with the specification (this may differ depending upon the country of installation).
- Ensure that the Gounding Rules are observed.
- Check the U-links before inserting cards into the Eurorack.
- Ensure that the cables between Control Units and Devices are firmly secured and that the screens of these cables are connected in accordance with the Grounding Rules.
- Ensure that the CP2B cards are interconnected correctly with 6 flat cables at frontside.
- Interrupts and Breaks must be wired so that they run across the printed circuit and NOT parallel to it (see below).

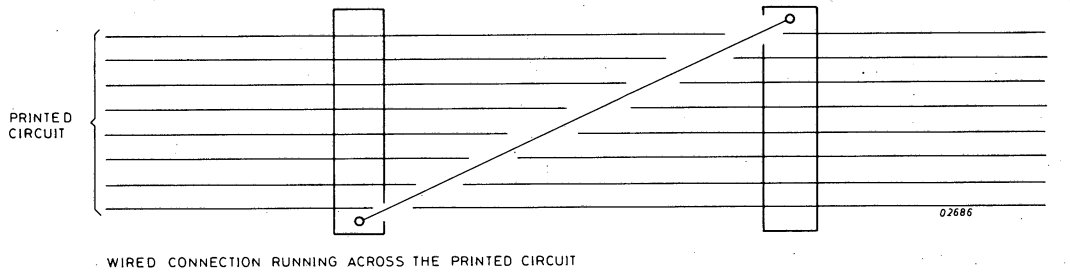


Figure 9.1 WIRING SYSTEM FOR BREAKS OR INTERRUPT

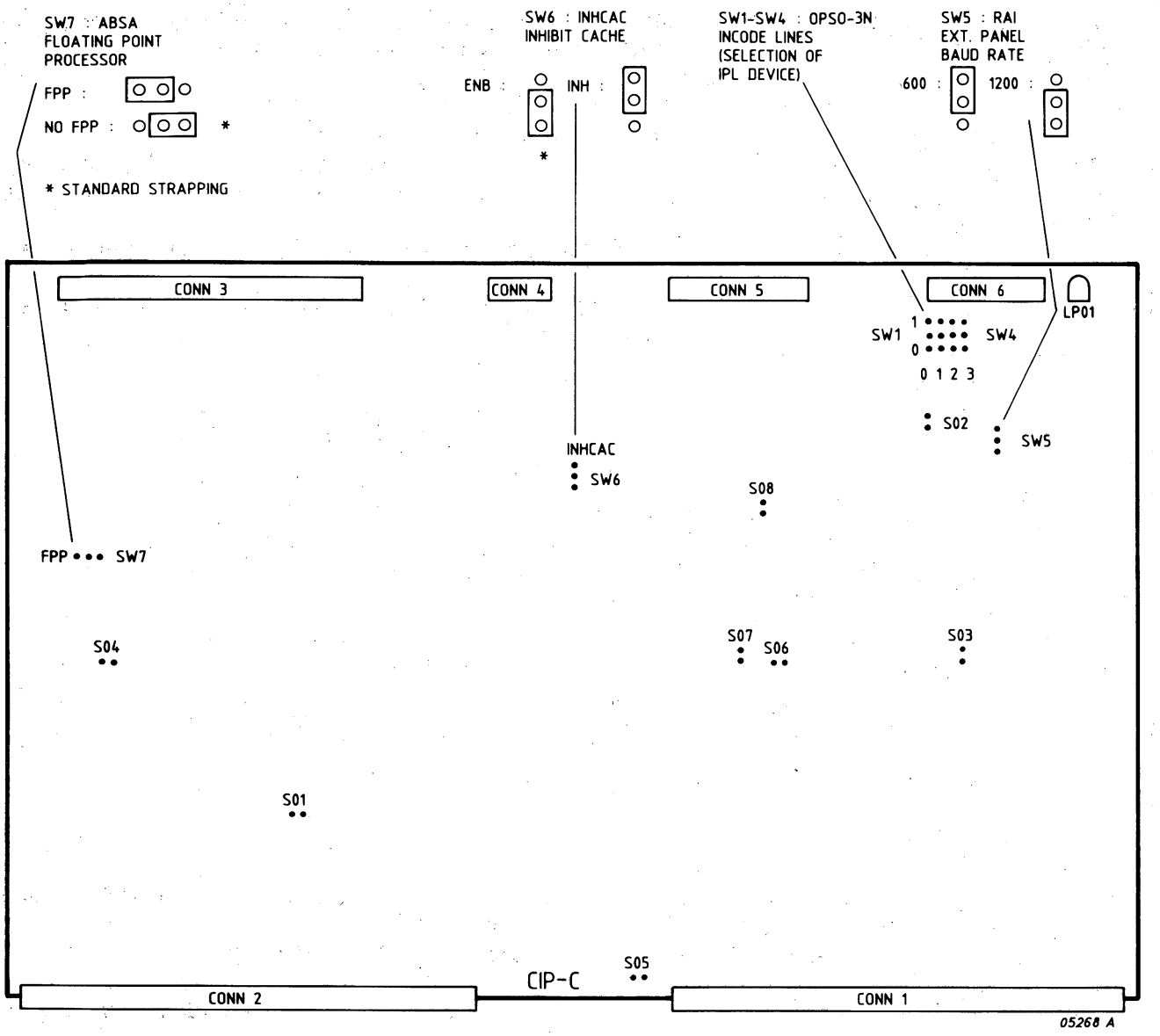
9.2.1 STRAP SETTINGS

There are U-links fitted to all 5 cards of the CP2B. Most U-links are workshop-test links and must normally always be fitted.
On 2 cards there are also U-links for selection of the following:

- CARD C - SW1, 2, 3 and 4 : Selection of IPL device for remote and/or automatic IPL
  - SW5 : 600 BAUD Extended Serial Panel
    1200 BAUD Extended Serial Panel
  - SW6 : Inhibit Cache Momory
    Enable Cache Memory (see Panel functions)
  - SW7 : Floating Point Processor present
    Floating Point Processor not present

- CARD F - SW1 : Internal or External Clock
  - SW2* : UPL or GPBS Control Unit, type selection
  - SW3 : ROMER (special purpose)
  - SW14 : Floating Point/USART- Clock adjustment

* Note: SW2 must be selected for UPL normally, but when one (ore more) CU is of GPBS type, SW2 must be in position GPBS.

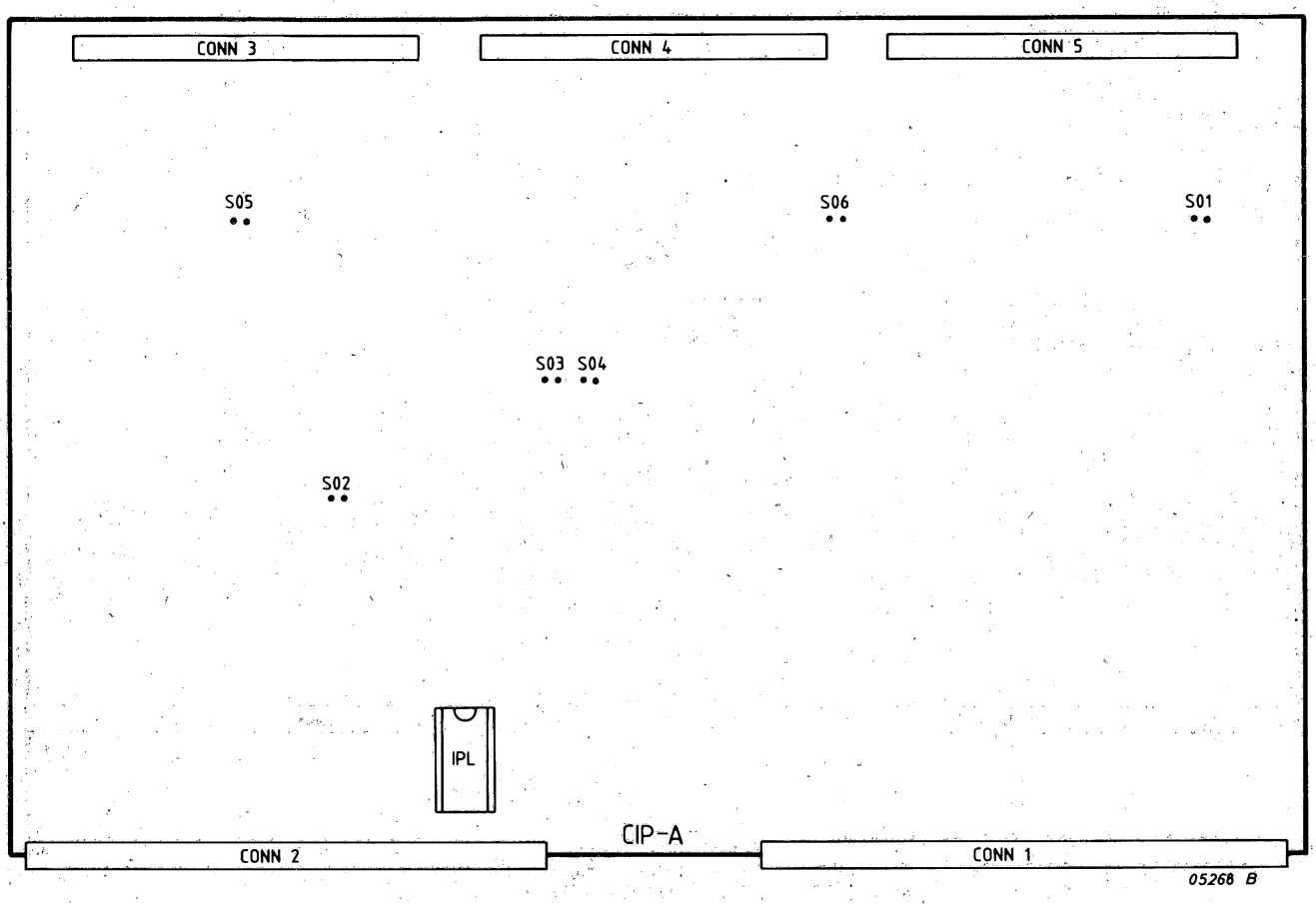


S01-S08 MUST BE FITTED (TEST PURPOSE)

LP01 : ON = CACHE INHIBITED
OFF = CACHE ENABLED

S01	: CRC1	CONDITION REGISTER ENABLE
S02	: FTX	USART (8251) TRANSMIT/RECEIVE CLOCK
S03	: PUPMHN	PANEL FUNCTIONS ENABLE
S04	: CRC4	ROM ENABLE
S05	: CRC5	PARALLEL INTERRUPT ENABLE
S06	: SIRBCI	BCI INTERRUPT ENABLE
S07	: OSC50	BCI CLOCK ENABLE
S08	: INCLA	USART (8251) CLOCK ENABLE

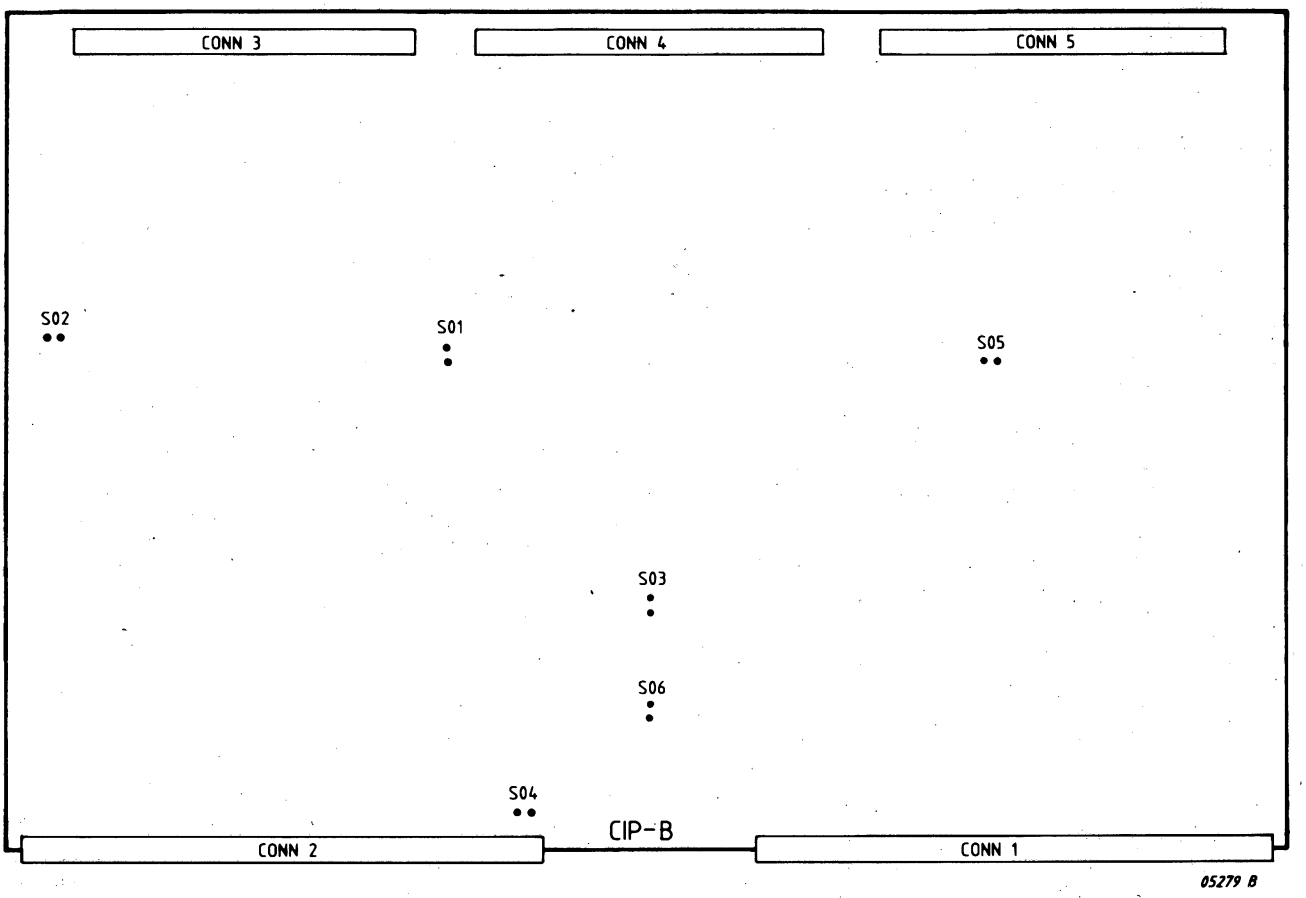
Figure 9.2 CIP-C U LINKS



S01-S06 MUST BE FITTED (TEST PURPOSE)

S01 : GRA1 29705 (SRATCH PAD) ENABLE
S02 : GRA2 ROM ENABLE
S03 : GRA3 PLAD, PLAEX ENABLE
S04 : GRA4 TEST ENABLE (JUMP CONDITIONS MICRO PROGRAM)
S05 : GRA5 PAL 16L8 ENABLE
S06 : GRA6 R1-,R2 FIELD ENABLE

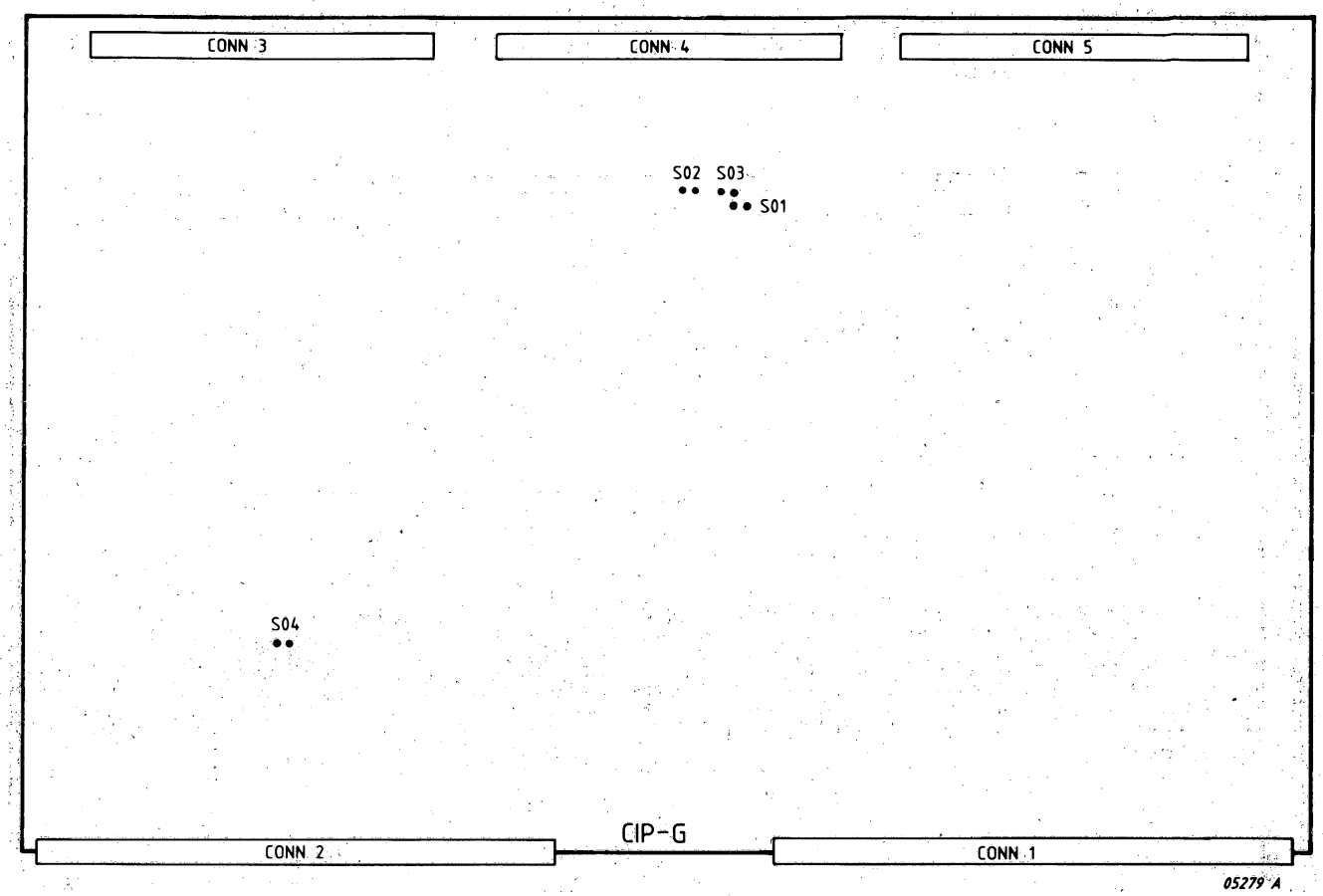
Figure 9.3 CIP-A U-LINKS



S01------S06 MUST BE FITTED (TEST PURPOSE)

S01	GRB1	PLA-CONTROL ENABLE
S02	PSPKN	K-REGISTER INPUT MULTIPLEXER ENABLE
S03	GRB3	PROGRAM COUNTER ENABLE
S04	GRB4	ROM ENABLE
S05	GRB5	ROM-CONSTANT ENABLE
S06	GRB6	PROGRAM COUNTER COMMAND REGISTER ENABLE

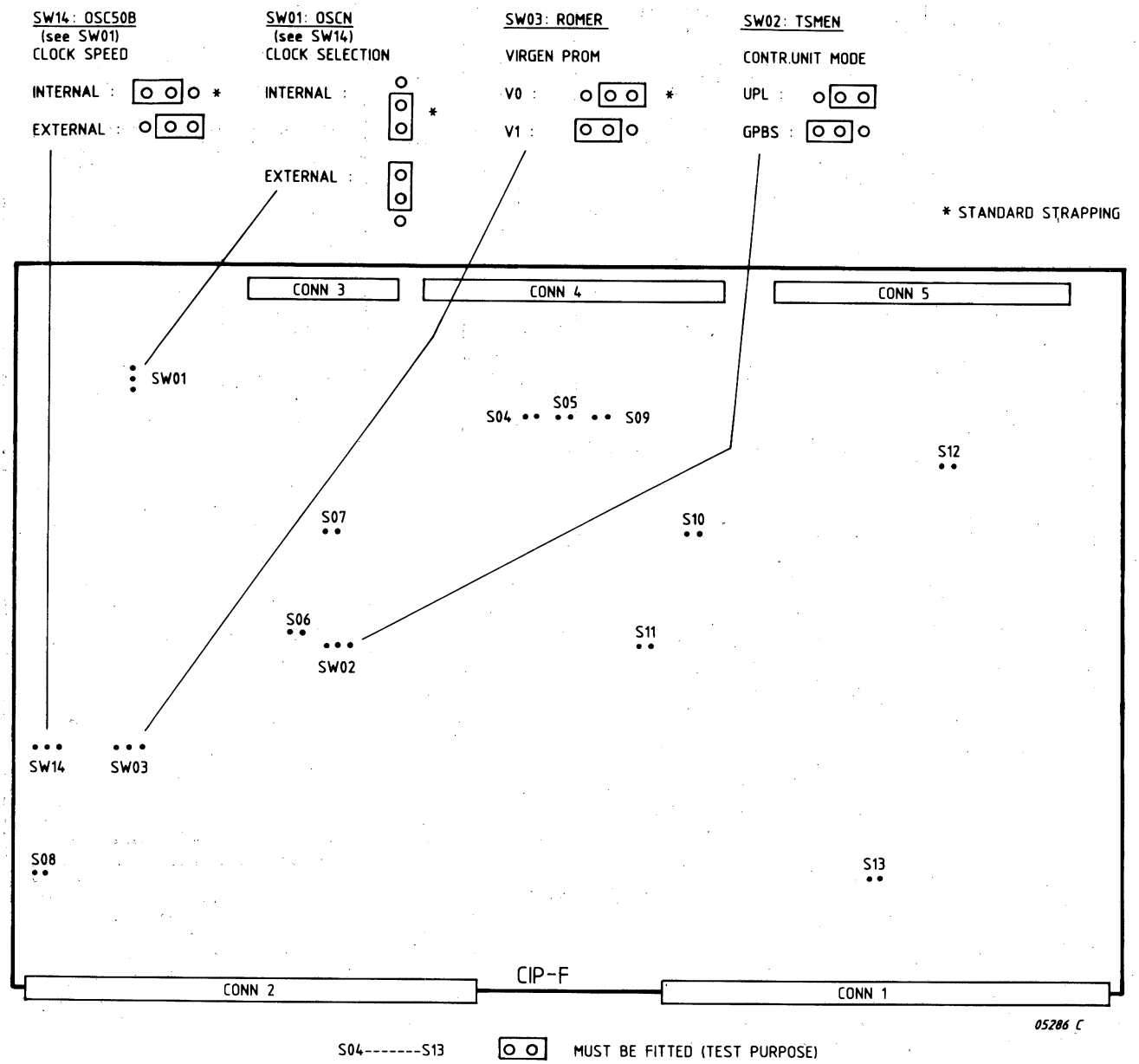
Figure 9.4 CIP-B U-LINKS



S01---S04 MUST BE FITTED (TEST PURPOSE)

S01 : COMPC
S02 : COMPCI
S03 : COMPD
S04 : FPOFF PRESET ENABLE

Figure 9.5 CIP-G U-LINKS



S04-------S13 MUST BE FITTED (TEST PURPOSE)

S04 :	COMPA	
S05 :	COMPB	
S06 :	DHIT	HIT Detection, Restart Sequensor enable
S07 :	CLK75	
S08 :	CLMAD	
S09 :	CSGRF5	
S10 :	WEAN	Write Enable CACHE A
S11 :	WEBN	Write Enable CACHE B
S12 :	EDRVAN	Enable Drivers CACHE A
S13 :	EDRVBN	Enable Drivers CACHE B

Figure 9.6 CIP-F U-LINKS

3	2	1	0	IPL WORD	MEMORY ADDRESS HEX
OPS3N	OPS2N	OPS1N	OPSON		
0	0	0	0	0	1FE
0	0	0	1	1	1FC
0	0	1	0	2	1FA
0	0	1	1	3	1F8
0	1	0	0	4	1F6
0	1	0	1	5	1F4
0	1	1	0	6	1F2
0	1	1	1	7	1F0
1	0	0	0	8	1EE
1	0	0	1	9	1EC
1	0	1	0	10	1EA
1	0	1	1	11	1E8
1	1	0	0	12	1E6
1	1	0	1	13	1E4
1	1	1	0	14	1E2
1	1	1	1	15	1E0

The following diagram shows the identification that is silkscreened on the card C and an example of word selection.

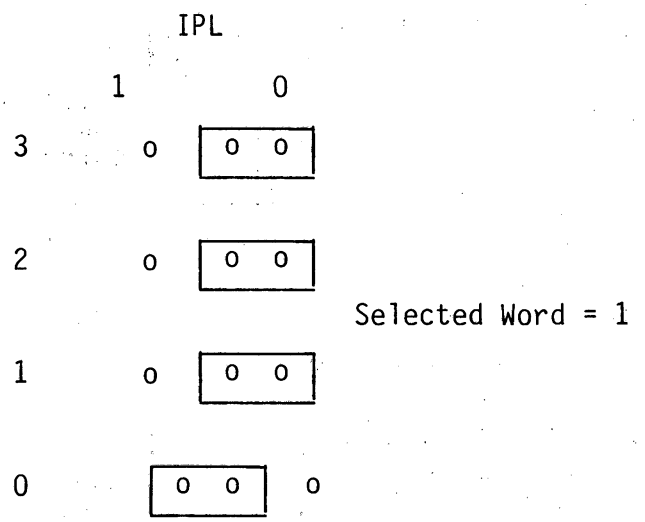


Table 9.1 SELECT IPL DEVICE (REMOTE OR AUTOMATIC IPL)

9.2.2 CONFIGURATION RULES

The following rules must be taken in account:

- Cards C, A. B, G and F must be in the rack position 1, 2, 3, 4 and 5 respectively.
- Other Masters follow in order of their system priority, determined by OKO-OKI links.
- When present the Floating Point Processor (FPPE) must be located at cardposition 6 and 7.
  On connector 2, dedicated wiring is necessary between the F card of the CP2B (5 slots backpanel) and the FPPE (2 slots backpanel).
- The UPL-Bus must not be extended out of the basic Eurorack without the signals being terminated.
- The recommended card location for TUGP is 23.

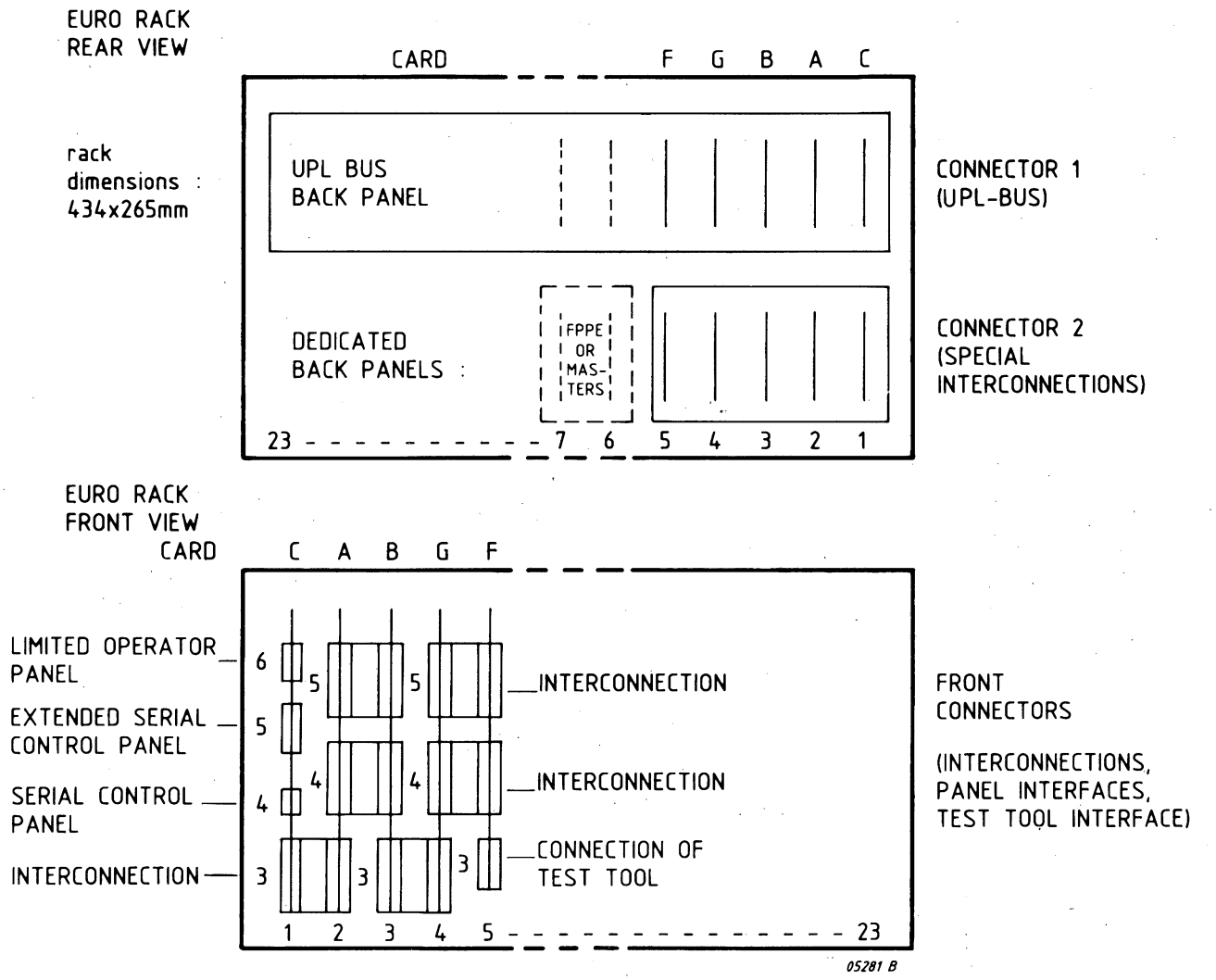


Figure 9.7 EURORACK REAR AND FRONT VIEW

9.3 INTERFACES

All Double Eurocards have 1 or 2 connectors for connection to the backpanel of the P876 (RAL22F) rack:

- connector 1 : UPL Bus
- connector 2 : Interconnection if multiple-card unit

Most cards also have connectors for connections at the frontside e.g. for Control Panels, devices or interconnections.

The figure shows the dimensions of all cards and the system of pinning and numbering of connectors on the card CIP-C.
In general the same system is used for all cards except that the pinning/ numbering of connectors 3, 4, etc. may differ for some cards.

For all CP2B cards the numbering of the connectors and their pins starts from connector 1 pin 1 and continues in a clockwise direction around the card as indicated in the figure.
The maximum height of components is less than 10mm.
Each card will occupy then only 1 slot in the card rack.

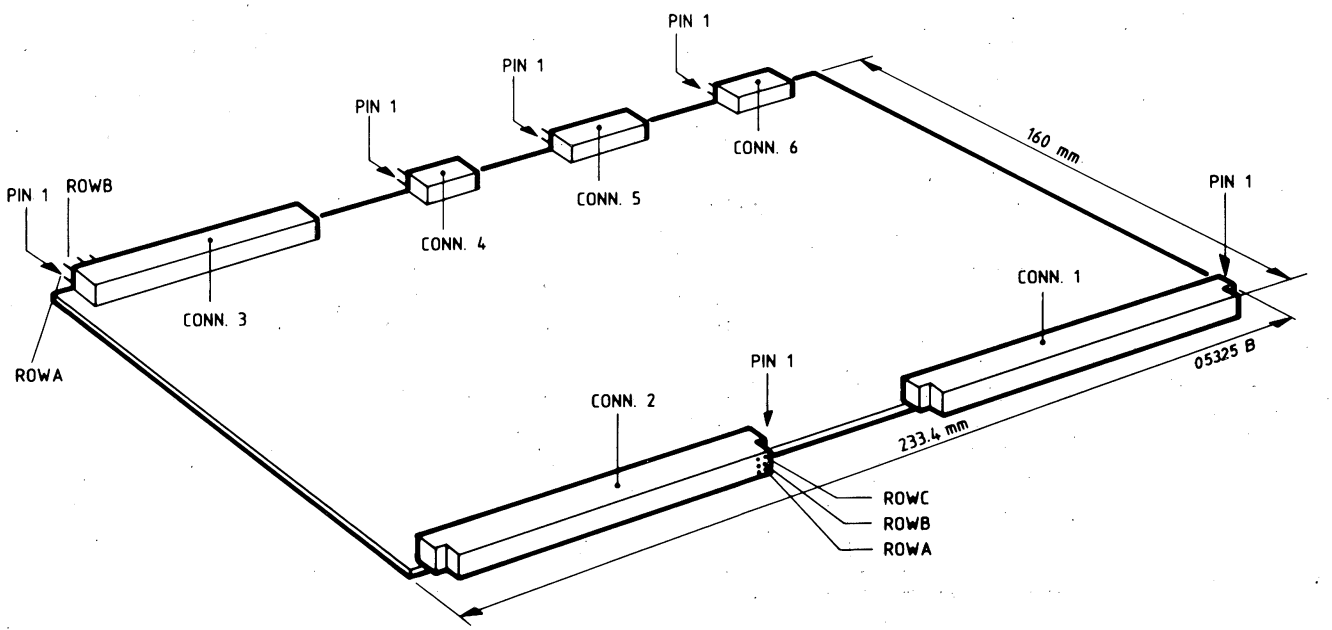


Figure 9.8 EUROCARD FORMAT (CIP-C)

9.3.1 INTERFACES SIGNALS AND PINS

All interface signals of the CP2B are listed in the following tables:

- 1.3a, b, c, d, e - UPL-BUS CONNECTOR 1
- 1.4 - INTERCONNECTIONS CONNECTOR 2
- 1.5a, b, c, d - INTERCONNECTIONS FRONT CONNECTORS
- 1.6a, b, c - PANEL INTERFACE CONNECTORS
- 1.7 - TEST INTERFACE CONNECTOR

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01	+12VL	1B01	ERQN	1A01	-12VL
1C02		1B02	BUSRN	1A02	
1C03	BCI	1B03	MSN	1A03	INCL
1C04	IR12N	1B04	0V	1A04	IR14N
1C05	IR13N	1B05	BSYN	1A05	IR15N
1C06	0V	1B06	OKO	1A06	0V
1C07	PWFN	1B07	RIPLN	1A07	
1C08	CLEARN	1B08	RTCN	1A08	ACN
1C09	0V	1B09	BAWOFN	1A09	0V
1C10	TMPN	1B10	STOPN	1A10	TSMN
1C11	TMEN	1B11	0V	1A11	TMRN
1C12	0V	1B12		1A12	0V
1C13		1B13		1A13	
1C14		1B14	0V	1A14	
1C15		1B15		1A15	
1C16		1B16		1A16	
1C17		1B17		1A17	
1C18		1B18		1A18	
1C19		1B19		1A19	
1C20		1B20		1A20	
1C21		1B21	0V	1A21	
1C22	0V	1B22	IRO4N	1A22	0V
1C23		1B23	IRO5N	1A23	
1C24		1B24	IRO6N	1A24	
1C25		1B25	IRO7N	1A25	
1C26		1B26	0V	1A26	
1C27		1B27	IRO8N	1A27	
1C28		1B28	IRO9N	1A28	
1C29		1B29	IR10N	1A29	
1C30		1B30	IR11N	1A30	
1C31		1B31	+5VL	1A31	
1C32	+5VL	1B32	+5VL	1A32	+5VL

Table 9.2a UPL-BUS CONNECTOR PINNING CARD C

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01		1B01		1A01	
1C02		1B02		1A02	
1C03		1B03		1A03	
1C04		1B04	0V	1A04	
1C05		1B05		1A05	
1C06	0V	1B06	0K0	1A06	0V
1C07		1B07	0K0	1A07	
1C08		1B08		1A08	
1C09	0V	1B09		1A09	0V
1C10		1B10		1A10	
1C11		1B11	0V	1A11	
1C12	0V	1B12		1A12	0V
1C13		1B13		1A13	
1C14		1B14	0V	1A14	
1C15		1B15		1A15	
1C16		1B16		1A16	
1C17		1B17		1A17	
1C18		1B18		1A18	
1C19		1B19		1A19	
1C20		1B20		1A20	
1C21		1B21	0V	1A21	
1C22	0V	1B22	IR16N	1A22	0V
1C23		1B23	IR17N	1A23	
1C24		1B24	IR18N	1A24	
1C25		1B25	IR19N	1A25	
1C26		1B26	0V	1A26	
1C27		1B27	IR20N	1A27	
1C28		1B28	IR21N	1A28	
1C29		1B29	IR22N	1A29	
1C30		1B30	IR23N	1A30	
1C31		1B31	+5VL	1A31	
1C32	+5VL	1B32	+5VL	1A32	+5VL

Table 9.2b UPL-BUS CONNECTOR PINNING CARD A

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01		1B01		1A01	
1C02		1B02		1A02	
1C03		1B03		1A03	
1C04		1B04	0V	1A04	
1C05		1B05		1A05	
1C06	0V	1B06	0K0	1A06	0V
1C07		1B07	0K0	1A07	
1C08		1B08		1A08	
1C09	0V	1B09		1A09	0V
1C10		1B10		1A10	
1C11		1B11	0V	1A11	
1C12	0V	1B12		1A12	0V
1C13		1B13		1A13	
1C14		1B14	0V	1A14	
1C15		1B15		1A15	
1C16		1B16		1A16	
1C17		1B17		1A17	
1C18		1B18		1A18	
1C19		1B19		1A19	
1C20		1B20		1A20	
1C21		1B21	0V	1A21	
1C22	0V	1B22	IR24N	1A22	0V
1C23		1B23	IR25N	1A23	
1C24		1B24	IR26N	1A24	
1C25		1B25	IR27N	1A25	
1C26		1B26	0V	1A26	
1C27		1B27	IR28N	1A27	
1C28		1B28	IR29N	1A28	
1C29		1B29	IR30N	1A29	
1C30		1B30	IR31N	1A30	
1C31		1B31	+5VL	1A31	
1C32	+5VL	1B32	+5VL	1A32	+5VL

Table 9.2c UPL-BUS CONNECTOR PINNING CARD B

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01		1B01		1A01	
1C02		1B02		1A02	
1C03		1B03		1A03	
1C04		1B04	0V	1A04	
1C05		1B05		1A05	
1C06	0V	1B06	OK0	1A06	0V
1C07		1B07	OK0	1A07	
1C08		1B08		1A08	
1C09	0V	1B09		1A09	0V
1C10		1B10		1A10	
1C11		1B11	0V	1A11	
1C12	0V	1B12	MADE0	1A12	0V
1C13	MAD00	1B13	MADE1	1A13	MAD01
1C14	MAD02	1B14	0V	1A14	MAD03
1C15	MAD04	1B15	MADE2	1A15	MAD05
1C16	MAD06	1B16	MADE3	1A16	MAD07
1C17	MAD08	1B17	MADE4	1A17	MAD09
1C18	MAD10	1B18	MADE5	1A18	MAD11
1C19	MAD12	1B19	MADE6	1A19	MAD13
1C20	MAD14	1B20	MADE7	1A20	MAD15
1C21		1B21	0V	1A21	
1C22	0V	1B22		1A22	0V
1C23	BI008N	1B23		1A23	BI000N
1C24	BI009N	1B24		1A24	BI001N
1C25	BI010N	1B25		1A25	BI002N
1C26	BI011N	1B26	0V	1A26	BI003N
1C27	BI012N	1B27		1A27	BI004N
1C28	BI013N	1B28		1A28	BI005N
1C29	BI014N	1B29		1A29	BI006N
1C30	BI015N	1B30		1A30	BI007N
1C31		1B31	+5VL	1A31	
1C32	+5VL	1B32	+5VL	1A32	+5VL

Table 9.2d UPL-BUS CONNECTOR PINNING CARD G

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01		1B01		1A01	
1C02		1B02		1A02	
1C03		1B03		1A03	
1C04		1B04	0V	1A04	
1C05		1B05	BSYN	1A05	
1C06	0V	1B06	0K0	1A06	0V
1C07		1B07	0K0	1A07	RSLN
1C08		1B08		1A08	
1C09	0V	1B09		1A09	0V
1C10	TMPN	1B10		1A10	TSMN
1C11	TMEN	1B11	0V	1A11	TMRN
1C12	0V	1B12		1A12	0V
1C13		1B13		1A13	
1C14		1B14	0V	1A14	
1C15		1B15		1A15	
1C16		1B16		1A16	
1C17		1B17		1A17	
1C18		1B18		1A18	
1C19		1B19		1A19	
1C20		1B20		1A20	
1C21	CHA	1B21	0V	1A21	WRITE
1C22	0V	1B22		1A22	0V
1C23		1B23		1A23	
1C24		1B24		1A24	
1C25		1B25		1A25	
1C26		1B26	0V	1A26	
1C27		1B27		1A27	
1C28		1B28		1A28	
1C29		1B29		1A29	
1C30		1B30		1A30	
1C31		1B31	+5VL	1A31	
1C32	+5VL	1B32	+5VL	1A32	+5VL

Table 9.2e UPL-BUS CONNECTOR PINNING CARD F

Table 9.3 INTERCONNECTIONS CP2B (CONNECTOR 2)

	CIP_F			CIP_G			CIP_B			CIP_A			CIP_C			
	C	B	A	C	B	A	C	B	A	C	B	A	C	B	A	
1	OSC50	0V	CLK50N		0V	CLK50N		0V	CLK50N		0V	CLK50N	OSC50	0V	CLK50N	1
2	0V	CLK75N	0V	0V		0V	0V		0V	0V		0V	0V	CLK75N	0V	2
3	CPB	0V	CPC	CPE	0V	0V	CPB	0V	CPDIV	CPA	0V	CPDIV	CPDIV	0V	CPC	3
4	0V	CPA	CPE	0V			0V	PLIR3	PLIR4	0V	PLIR3	GIR2	GIR2	PLIR3	PLIR4	4
5	OSCFPP *	0V	0V				GIR3	PLIR5	EI3N	EI3N	PLIR5	PLIR4	GIR3	PLIR5	FDONEN	5
6	0V	*FLCR0	FDONEN	0V			0V	15R1N	CVN	0V	FRSLDN	CVN	0V	FLCR1	FLCR0	6
7	DONEFN	*FLCR1	FRSLDN	BC13	BC14	BC15	BC15	BC14	BC13	FU			ENTMRN	15R1N	CVN	7
8	0V	*ENTMRN	FTSMA	FTSMA	ENCACH	BC12	BC12				PFFL		FU	FTSMA	ENCACH	8
9	TMFN *	0V	BUSRQ		0V	BC11	BC11	0V			0V	EI2N	EI2N	0V	BUSRQ	9
10	0V	*FU	0V	CLKMAD		BC10	BC10	ALU00	ALU08	ALU00	ALU01	ALU02	ALU00	ALU01	ALU02	10
11	BSYOKN	*PFFL	ENCACH	EMADN	0V	BC09	BC09	ALU01	ALU09	ALU03	ALU04	ALU05	ALU03	ALU04	ALU05	11
12	0V	*CLKMAD	0V	0V		BC08	BC08	ALU02	ALU10	ALU06	ALU07	ALU08	ALU06	ALU07	ALU08	12
13	PAFTN *	0V	EMADN	ENBION	0V	BC05	BC05	ALU03	ALU11	ALU09	ALU10	ALU11	ALU09	ALU10	ALU11	13
14	0V	*ENBION	0V	ECACHN		BC04	BC04	ALU04	ALU12	ALU12	ALU13	ALU14	ALU12	ALU13	ALU14	14
15	FLOCR0 *	0V	ECACHN	ENBUSN	0V	BC03	BC03	ALU05	ALU13	ALU15	0V		ALU15	0V	BC06	15
16	0V	*ENBUSN	0V	FDCHAN	DCSRAN	BC02	BC02	ALU06	ALU14	0V	KREG05		0V	KREG05	BC07	16
17	FLOCR1 *		FDCHAN	0V	0V	BC01	BC01	ALU07	ALU15	KREG08	KREG07	KREG06	KREG08	KREG07	KREG06	17
18	0V	*DCSRAN		BC00	BC07	BC06	BC07	0V	BC06		0V	KREG09	PUPSTN	0V	KREG09	18
19	FLOACT	*MTMF	0V	PUPSTN	STOPAD	0V	BC00	KREG05	0V				STOPAD	FL125N	FPOFN	19
20	0V	*FRSLAN	FL125N	FPOFN	FRSLAN	ADRUS	KREG07	KREG08	KREG06				ADRUS			20
21	BOFFN *	0V	DPF		0V		FRSLAN	0V	KREG09	FRSLAN	0V		FWPA1N	0V	FWPA2N	21
22	0V	*MGFETC	MFLOAT		FWPA2N	FWPA1N	ROMER	DPF			DPF		MTLTS	MTMF	MBOFF	22
23	GFETCH	*NAD0Z1	MBOFF	MTLTS			RENECH				NAD0Z1		MFLOAT	MGFETC	BRK *	23
24	0V	*MB	MA	0V		MA	MCHA	MB	MA				BRKZON*	MB	MA	24
25	WAITB	0V	RENECH	WAITB	0V	MWRITN	MWRITN	0V	MEX	MWRITN	0V	MEX	MWRITN	0V	MEX	25
26	FECLSN	MTLTS	MCHA	FECLSN	MNIC		MENPRN	MNIC	MPLA1	MENPRN	MNIC	MPLA1	MENPRN	MNIC	MPLA1	26
27	ROMER	MWRITN	0V				MPLA2N	MRCA7N	MRCA5N	MPLA2N	MRCA7N	MRCA5N	MPLA2N	MRCA7N	MRCA5N	27
28			NAD11				MRCA4N	0V	NAD11	MRCA4N	0V	NAD11	MRCA4N	0V	NAD11	28
29	NAD10	NAD09	NAD08				NAD10	NAD09	NAD08	NAD10	NAD09	NAD08	NAD10	NAD09	NAD08	29
30	NAD07	NAD06	NAD05				NAD07	NAD06	NAD05	NAD07	NAD06	NAD05	NAD07	NAD06	NAD05	30
31	NAD04	NAD03	NAD02				NAD04	NAD03	NAD02	NAD04	NAD03	NAD02	NAD04	NAD03	NAD02	31
32	0V	NAD00	NAD01	0V			0V	NAD00	NAD01	0V	NAD00	NAD01	NAD01	NAD00	0V	32

6245

* Note: CIP_C = Console operator interface (SCUZ card). CIP_F = Floating Point Processor interface

BACKPANEL 5111 199 57570

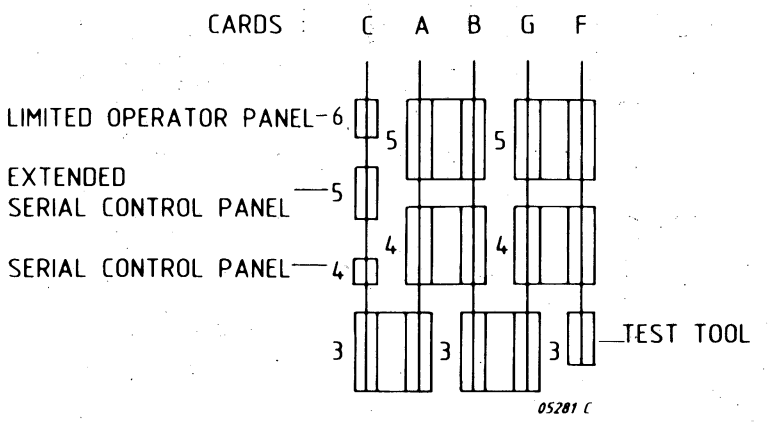


Figure 9.9 FRONT CONNECTORS OF CARDS C, A, B, G AND F

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
3A25	0V	3B25	
24		24	
23		23	
22		22	
21	FRSLDN	21	
20	OVERFL	20	0V
19	FSIGN	19	0V
18	SIG	18	0V
17	FZERO	17	0V
16	ZERO	16	0V
15	ENPSWN	15	0V
14	FK09	14	0V
13	FK08	13	0V
12	FEX	12	0V
11	INTN	11	0V
10	PUPN	10	0V
09	TSTON	09	0V
08	MNAD02	08	0V
07	MNAD03	07	0V
06	MNAD04	06	0V
05	MNAD05	05	0V
04	MXCNT0	04	0V
03	MXCNT1	03	0V
02	MUPCT	02	0V
3A01	MINHCT	3B01	0V

Table 9.4a INTERCONNECTION CARDS C AND A

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
5A25	0V	5B25	ACCU00
24	ACCU01	24	ACCU02
23	ACCU03	23	ACCU04
22	ACCU05	22	ACCU06
21	ACCU07	21	0V
20	ACCU08	20	ACCU09
19	ACCU10	19	ACCU11
18	ACCU12	18	ACCU13
17	ACCU14	17	ACCU15
16	0V	16	PFAC
15	0V	15	RCL00
14	RCL01	14	RCL02
13	RCL03	13	RCL04
12	RCL05	12	RCL06
11	RCL07	11	0V
10	MRCA0N	10	MRCA1N
09	MRCA2N	09	MRCA3N
08	MRCA6N	08	0V
07		07	
06		06	
05		05	0V
04	FPCZ	04	0V
03	FPSIGN	03	0V
02	COMPT3	02	0V
5A01		5B01	0V
4A25	0V	4B25	SPA00
24	SPA01	24	SPA02
23	SPA03	23	SPA04
22	SPA05	22	SPA06
21	SPA07	21	0V
20	SPA08	20	SPA09
19	SPA10	19	SPA11
18	SPA12		SPA13
17	SPA14	17	SPA15
16	0V	16	KREG00
15	KREG01	15	KREG02
14	KREG03	14	KREG04
13	KREG10	13	0V
12	KREG11	12	KREG12
11	KREG13	11	KREG14
10	KREG15	10	0V
09	PFK	09	0V
08	OR1N	08	0V
07	OR2N	07	0V
06	15R2N	06	0V
05	PFT	05	0V
04		04	
03		03	
02		02	0V
4A01		4B01	0V

Table 9.4b INTERCONNECTION CARDS A AND B

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
3A25	0V	3B25	DS00
24	DS01	24	DS02
23	DS03	23	DS04
22	DS05	22	DS06
21	DS07	21	0V
20	DS08	20	DS09
19	DS10	19	DS11
18	DS12	18	DS13
17	DS14	17	DS15
16	0V	16	DDAT00
15	DDAT01	15	DDAT02
14	DDAT03	14	DDAT04
13	DDAT05	13	DDAT06
12	DDAT07	12	0V
11	DDAT08	11	DDAT09
10	DDAT10	10	DDAT11
09	DDAT12	09	DDAT13
08	DDAT14	08	DDAT15
07	0V	07	
06		06	
05		05	0V
04	EDAT3N	04	0V
03	IMAD15	03	0V
02	SOPR	02	0V
3A01	SOPL	3B01	0V

Table 9.4c INTERCONNECTION CARDS B AND G

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
5A25	0V	5B25	ADAB00
24	ADAB01	24	ADAB02
23	ADAB03	23	0V
22	ADAB04	22	ADAB05
21	ADAB06	21	ADAB07
20	0V	20	ADAB08
19	ADAB09	19	ADAB10
18	ADAB11	18	0V
17	ADAB12	17	ADAB13
16	ADAB14	16	ADAB15
15	0V	15	BU00N
14	BU01N	14	BU02N
13	BU03N	13	0V
12	BU04N	12	BU05N
11	BU06N	11	BU07N
10	0V	10	BU08N
09	BU09N	09	BU10N
08	BU11N	08	0V
07	BU12N	07	BU13N
06	BU14N	06	BU15N
05	0V	05	0V
04	WECN	04	0V
03	WEDN	03	0V
02	LSMMU1	02	0V
3A01	EPMMU1	3B01	0V
4A25		4B25	IMAD00
24	IMAD01	24	IMAD02
23	IMAD03	23	0V
22	IMAD04	22	IMAD05
21	IMAD06	21	IMAD07
20	0V	20	IMAD08
19	IMAD09	19	IMAD10
18	IMAD11	18	IMAD12
17	IMAD13	17	IMAD14
16	0V	16	0V
15	IMADE0	15	IMADE1
14	IMADE2	14	IMADE3
13	IMADE4	13	IMADE5
12	IMADE6	12	IMADE7
11	0V	11	0V
10	COMPC	10	COMPD
09	INVCN	09	INVDN
08		08	WDMA
07	INHCPU	07	INVALN
06	IDMAN	06	0V
05	CSRAMN	05	0V
04	INVDMA	04	0V
03	WCINVN	03	0V
02	EDRVCN	02	0V
4A01	EDRVDN	4B01	0V

Table 9.4d INTERCONNECTION CARDS G AND F

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
6A10	Dummy	6B10	TSTOKN
09	RAZTN	09	FTIMN
08	ENCACN	08	RUNN
07	Dummy	07	
06	+5VL	06	0V
05	0V	05	LOCK
04	RTCE	04	0V
03	0V	03	
02	OPS3N	02	OPS2N
6B01	OPS1N	6B01	OPSON

OPS0-3N U-links must be in position "1" for connection of LIMITED PANEL TO THESE INPUTS

Table 9.5a LIMITED OPERATOR PANEL INTERFACE

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
5A13	Dummy	5B13	
12		12	
11		11	
10		10	
09		09	CT125
08	CT109	08	CT108/2
07	0V	07	CT108/1
06	CT107	06	0V
05	CT106	05	TELEN
04	CT105	04	0V
03	CT104	03	
02	CT103	02	
5A01	0V	5B01	

Note: All signals are V28 except: TELEN is TTL level.

Table 9.5b CONTROL PANEL INTERFACE (EXTENDED)

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
4A05	Dummy	4B05	+12V
04	-12V	04	+ 5V
03	RESETN	03	0V
02	RTCE	02	CT103 *
4A01	SDPM	4B01	LOCK

SDPM and CT103 are V28.
Other signals are TTL levels.

* CT103 = SDMP

Tabel 9.5c CONTROL PANEL (FRCP, HHP) INTERFACE

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
3A13	0V	3B13	NADT00
12	NADT01	12	NADT02
11	NADT03	11	0V
10	NADT04	10	NADT05
09	NADT06	09	NADT07
08	0V	08	NADT08
07	NADT09	07	NADT10
06	NADT11	06	0V
05	0V	05	CPTST
04	CLK5OT	04	0V
03	0V	03	OSTST
02	+5V	02	0V
3A01	+5V	3B01	

Table 9.6 TEST-TOOL INTERFACE

9.3.2 INTERCONNECTIONS

The following system interconnections have to be made:

- Interrupt Lines (IR04-31)
- OKO/OKI from CIP-F to the other masters in the order of their priority
- BRK/BRKZO connections with SCUZ Card (pins: 1C04/1A04).
- Remote IPL (RIPLN) to be connected with a special CU or Device
- Floating Point connections when Floating Point Processor is present at card locations 6 and 7. Floating point interface of CP2B at card CIP-F on connector 2, row C.

Next figure shows the backpanel pinning for all system interconnections.

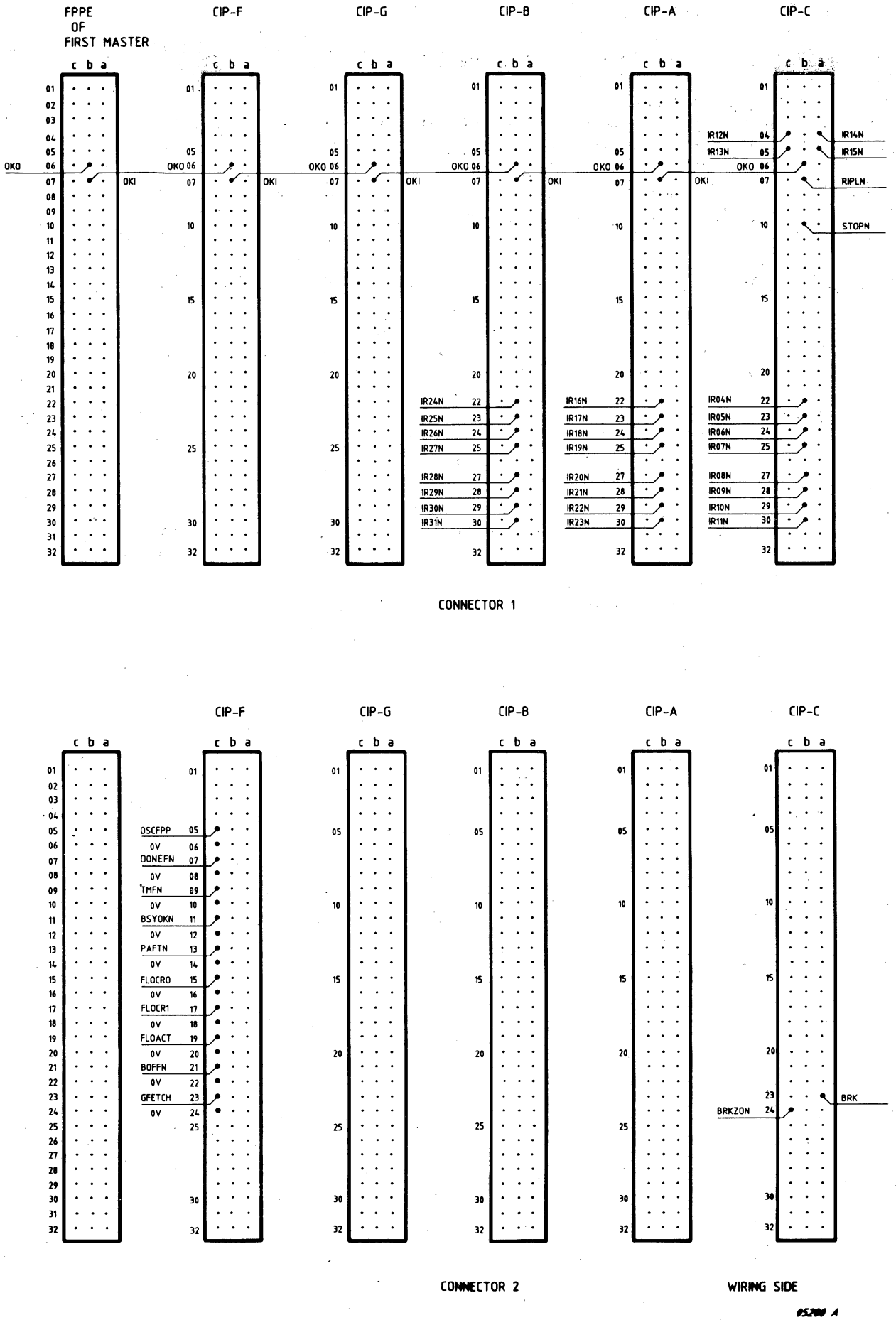


Figure 9.10 INTERCONNECTIONS ON BACKPANEL

9.4 FUNCTIONAL BLOCKDIAGRAM CP2B

Figure 9.11 shows the functional blockdiagram of the CP2B. Connections to other system-elements are via the UPL-Bus.

The ALU and Scratchpad (SPA) registers A1-A14 are for general purpose use.
A15 is the dedicated stackpointer.
A0 is the program counter, located in the PC-circuit.
The PC-circuit also contains operand address- and preset-shadow registers.

The Microprogram is in a 96-bit, 4K ROM and controls the hardware of the CIP.
Instructions are decoded by PLAD, PLAEX, PLAC and a PAL circuit.
An IPL-ROM contains a bootstrap program for the Initial Program Load.
The bootstrap depends on the application:

- P800 systems - (P)ROM 4063 (CIP A, location M0) *
- PTS6900 systems - (P)ROM 5514 (CIP A, location M0) *

A Cache Memory is integrated in the CP2B to decrease the number of data-input cycles on the UPL-Bus. This improves the CIP performance strongly.

* Note: Remove Bootstrap Prom from the PCB-CIPA before sending the card for repair. because the Bootstrap Prom is normally not present on spare CPU cards.

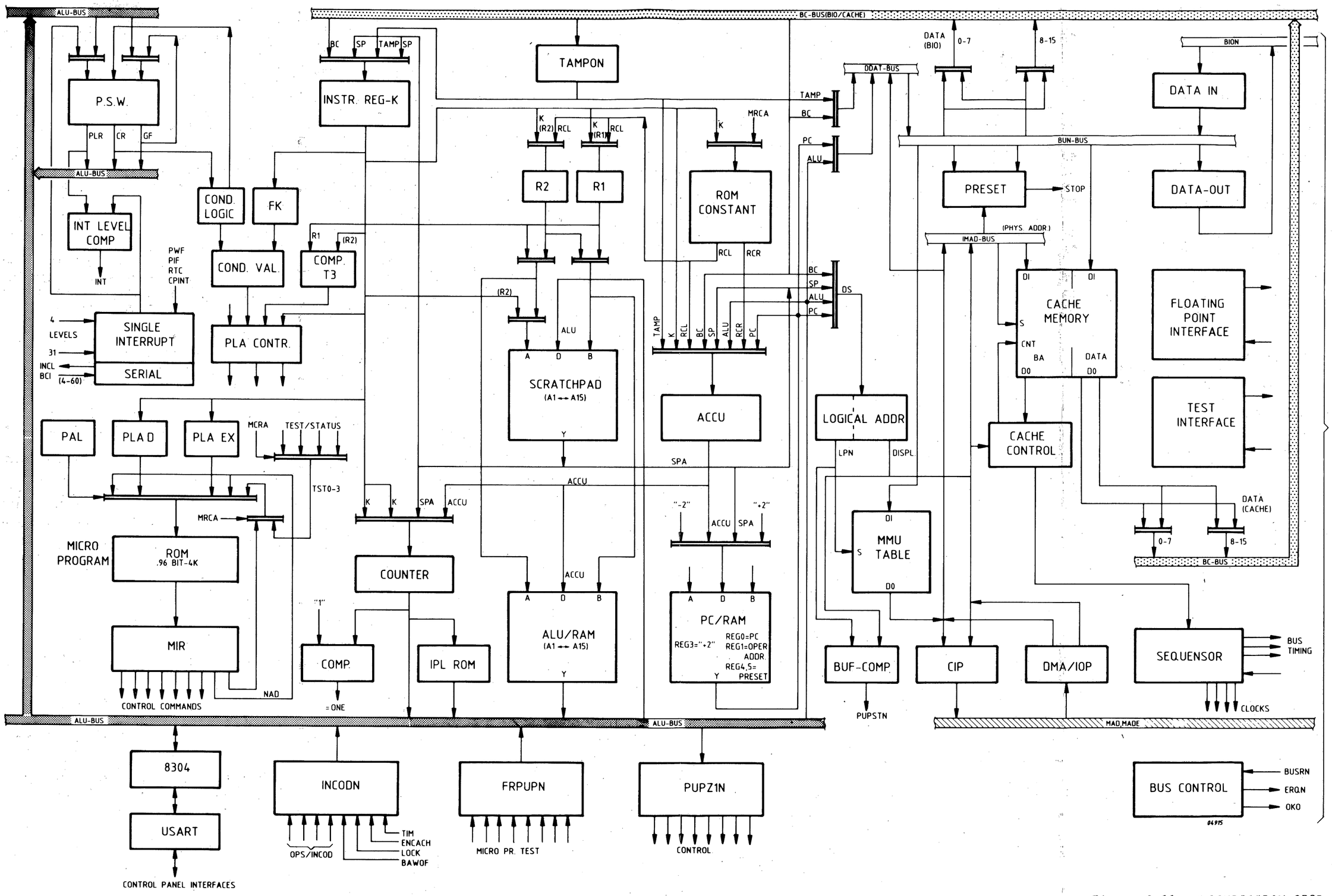


Figure 9.11 BLOCKDIAGRAM CP2B

9.5 CACHE MEMORY (P876)

A so called Cache Memory is integrated in the CP2B to decrease the number of Main Memory accesses which improves the performance.
The use of the Cache Memory is fully transparent for the software.

9.5.1 CACHE MEMORY PRINCIPLE

The 4K-word Cache Memory has an access time which is so short that it can work synchronous with the microprogram of the CIP.
The Cache Memory will copy all words read by the CIP from the Main Memory and remembers also the corresponding memory addresses.
When the CIP wants to read the content of a certain memory address, the Cache Memory will examine the memory address and detect if the content is already present ("HIT") in the Cache Memory or not present ("MISS").
When the Cache Memory detects a "HIT", the CIP will not access the Main Memory but copies the equivalent data already available from the Cache Memory.
When a "MISS" is detected, the CIP must read the data from the Main Memory (longer access time) and the Cache Memory will copy the data and address.

The HIT/MISS ratio strongly influences the performance of the CIP and depends on the software which is used.

The usefull contents of the Cache Memory must always be identical to the corresponding contents of the Main Memory.
In case of Write Memory from the CIP, the Cache Memory is only updated if the address concerned (with the old data) is already present in the Cache Memory ("HIT" detected).
With Write Memory in character mode the Cache Memory cannot copy the data-byte in the correct way and will be invalidated at the corresponding address.
Invalidation of Cache Memory address also happens when a time-out on the UPL-Bus is detected during a memory access, or when the CIP detects a Write Memory access from a DMA or IOP to a memory address also present in the Cache Memory or when the CIP works with FLoating Point Processor.
The time between two Write Memory cycles from DMA or IOP must be more than 350nSec.

9.5.2. CACHE MEMORY ORGANISATION

The physical memory address from the Memory Address Register is devided into the following 3 parts:

MAD15 - 1 bit to select the left- or right hand byte of a data word

MAD05-14 - 10 bits Index field to select 1 address in each of the 4 Cache Memory sets A, B, C and D.

MADE0-7, MAD00-04 - 13 bits Block Address to be stored in the "BA-Cache Memory" or compared with the previously stored value "BA" in the Cache Memory.

The Cache Memory contains at each address the following information:

- Block Address - 13 bits which represent the most significant part of a physical memory address (BA)

- Invalid Bits - 2 bits to indicate that the contents of the Cache Memory address is not valid (after Write Memory in character mode or Bus time-out etc.).
  One of the bits is in a separate 16K 1-bit memory.

- Data Word - 16 bits data which (if not invalidated) must be equal to the data at the Main Memory address formed by the fields Block Address and Index.

To improve the efficiency, the Cache Memory is devided into 4 sets A, B, C and D of 1K words each.
In this way at each indexed address of the Cache Memory 4 different Block Addresses with the corresponding Data can be stored.

When the CIP wants to access a memory address, the Block Address from the Memory Address Register is compared with the 4 Block Addresses from the indexed Cache Memory addresses in the 4 sets A, B, C and D.
When in 1 of the 4 sets a Block Address is found which is equal to that from the Memory Address Register, the data at the indexed address of that set must be equal to the data at the physical Main Memory address ("HIT" detected by 1 of the 4 Cache Memory sets).
When none of the 4 Block Addresses from the sets are equal to that from the Memory Address Register, the data at the indexed Cache Memory address is not representing the contents of the physical Main Memory address ("MISS" detected by all 4 sets of Cache Memory).

In total 4 possibilities can be considered with memory access by CIP:

- Memory Write, "MISS" - No action in Cache Memory.

- Memory Write, "HIT" - The Cache Memory copies the Write-Data word from the Bus and stores it at the indexed address of the set that detected the "HIT".
  In case of character mode on the Bus the Cache Memory address is invalidated because only words can be stored.

- Memory Read, "MISS" - The Cache Memory stores the data read from Main Memory, together with the corresponding Block Address, at the indexed address of only 1 of the 4 sets.
  In this case the set is selected by a 4 position counter which will select the next set after each completed Memory Read cycle on the Bus.

- Memory Read, "HIT" - The Cache Memory supplies the Read-Data to the CIP and Main Memory access via the Bus is not necessary and therefore canceled.

9.5.3 DMA/IOP WRITE MEMORY

When a DMA or an IOP writes new data to a Main Memory address, it will be necessary to invalidate the corresponding Cache Memory address when present.
For this purpose 4 separate sets of 1K bit memory are used to store flag bits.
During each micro-instruction the CIP scans for DMA/IOP Write Memory accesses on the Bus and if necessary the physical address is offered to the Cache Memory.
When the Cache Memory detects a "HIT" in one of its 4 sets the corresponding flag bit on the indexed address will be set.
In this way all Cache Memory addresses, containing data that has been overwritten in the corresponding Main Memory addresses, will be invalidated.

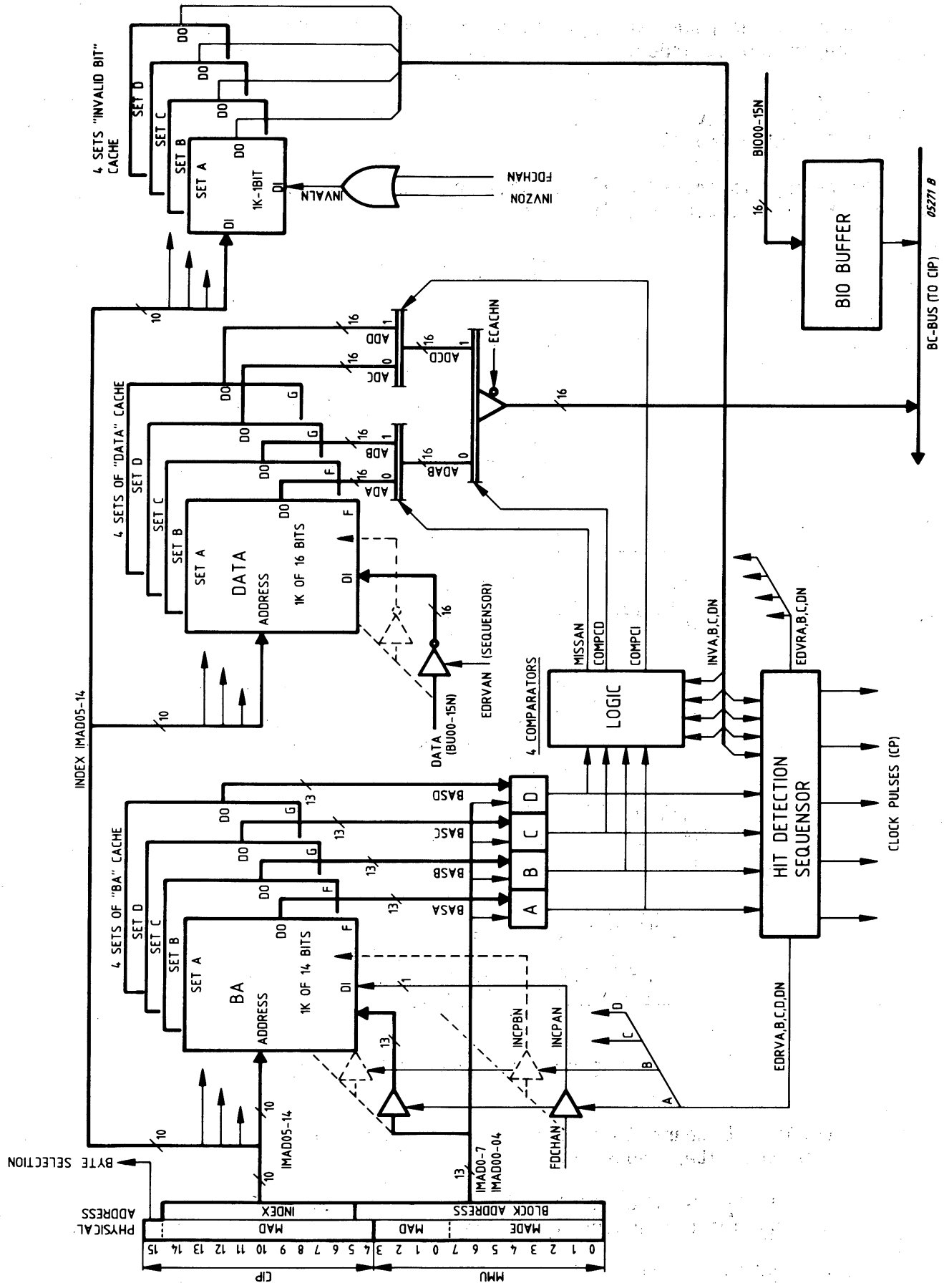


Figure 9.12 CACHE MEMORY BLOCKDIAGRAM

9.6 POWER-ON SEQUENCE

With Power-On the power supply must start the standard sequence of actions which is in the following order:

- DC voltages on
- RSLN off (high level)
- PWFN off (high level)

The following flowchart indicates what happens depending on the signals LOCK and BAWOFN when the power is switched on.

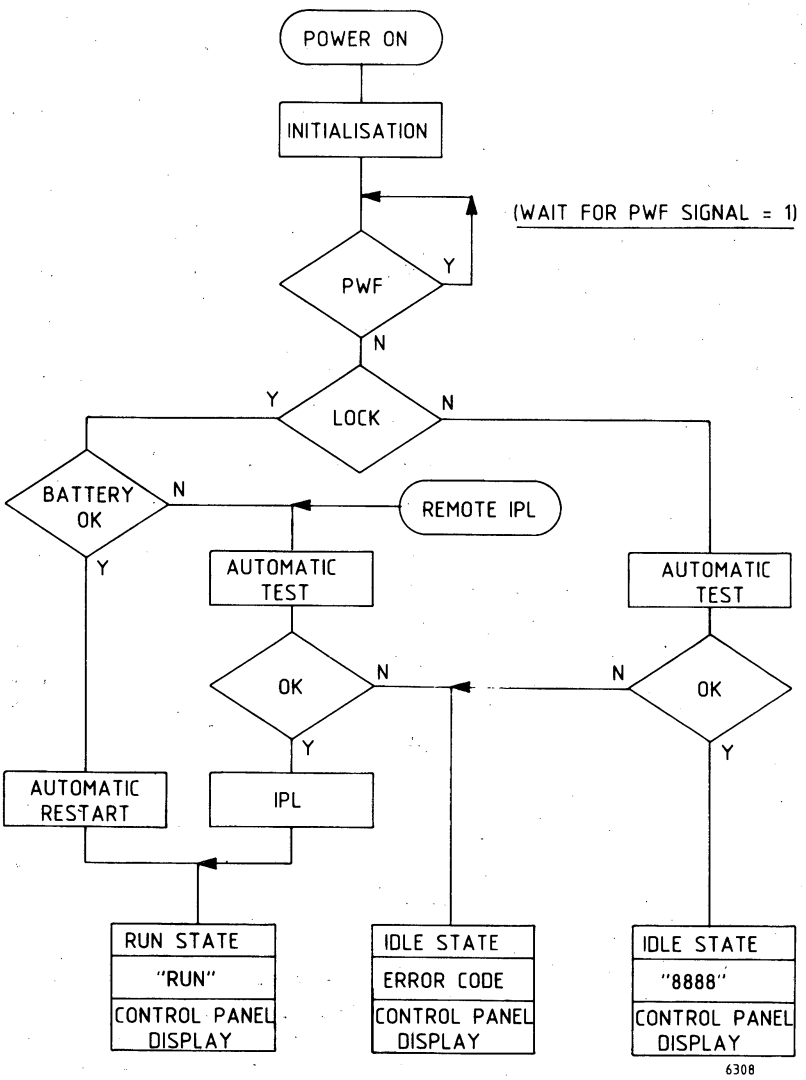


Figure 9.13 POWER-ON SEQUENCE

Notes: BAWOFN = 1 means that the battery was normally supplying the memories since the latest power-off.

LOCK can be switched to "0" from either the HHP/FRCP or from an operator panel with a corresponding switch. Without a panel, LOCK = "1".

Check of "Automatic-IPL":
When LOCK is 1 and the battery was disconnected to force BAWOFN = 0, an Automatic-IPL is done instead of Automatic Restart, which normally is done.

9.6 AUTOMATIC TEST

The AUTOMATIC TEST is always done after Power-On and before Remote or Auto IPL. The major part of the CIP and the CACHE control logic and memory are tested. The result depends on the state of the LOCK signal and the serial panel being connected or not and will be according to the table below:

LOCK	SERIAL PANEL CONNECTED	RESULT OF TEST	SERIAL PANEL DISPLAY	INTERFACE OF PANEL TSTOK SIGNAL	CPU ACTIVITY
1	NO	OK	--	1	RUN
		NOT OK	--	0	IDLE
	YES	OK	"RUN"	1	RUN
		NOT OK	Error Code	0	IDLE
0	YES	OK	/8888	1	IDLE
		NOT OK	Error Code	0	IDLE

Table 9.7 AUTOMATIC TEST

The Automatic Test is of the GO/NO-GO type. If an error is detected, the CIP will come in the IDLE state. In that case the Error Code is displayed.

In general it has no use to do further tests when the automatic test fails (TSTOK=0), except microdiagnostic from panel.

If no error was detected it can be usefull to use the Microdiagnostic test as described in the next section.

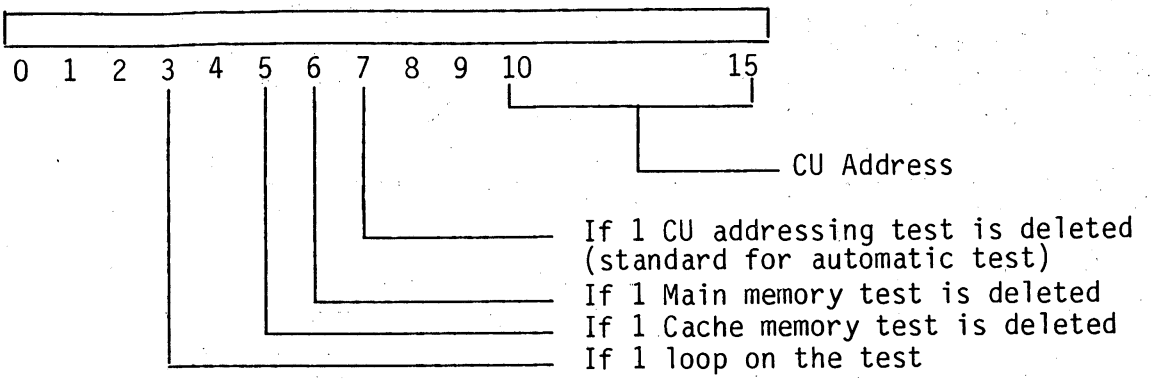
9.6.2 MICRODIAGNOSTIC TEST

The Microdiagnostic will test the complete CP2B, the memory and a specified Control Unit. To start Microdiagnostic a Serial Panel must be connected and simultaneously the buttons "0" and "TEST" on the panel must be pressed.
Microdiagnostic is also started before Automatic-IPL or Remote-IPL, but without the Control-Unit Test. It is then called "Automatic Test".
A letter "d" is displayed on the control panel as long as the test is running.
The Microdiagnostic can be split up into the following parts:

- CIP test
- Cache Memory test
- Main Memory test
- Control Unit addressing test

Before starting the Microdiagnostic tests, parameters can be entered in the Data part of the Serial Panel to delete some tests, to loop on test and to select a Control Unit address.

The Data Register of the serial control panel must be loaded as follows:



The complete main memory is tested (if consecutive).

Tests are executed in the order as indicated in the flowchart.

At the end of the microdiagnostic test a code is displayed on the serial panel, giving either the correct end of test or an error.

When loop on the test (bit 3) has been specified, the testing stops only in case of errors or after any Control-Panel Function.

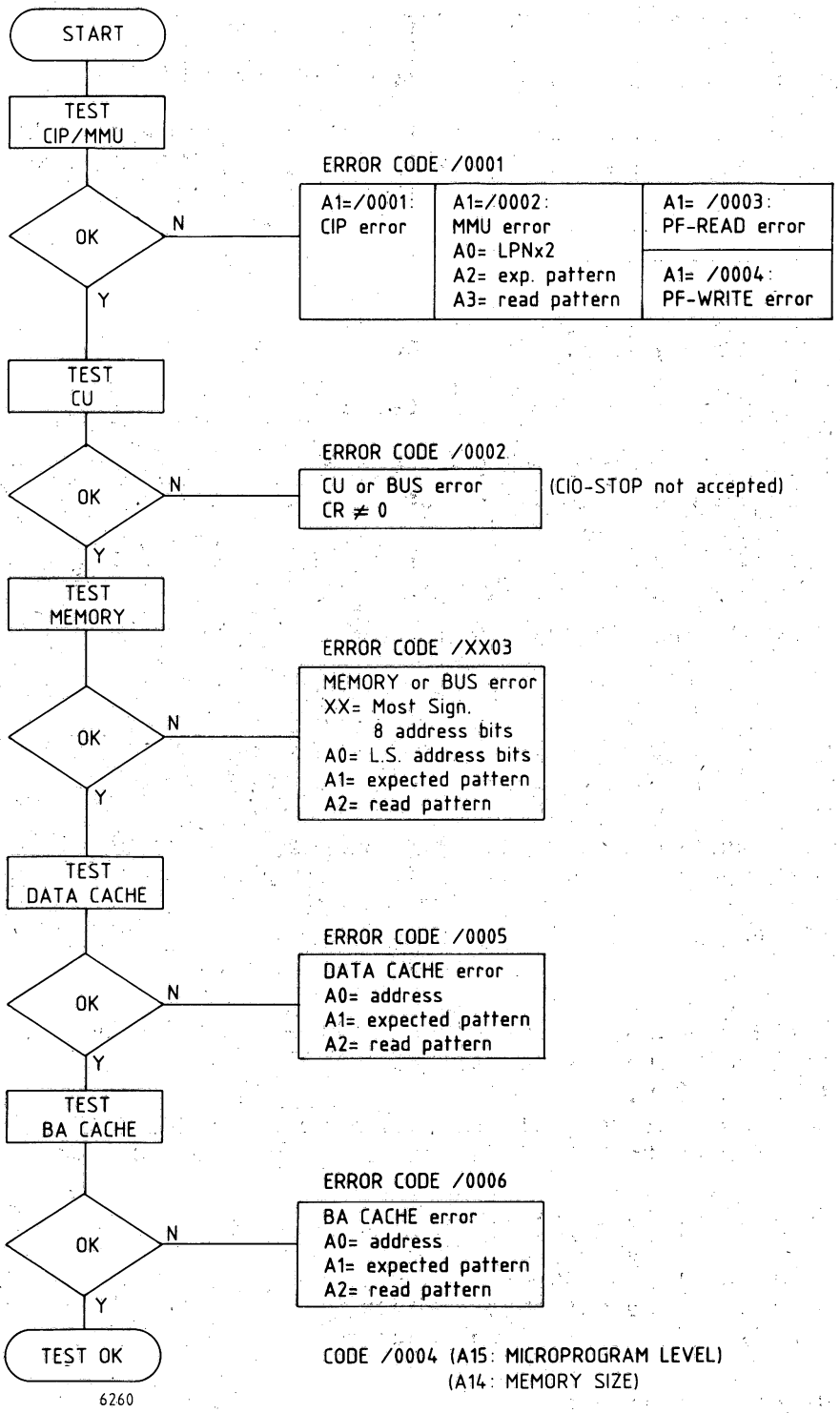


Figure 9.14 MICRODIAGNOSTIC TESTS

9.7 SHORT DESCRIPTION OF TESTPROGRAMS

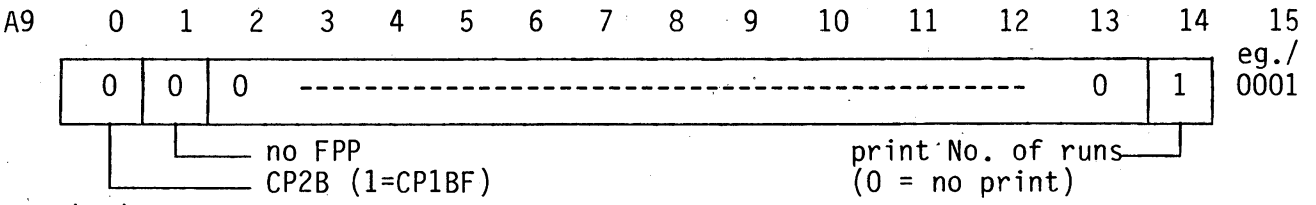
TESTPROGRAM CP1/2B

Memory size 32kb minimum

Power fail/auto restart and Real Time Clock allowed.

Program to test the instruction set of CP1BF and CP2B Central Instruction Processors.

Procedure:
- IPL
- Change CPU register contents:



- start

For this program, the No. of runs is printed on the Console, dev.addr./10:

```
run CPU = 0001
run CPU = 0002
          0003
           etc.
```

If an error (or unexpected interrupt) occurs, the count is stopped, but no information about the error is displayed. It is only a GO/NO GO test.

One complete CPU run lasts 2 - 3 secounds.

Note,
After IPL the program stops at /300. Unexpected interrupt stops at /24A.
The number of CPU runs is counted at /24A.
A TRAP stops at /248.
In case of error the program stops. The instruction causing the stop can be found by searching the stop address in the program listing.

Tested: all CPU instructions, except:
- ABK in T8 format
- LKM, ENB, INH and RIT
- all input/output instructions

The test program is split up in 3 main parts:

1. Instruction set of P854/8/9
2. Test of the trapped instruction
3. "D"-type instruction Set.

The program is designed to start from very simple instructions which are then used to check the other instructions.

Procedure: 5111 991 13061
Listing : 5111 991 13071
Program : 5111 199 56991

10 MEMORY MODULES

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10.1 P843-608 WMD MEMORY (HIGH SPEED VERSION)

10.1.1 IDENTIFICATIONS

- Type No. : P843-608 (WMD)
- Testprograms : BRAM (4KW-32KW)
  BBRAM (32KW-512KW)

- Power Consumption:

	Max. Average Current		
	Operating	Stand-By	Stand-By Battery
+5VL +5VM	1.5A 1.14A [1]	1.5A 0.62A	-- 0.62

[1] Based on Memory Request Rate of 660 nsec.

Table 10.1.1 POWER CONSUMPTION P843-608 (WMD)

- 12NC code on the sticker on the board:
  P843-608: 5122 194 4199x (WMD) (5322 216 21236)
x = modification level

- Performance Data

The capacity of one WMD-H/S semiconductor memory (SCM) is 256K bytes (128K words). One word consists of 16 bits plus 5 bits for internal error correction of one faulty bit.
The X-tal frequency of High Speed Version is 27 Mc. Access time = 340 nS.

CYCLE	ACN ACCESS TIME	TSMN ACCESS TIME	MEM	BUS CYCLE
	TYP	TYP	CYCLE	TYP
READ No Error Detected	190nS	340nS	362nS	395nS
READ Error Corrected	190nS	412nS	362nS	430nS
WRITE Word	190nS	190nS	362nS	340nS
WRITE Character	190nS	190nS	724nS	700nS

Table 10.1.2 ACCESS AND CYCLE TIMES P843-608 (WMD)

WARNING
TAKE CARE OF MOS - HANDLING PROCEDURE!

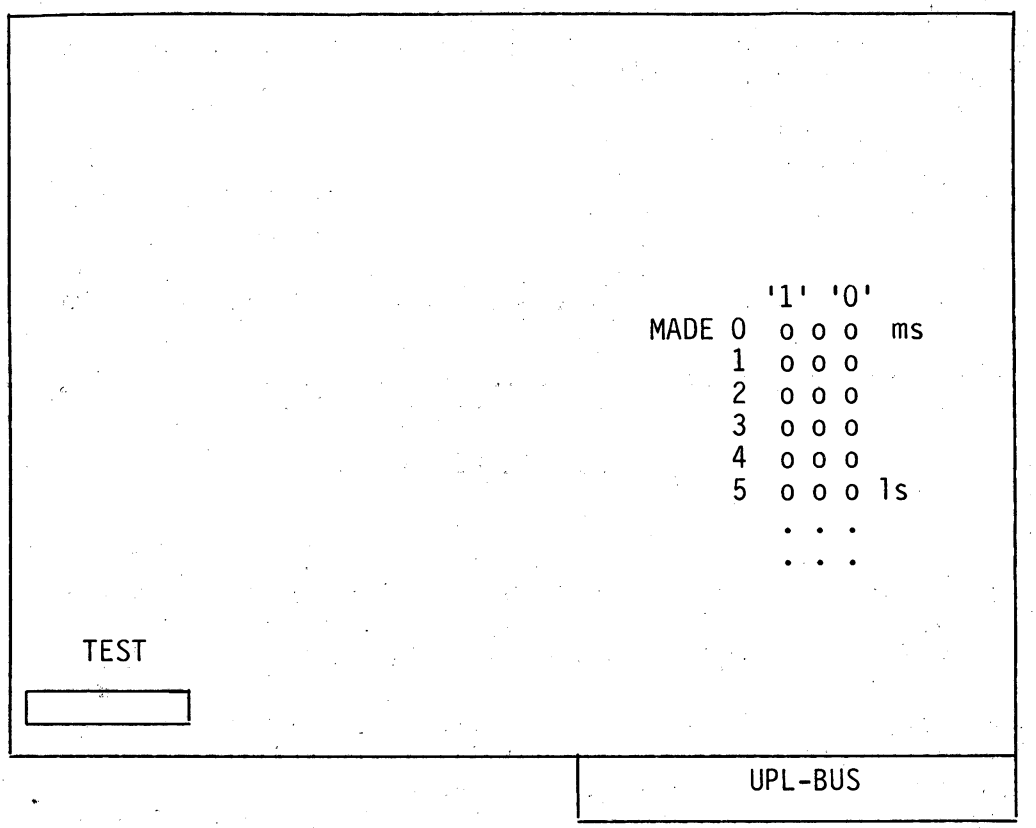


Figure 10.1.1 U-LINK SETTING P843-608 (WMD)

Module No.	Memory Range	MADE 0 1 2 3 4 5	Address Range
0	0 - 128K16	0 0 0 0 0 0	/000000 - /03FFFE
1	128 - 256	0 0 0 0 0 1	/040000 - /07FFFE
2	256 - 384	0 0 0 0 1 0	/080000 - /0BFFFE
3	384 - 512	0 0 0 0 1 1	/0C0000 - /0FFFFE
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
63	8M16	1 1 1 1 1 1	/FC0000 - /FFFFFE

Table 10.1.3 U-LINK SETTING P843-608 (WMD)

10.1.3 BLOCKING ERROR-RECOVERY

For repair in the workshop error recovery can be blocked.
Also in case of repeated memory faults at the customer, running the testprogram without error recovery may be useful.

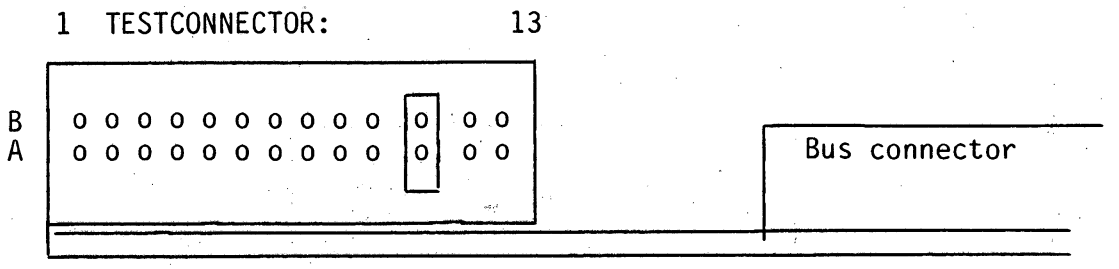


Figure 10.1.2. TEST CONNECTOR P843-608 (WMD)

Interconnection of TBLECN and 0V (pin B11 to A11) blocks error detection and correction. This link can be made with a U-link and can be applied when running the testprogram. DO NOT FORGET TO REMOVE THIS LINK AFTER SERVICE!

Note: For normal service this is not allowed, as error recovery is to obtain a better MTBF and thus receiving less cards for repair.
A card may be sent up for repair if two errors are on a PCB or the card is suspected to give problems to the customer (= sometimes two errors or timing problems).

10.2 P844-016 CMOS MEMORY (CM8)

10.2.1 IDENTIFICATIONS

- Type number : P844-016 (8K16)

- Testprogram : BRAM (from 4KW-32KW)

- Power consumption:

+5VL	1.25A (typ)
+5VM	0.03A (typ)
+12VM	1mA (max)

Table 10.2.1 POWER CONSUMPTION P844-016

-12NC code on the sticker on the board:

P844-016: 5111 199 6788x (5322 216 21227)

X = modification level

- Performance Data

The minimum cycle time of the Memory is = less than 750nS.
For UPL Mode the access time is 580nS (typ), 640nS (max).

- Facilities

The CM8 (CMOS Memory 8K) is a 16-bit RAM Memory Module intended to be used as the main memory for GPBS (P851) or UPL Bus (P854) System. The principle facilities available with this card are as follows:

- Two operating cycles, read and write.
  Word or character mode for both read and write cycles.
- The card may be depopulated so that the user has a memory module of either 2K, 4K or 8K words.
- Data retention to enable a memory card to be transferred from one computer to another. This facility is enabled with the SAVE Switch.
- Rechargeable battery mounted on the card.
- Memory protection in the event of a power failure.

WARNING
Take care of MOS HANDLING PROCEDURE

10.2.2 INSTALLATION DETAILS

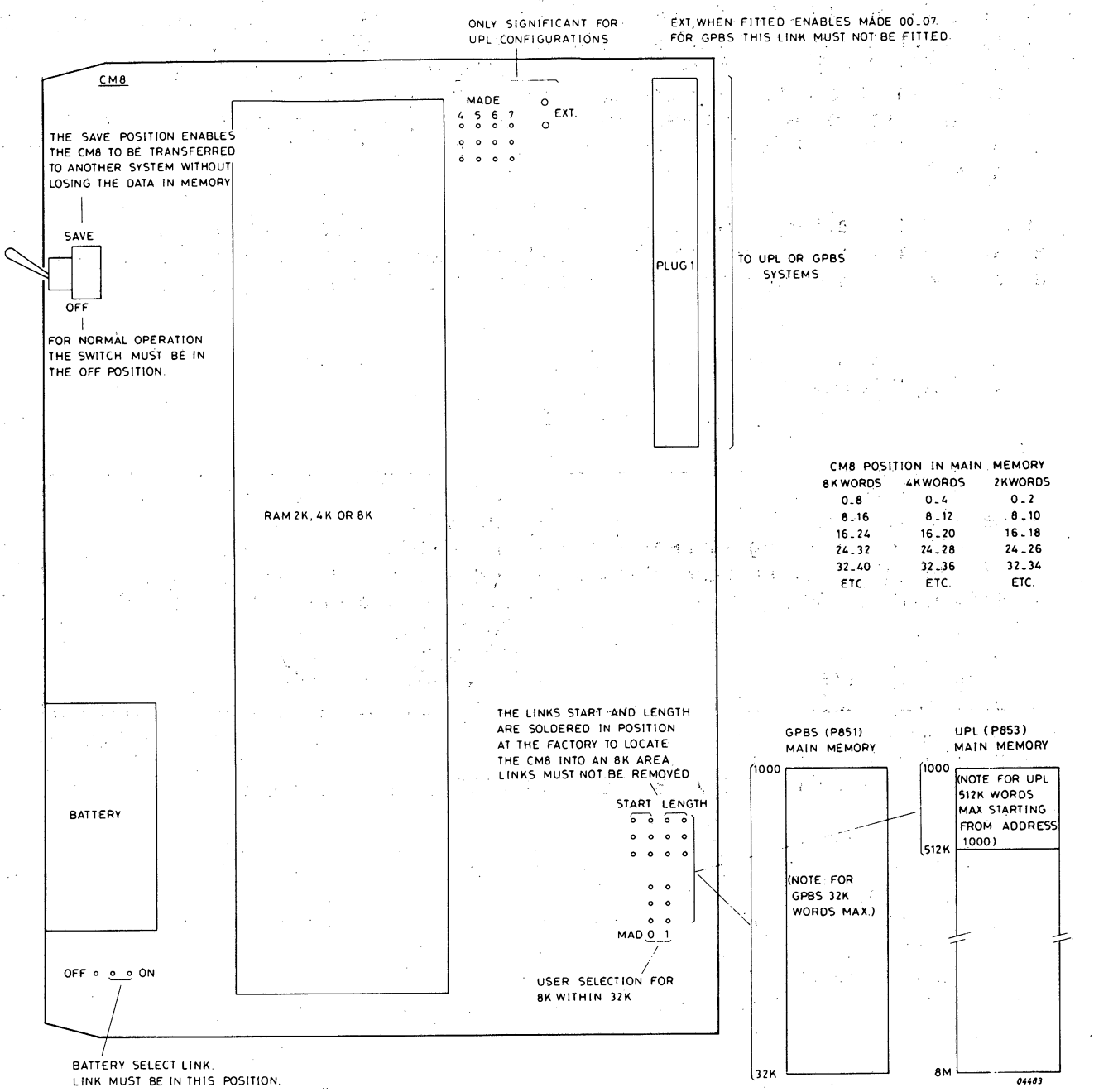


Figure 10.2.1 U-LINK SETTING P844-016

U-LINK SETTINGS

The location of the U-links is shown in Figure 10.2 and their function is as follows:

- BAT - There are 2 positions for this link: ON connects the Battery to the Memory and OFF disconnects the Battery.
- MAD 00, 01 and MADE4, E5, E6, E7 - These links are used to position the CM8 in the System Memory. (MADE not significant for GPBS or P853).
- START, LENGTH - These links are not selectable by the user; they are soldered in position at the factory and must not be removed.
- EXT - When fitted enables MADE 0-7 to be taken into account by the CM8 logic; when not fitted MADE 0-7 are inhibited (only fitted for UPL configurations with MMU).

A two position battery switch enables the user to select either SAVE or OFF. In the SAVE position the card may be transferred to another system without loosing the data. For normal operation the Switch must be in the OFF position.

BATTERY CHARACTERISTICS

Nominal voltage	- 2.4V
Capacity	- 100 mA/H
Permanent charging current (max)	- 3mA at 0°C
Permanent charging current (max)	- 5mA between 10 to 50°C
Retention Time	- After a complete charge at +20°C: 2KW memory: 17 days 8KW memory: 5 days
Charging time	- Less than 48 hours

Table 10.2.2 BATTERY CHARACTERISTICS P844-016

10.3 P851-010 PROM/EPROM MEMORY (PR016)

10.3.1 IDENTIFICATIONS

- Type number: P851-012
- Power consumption:

	Module	Voltage	Power Consumption Standby	Operating TYPICAL	tolerance
	ØK	+5V	700mA	700mA	+5%
EPROM 2716	8KB	"	760mA	860mA	"
	16KB	"	820mA	920mA	"
	24KB	"	880mA	980mA	"
	32KB	"	940mA	1 040mA	"
PROM 82S191	8KB	"	1 220mA	1 220mA	+5%
	16KB	"	1 740mA	1 740mA	"
	24KB	"	2 260mA	2 260mA	"
	32KB	"	2 780mA	2 780mA	"

Table 10.3.1 POWER CONSUMPTION P851-010

An extra +25V generated on the program tool is needed during programming mode. EPROM and PROM devices can not be mixed on the same module, because of pin incompatibility.

- 12NC code on the sticker on the board:
  P851-010: 5111 199 6814x
X = modification level (board without PROM's)

- Performance Data

The capacity of the module is 16K words. The capacity can be reduced to 12-8-4k words.

The module can be used in a 32k word system (P851 system), or in a 8M word system (UPL).
In the latter case the preselection done by U-links is limited to the first 1M byte area of the memory.

Cycle time:

		Tcycle (typ) in ns.	Tcycle (Max) in ns.
P 851 Mode	EPROM (2716)	760 ns.	910 ns.
	PROM 82S191	360 ns.	510 ns.
UPL Mode	EPROM (2716)	810 ns.	970 ns.
	PROM 82S191	410 ns.	570 ns.

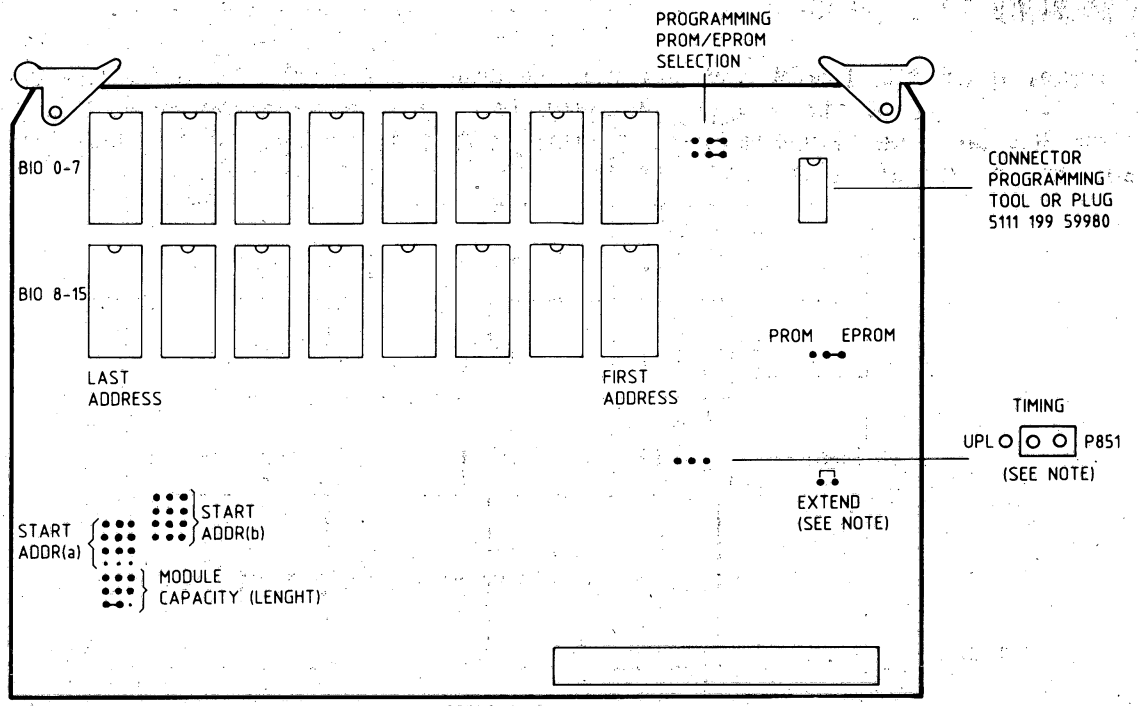
Table 10.3.2 CYCLE TIME P851-010

Access time:

		Tacc (typ) in ns.	Tacc (Max) in ns.
P 851 Mode	EPROM (2716)	650 ns.	765 ns.
	PROM 82S191	250 ns.	365 ns.
UPL Mode	EPROM (2716)	710 ns.	825 ns.
	PROM 82S191	310 ns.	425 ns.

Table 10.3.3 ACCESS TIME P851-010

10.3.2 INSTALLATION DETAILS



NOTE: THE TIMING U-LINK MUST BE ACCORDING TO THE CORRESPONDING U-LINK ON CP1BF OR CP2B.

START ADDRESS (a)
O O O MSB
O O O
O O O LSB
'0' '1'

START ADDRESS (a)	
MSB — LSB	MEM. ADDR.
0 0 0	/0000
0 0 1	/1000
0 1 0	/2000
0 1 1	/3000
1 0 0	/4000
1 0 1	/8000
1 1 0	/A000
1 1 1	/C000

START ADDRESS (b)
O O O MADE 7
O O O MADE 6
O O O MADE 5
O O O MADE 4
'1' '0'

NOTE: NOT USED ON P851, EXTEND OUT.

START ADDRESS (b)	
MADE4 — MADE7	MEM. ADDR.
0 0 0 0	/00000
0 0 0 1	/10000
0 0 1 0	/20000
0 0 1 1	/30000
0 1 0 0	/40000
0 1 0 1	/50000
0 1 1 0	/60000
0 1 1 1	/70000
1 0 0 0	/80000
1 0 0 1	/90000
1 0 1 0	/A0000
1 0 1 1	/B0000
1 1 0 0	/C0000
1 1 0 1	/D0000
1 1 1 0	/E0000
1 1 1 1	/F0000

MODULE CAPACITY (LENGTH)
O O O MSB
O O O
O—O o LSB
'0' '1'

MODULE CAPACITY (LENGTH)	
MSB — LSB	LENGTH IN K WORDS
0 0 0	4
0 0 1	8
1 1 0	12
1 1 1	16

05824

FIELD SELECTION: START ADDR. (A + B) (FOR P851 B=0 ALWAYS)
START ADDR. A + LENGTH MUST NOT PASS A 32 KW BOUNDARY.

Figure 10.3.1 U-LINK SETTING P851-010

10.3.3 APPLICATION NOTES

PROGRAMMING TOOL (P843-012)

Programming of the EPROM modules can be done on the system with the programming tool. The Slave Control Unit Programming Tool has to be placed between the system BUS and the EPROM module. A small cable is connected for the +25V and the transfer of certain commands.

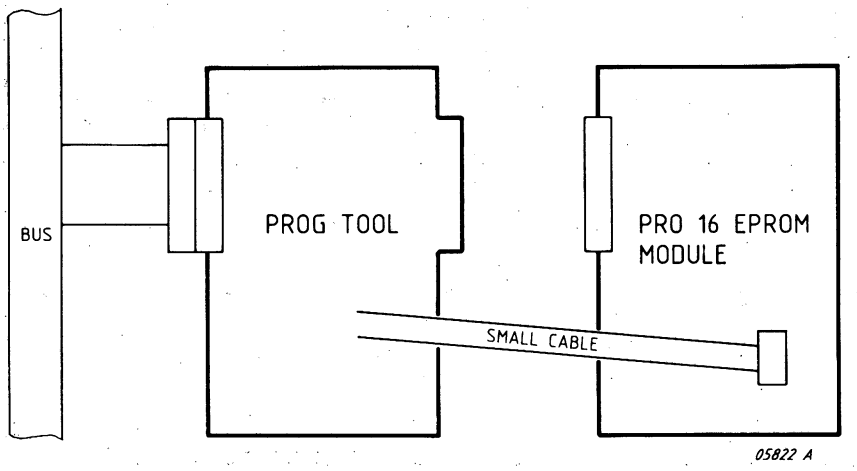


Figure 10.3.2 PROGRAMMING TOOL CONNECTION

Pin number	Signal name	Pin number	Signal name
01	0V	08	0V
02	DEVEN	09	DEVEN
03	IPGMEN	10	IPGMEN
04	OE-N	11	OE-N
05		12	
06	25V	13	25V
07		14	

DEVEN Level "0" Enables the BIO Gates for input from the Bus.

IPGMEN Level "1" Enables selection of the proper pair of EPROM's to program.

OE-N Level "0" Inhibits output of the EPROM during programming.

Table 10.3.4 PROGRAMMING TOOL CONNECTOR (14 PIN SOCKET)

10.4 P851-012 PROM/EPROM MEMORY (PR032)

10.4.1 IDENTIFICATIONS

- Type number: P851-012
- Power consumption:

	Module	Voltage	Power Consumption Standby	Operating TYPICAL	tolerance
	ØK	+5V	700mA	700mA	+5%
EPROM 2732	16KB	"	820mA	1 060mA	"
	32KB	"	940mA	1 080mA	"
	48KB	"	1060mA	1 300mA	"
	64KB	"	1180mA	1 420mA	"
PROM 2732A	16KB	"	840mA	1 070mA	+5%
	32KB	"	980mA	1 210mA	"
	48KB	"	1 120mA	1 350mA	"
	64KB	"	1 260mA	1 490mA	"

Table 10.4.1 POWER CONSUMPTION P851-012

An extra +25V generated on the program tool is needed during programming mode. EPROM and PROM devices can not be mixed on the same module, because of pin incompatibility.

- 12NC code on the sticker on the board:
  P851-012: 5111 199 6009x

X = modification level (board without PROM's)

- Performance Data

The capacity of the module is 32K words. The capacity can be reduced to 28-24-20-16-12-8-4K words.

The module can be used in a 32k word system (P851 system), or in a 8M word system (UPL).
In the latter case the preselection done by U-links is limited to the first 1M byte area of the memory.

Cycle time:

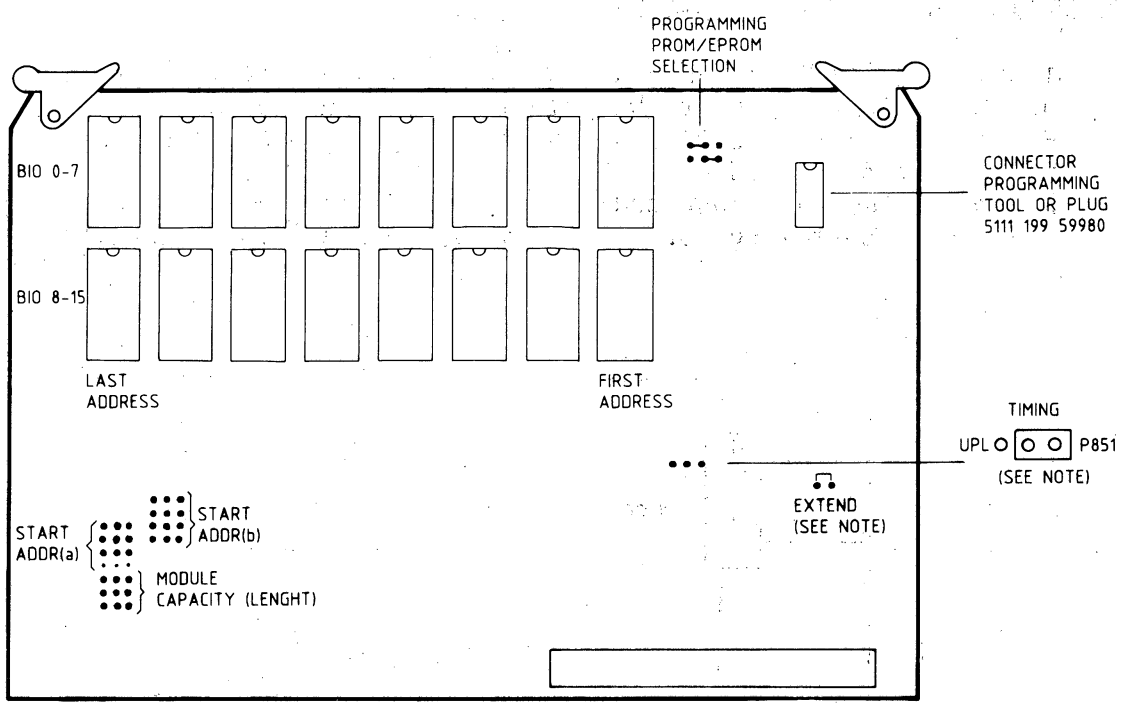
		Tcycle (typ) in ns.	Tcycle (Max) in ns.
P 851 Mode	EPROM (2732)	750 ns.	900 ns.
UPL Mode	EPROM (2732)	810 ns.	960 ns.

Table 10.4.2 CYCLE TIME P851-012

Access time:

		Tacc (typ) in ns.	Tacc (Max) in ns.
P 851 Mode	EPROM (2732)	650 ns.	765 ns.
UPL Mode	EPROM (2732)	710 ns.	825 ns.

Table 10.4.3 ACCESS TIME P851-012



NOTE: THE TIMING U-LINK MUST BE ACCORDING TO THE CORRESPONDING U-LINK ON CP1BF AND CP2B CPU'S.

START ADDRESS (a)	
O O O	MSB
O O O	
O O O	LSB
'0' '1'	

START ADDRESS (a)	
MSB → LSB	MEM. ADDR.
0 0 0	/0000
0 0 1	/1000
0 1 0	/2000
0 1 1	/3000
1 0 0	/4000
1 0 1	/5000
1 1 0	/6000
1 1 1	/7000

START ADDRESS (b)	
O O O	MADE 7
O O O	MADE 6
O O O	MADE 5
O O O	MADE 4
'1' '0'	

NOTE: NOT ON P851 WITH EXTEND OUT. A WIRED PLUG 5111 199 59980 MUST BE PRESENT IN SOCKET AT LOCATION B4.

START ADDRESS (b)	
MADE4 → MADE7	MEM. ADDR.
0 0 0 0	/00000
0 0 0 1	/10000
0 0 1 0	/20000
0 0 1 1	/30000
0 1 0 0	/40000
0 1 0 1	/50000
0 1 1 0	/60000
0 1 1 1	/70000
1 0 0 0	/80000
1 0 0 1	/90000
1 0 1 0	/A0000
1 0 1 1	/B0000
1 1 0 0	/C0000
1 1 0 1	/D0000
1 1 1 0	/E0000
1 1 1 1	/F0000

MODULE CAPACITY (LENGTH)	
O O O	MSB
O O O	
O O O	LSB
'0' '1'	

MODULE CAPACITY (LENGTH)	
MSB → LSB	LENGTH IN K WORDS
0 0 0	4
0 0 1	8
0 1 0	12
0 1 1	16
1 0 0	20
1 0 1	24
1 1 0	28
1 1 1	32

05823

FIELD SELECTION: START ADDR. (A + B) (FOR P851 B=0 ALWAYS)
START ADDR. A + LENGTH MUST NOT PASS A 32 KW BOUNDARY.

Figure 10.4.1 U-LINK SETTING P851-012

10.4.3 APPLICATION NOTES

PROGRAMMING TOOL PRGT 2 (P843-012)

Programming of the EPROM modules can be done on the system with the programming tool. The Slave Control Unit Programming Tool has to be placed between the system BUS and the EPROM module. A small cable is connected for the +25V and the transfer of certain commands.
A special plug must be inserted if the PRO32 is operating normally in the system, without Programming Tool (pin 7 to 8 and pin 1 to 5 connected).

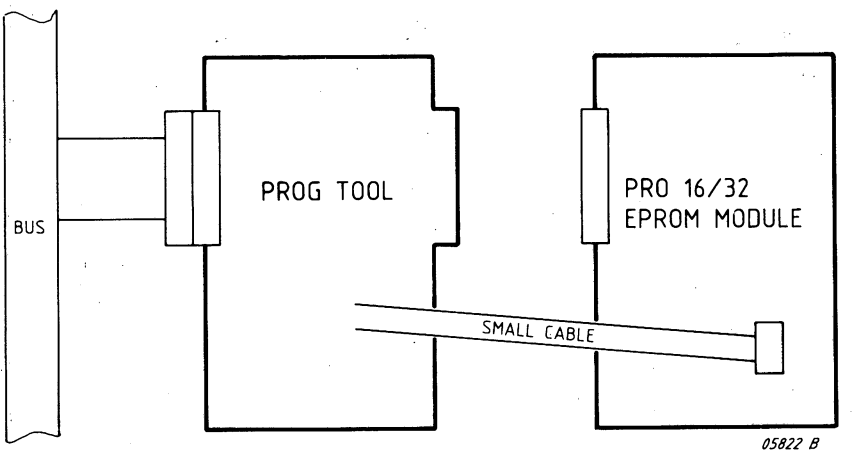


Figure 10.4.2 PROGRAMMING TOOL CONNECTION

Pin number	Signal name	Pin number	Signal name
01	0V	08	0V
02	DEVEN	09	DEVEN
03		10	
04	OE-N	11	OE-N
05	IPGMEN2	12	IPGMEN2
06		13	
07	21VP/25VP	14	21VP/25VP

DEVEN Level "0" Enables the BIO Gates for input from the Bus.

IPGMEN2 Level "1" Enables selection of the proper pair of EPROM's to program.

OE-N Level "0" Inhibits output of the EPROM during programming.

Note: Pin 07/14 is normally 25V (chips 2716 or 2732) but must not be higher than 21V for chips 2732A.

Table 10.4.4 PROGRAMMING TOOL CONNECTOR (14 PIN SOCKET)

10.5 P843-012 PROGRAMMING TOOL (PRGT2)

10.5.1 IDENTIFICATIONS

- Type No. : P843-012 (PRGT2)
- Power Consumption

VOLTAGE	CURRENT	OPERATING TOLERANCE	SAFE VOLTAGE
+ 5VL	2.2A	± 5%	+6V
+ 12VL	0.55A	± 5%	+15V

Note: The +12VL is used to generate the +21V or +25V for programming.

Table 10.5.1 POWER CONSUMPTION P843-012 (PRGT2)

- 12NC code on the sticker on the board:
  P843-012 : 5111 199 59740 (PRGT2)

- Cable : 5111 199 64550 Cable PRGT-PRO16

- Performance Data:
  The programming time for a complete 32K-byte card (PRO16) is about 20 minutes, for 64K-byte (PRO32) about 40 minutes.

10.5.2 INSTALLATION DETAILS

U-LINK SETTING

Before the PRGT2 card is plugged into the rack the U-links must be correctly positioned, as follows:

° The U-links marked MAD10 to 15 must correspond with the chosen CU address.

° The U-link marked 2732A-2716-32 must be positioned to select the correct voltage for the type of Eprom's to be programmed (i.e. +25V for 2716-2732 or +21V for 2732A).

WARNING: - Programming the 2732A packages with +25V will destroy the EPROM's.

INSTALLATION

The PRGT2 card is first plugged into one of the CU slots in the rack. The U-link EXTEND on the PRO-- card must be disconnected, then the PRO-- card is plugged into connector 4 of the PRGT2 card. The special socket and cable should now be installed between the PRGT2 and the PRO-- card.

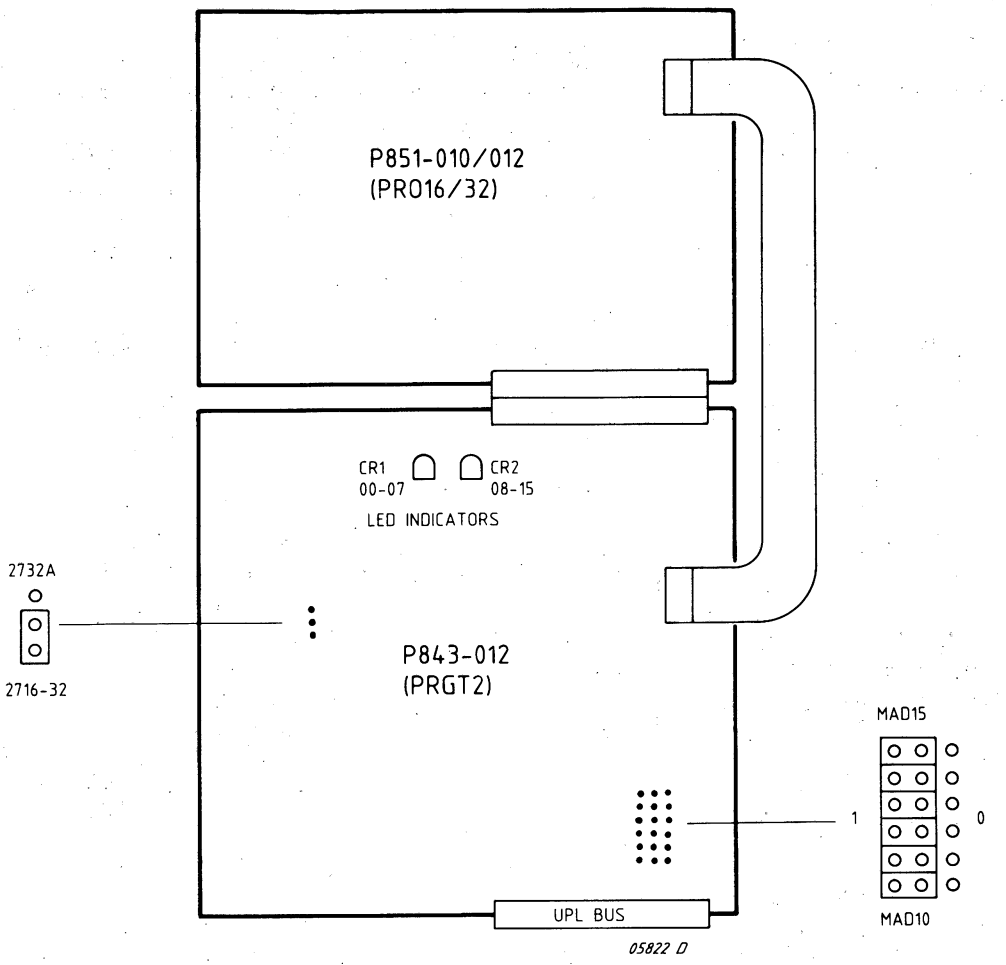


Figure 10.5.1 U-LINK SETTING AND LED INDICATORS P843-012

LED CR1 00 - 07	LED CR2 08 - 15	INDICATES
OFF	OFF	No Error
OFF	ON	Error BION08 to 15
OFF	OFF	Error BION00 to 07
ON	ON	Error BION00 to 15

Note: During an SST command the contents of R3 will be the address of the last word programmed.

Table 10.5.2 LED INDICATIONS P843-012

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01	+12VL *	1A01		4C01		4A01	
1C02		1A02		4C02		4A02	
1C03		1A03		4C03		4A03	
1C04		1A04		4C04		4A04	
1C05		1A05		4C05		4A05	
1C06	0V	1A06	0V	4C06	0V	4A06	0V
1C07	PWFN *	1A07	RSLN	4C07		4A07	RSLN
1C08		1A08		4C08		4A08	
1C09	0V	1A09	0V	4C09	0V	4A09	0V
1C10		1A10	TSMN	4C10		4A10	TSMAN
1C11		1A11	TMRN	4C11		4A11	TMRAN
1C12	0V	1A12	0V	4C12	0V	4A12	0V
1C13	MAD00	1A13	MAD01	4C13	MADA00	4A13	MADA01
1C14	MAD02	1A14	MAD03	4C14	MADA02	4A14	MADA03
1C15	MAD04	1A15	MAD05	4C15	MADA04	4A15	MADA05
1C16	MAD06	1A16	MAD07	4C16	MADA06	4A16	MADA07
1C17	MAD08	1A17	MAD09	4C17	MADA08	4A17	MADA09
1C18	MAD10	1A18	MAD11	4C18	MADA10	4A18	MADA11
1C19	MAD12	1A19	MAD13	4C19	MADA12	4A19	MADA13
1C20	MAD14	1A20	MAD15	4C20	MADA14	4A20	MAFA15
1C21	CHA *	1A21	WRITE	4C21	0V	4A21	WRITEA
1C22	0V	1A22	0V	4C22	0V	4A22	0V
1C23	BI008N	1A23	BI000N	4C23	BIOA08N	4A23	BIOA00N
1C24	BI009N	1A24	BI001N	4C24	BIOA09N	4A24	BIOA01N
1C25	BI010N	1A25	BI002N	4C25	BIOA10N	4A25	BIOA02N
1C26	BI011N	1A26	BI003N	4C26	BIOA11N	4A26	BIOA03N
1C27	BI012N	1A27	BI004N	4C27	BIOA12N	4A27	BIOA04N
1C28	BI013N	1A28	BI005N	4C28	BIOA13N	4A28	BIOA05N
1C29	BI014N	1A29	BI006N	4C29	BIOA14N	4A29	BIOA06N
1C30	BI015N	1A30	BI007N	4C30	BIOA15N	4A30	BIOA07N
1C31		1A31		4C31		4A31	
1C32	+5VL	1A32	+5VL	4C32	+5VL	4A32	+5VL

* These signals are not used by PRO16/32.

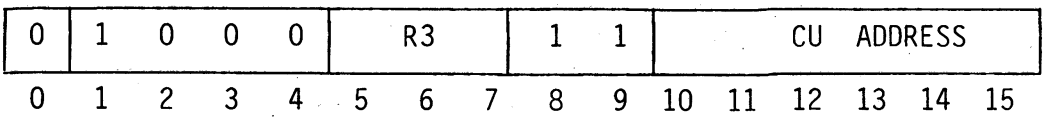
Table 10.5.3. CONNECTOR 1 (UPL-BUS) AND 4 (PRO16/32) OF P843-012

PIN NUMBER	SIGNAL NAME	PIN NUMBER
01	0V	08
02	DEVEN	09
03	IPGMEN	10
04	OE2N	11
05	IPGMEN2	12
06	+25V	13
07	+21VP	14

Table 10.5.4 INTERFACE P843-012 AND P851-010/012

10.5.4 HARDWARE-SOFTWARE INTERFACES DETAILS

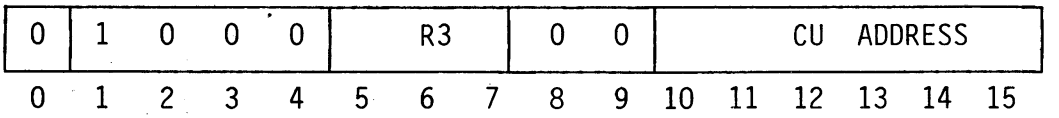
- CIO-START



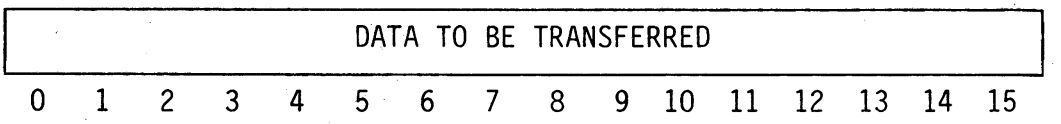
R3 Contents



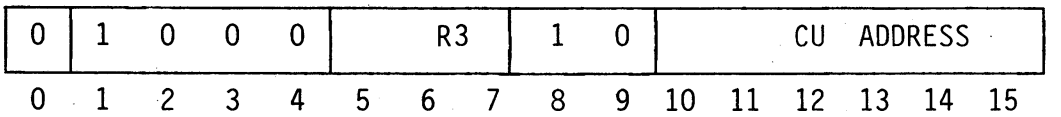
- OTR



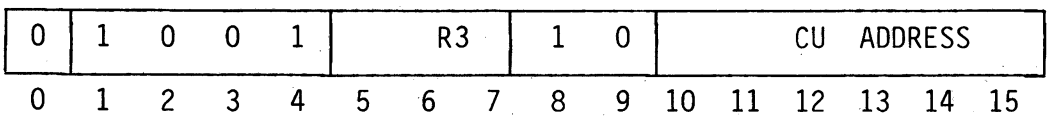
R3 Contents



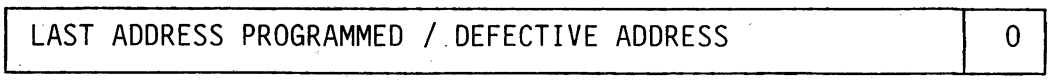
- CIO-HALT



- SST



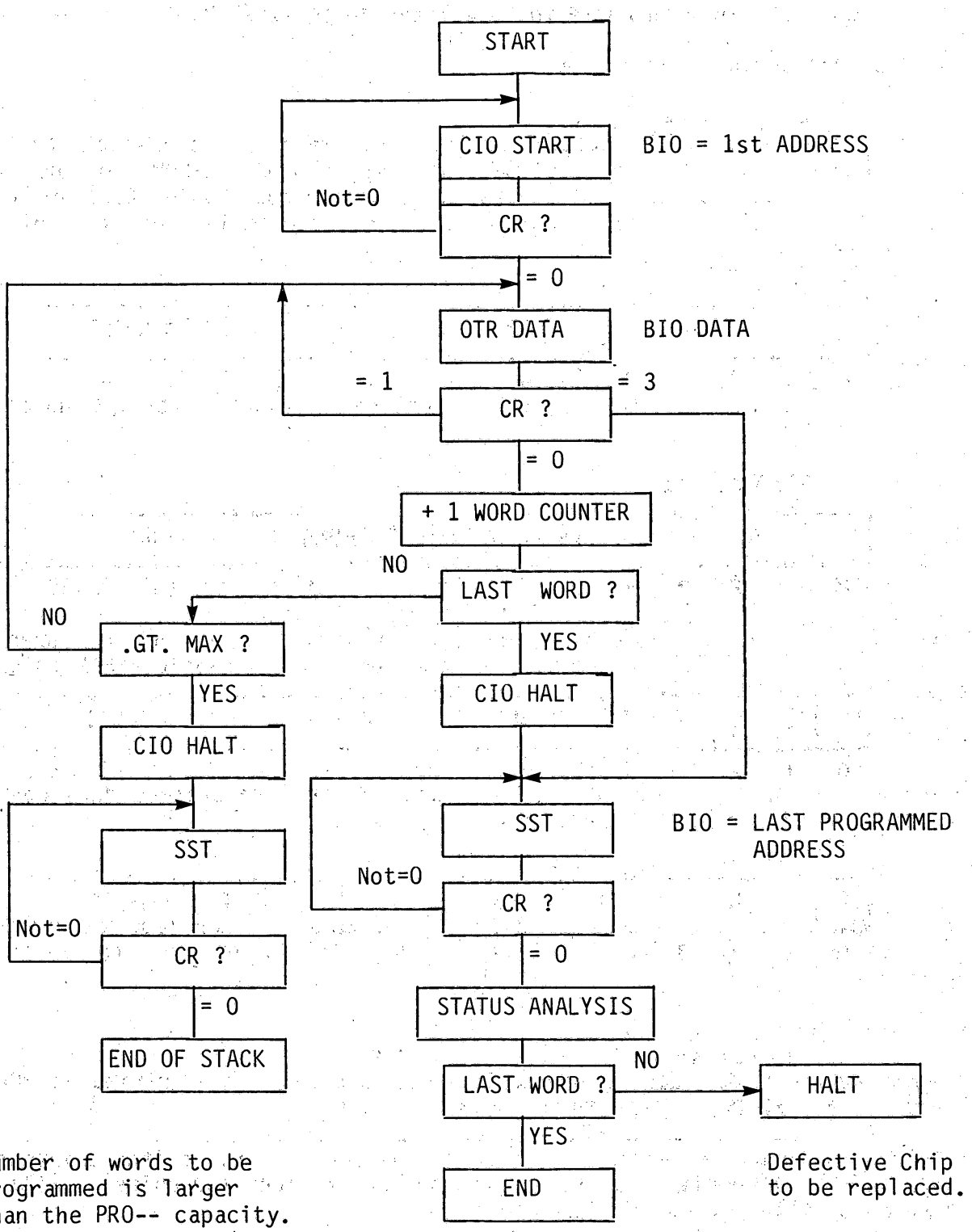
R3 Contents



10.5.5 APPLICATION NOTES

10.5.5.1 PRGT PROGRAMMING RULES

The PRO16 card is addressed between 0 and 32K-Bytes, and the PRO32 card is addressed between 0 and 64K-Bytes.



A standard operating software package is available with the PRGT2 card.

Figure 10.5.2. PRGT PROGRAMMING RULES

10.5.5.2 SYSTEM CONFIGURATION AND REQUIREMENTS

The system configuration requirements for a PRGT2 card is any basic P851 ore UPL machine with:

- At least one free slot for the PRGT2 card.
- Enough memory to hold the data to be written into the PROM.
- The required software utilities.

The Programming Tool acts as a normal Control Unit which can transfer data from the main memory of the system (i.e. RAM memory) into the EPROMs of the card connected to the PRGT2 card. The data is transferred in the form of word strings, and these strings are written (coded) into sequential locations of the PRO-- card memory area.

CONTROL UNIT OPERATING MODE

This CU only operates via the Programmed Channel without interrupt handling (Inhibit Mode).

CONTROL UNIT ADDRESSING

The CU address can be selected between 0 and /3F by means of U-links.

PRO-- PROGRAMMING FORMAT

The PRO-- is normally programmed 16 bits (1 word) at a time, but for special applications it is possible to write only one byte into a single EPROM chip if the other byte is written with /FF in a clean package.

PRO-- PROGRAMMING LENGTH

Programming is done Word by Word and the length of the transferred data can be any number of words up to the capacity of the PRO--.

PRO-- PROGRAMMING START ADDRESS

The PRO-- card is always positioned in the first block of the memory area, and the address of the first word to be transferred is one of the program parameters.

PRO-- PROGRAMMING VERIFICATION

After each word has been transferred, the data contents are verified at PRGT2 card level.

If after four attempts an error is detected, the control unit switches into the WST state and the defective byte(s) - lefthand and/or righthand chips - will be indicated by an illuminated LED (one per byte).

The defective address is set on the BION lines during the SST command.

10.6 SHORT DESCRIPTION OF TESTPROGRAMS

TESTPROGRAM BRAM

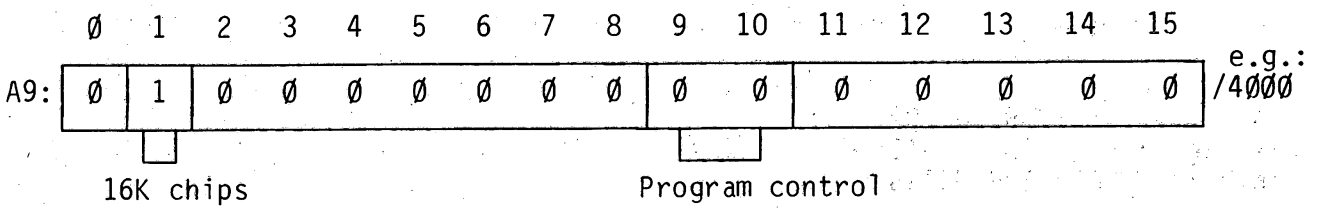
Test for up to 32 kw memory
No CTW or terminal output
RTC and PF/AR possible

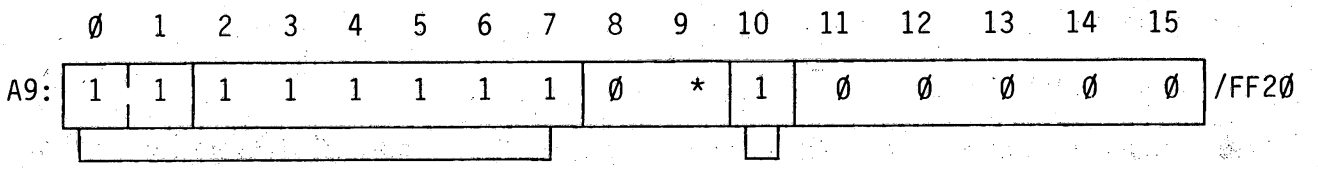
P876:
For MEM-module test:
O+MCL: SWITCH OFF CACHE

For CACHE test:
O+RUN: SWITCH ON CACHE

Procedure:

- IPL
- Program stops at /2ØØ (=restart address and correct end of test)
- Change registers:





1 = standard tests
* = optional test

(Memory is tested between address in A11 and end address in A12.)

- MCL, RUN

Test takes about 4 minutes.
Error stop at /1ØØ
Restart address after power off: /1DØ
Interrupt also stops at /1ØØ. A1 = 1Øxy.
Depress RST: displayed 6 ms bits indicate the interrupt level.

Error: A1 = /OOxy where x = phase no. and y = check no.
A2 = received pattern (wrong)
A3 = expected pattern
A4 = address of wrong pattern

Continuous test: A9 = /4Ø6Ø, MCL, RUN.
- Stop: by INST on HHP -or- interrupt.
- Address /B2 contains the no. of passes of the program.
/B4 contains the no. of detected errors.

For more information see the official testprogram description.

Note: Do not forget to SWITCH-ON the CACHE again (P876):
The LED on the CIP-C card must be "OFF".

BRAM tested:

Check	Standard Mode	Test	32kw
Ø	yes	All "Ø"	2s
1	yes	All "1"	2s
2	yes	Addressing test	2s
3	yes	Addressing test	2s
4	yes	Character test	4s
5	yes	Character test	4s
6	yes	Row disturb	5s
7	yes	Column disturb	5s
9	no	Ping pong	xxxx
10	yes	Butterfly	4min

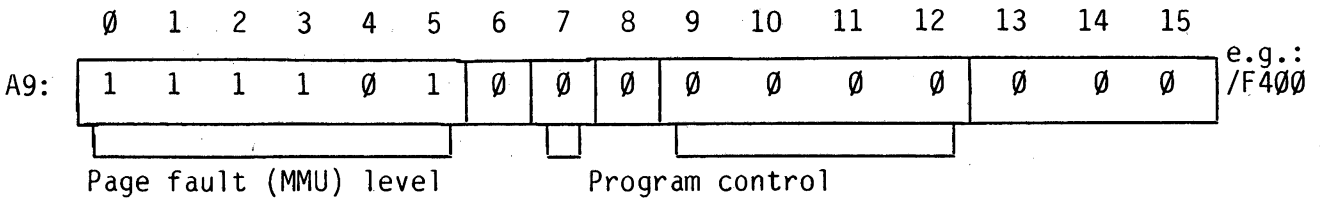
Procedure: 5111 991 08602
Listing : 5111 991 08613
Program : 5111 199 70773

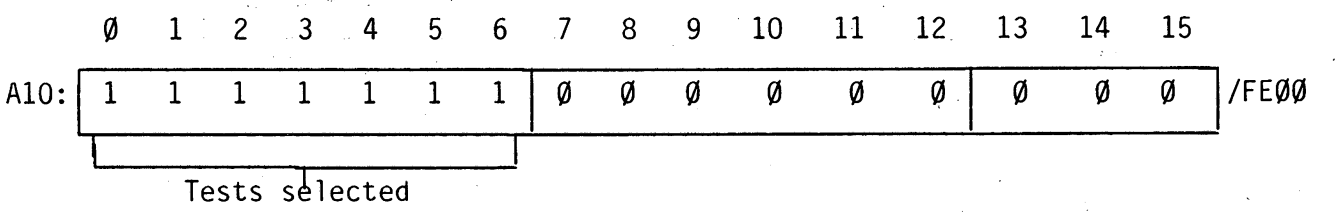
TESTPROGRAM BBRAM

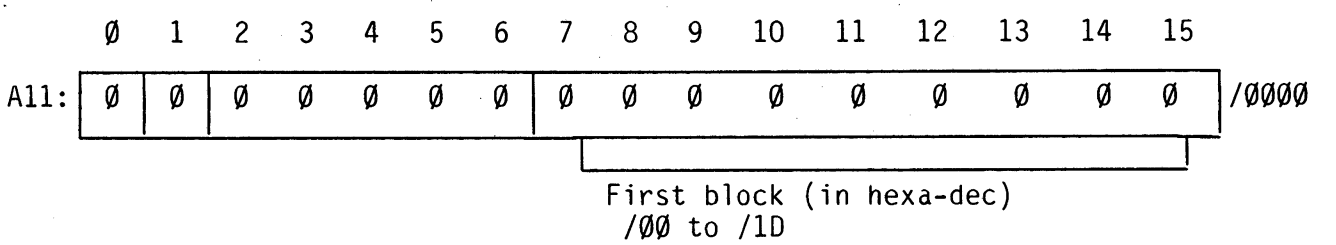
Test for MOS-memory 32kw up until 512 kw
MMU used
RTC and PF/AR possible
Procedure:
- IPL
  Program displays /7ØØ (= restart point and normal end of tests, interrupt returns to /7ØØ).
- Switch on RTC.
- Change registers

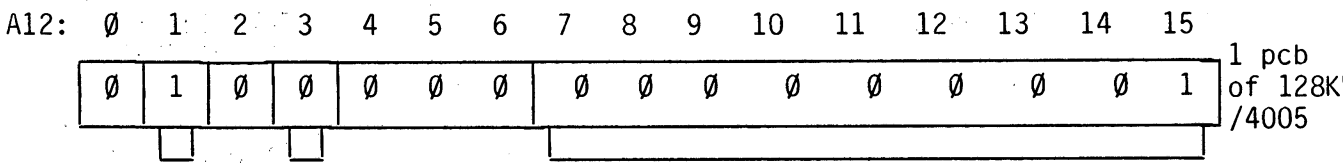
P876 For MEM-module test:
0+MCL: SWITCH OFF CACHE

For CACHE test:
0+RUN: SWITCH ON CACHE

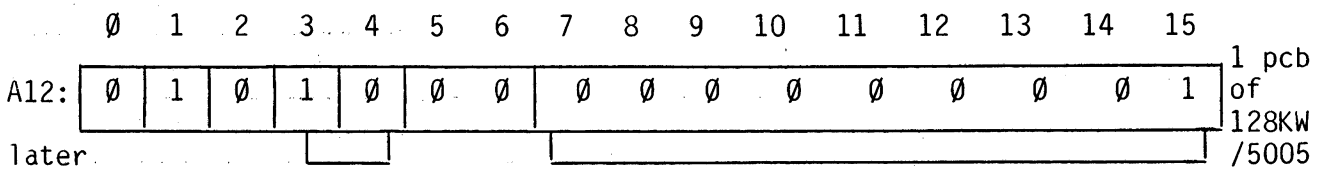








older versions:



later version:
(5111 199 65477)

Error stop at /5FØ
Information stop at /5EØ
Do not forget to SWITCH-ON the CACHE again (CIPC:LED "OFF").
For more information see the official testprogram description.

BBRAM - Blockdiagram for register A11 and A12:
Zone Ø to 32KW reserved for test program.

Ø	/Ø	1	/1	2	/2	3	/3
32 - 48		48 - 64		64 - 8Ø		8Ø - 96	
4	/4	5	/5	6	/6	7	/7
96-112		112-128		128-144		144- 16Ø	
8	/8	9	/9	10	/A	11	/B
16Ø - 176		176 - 192		192 - 2Ø8		2Ø8 - 224	
12	/C	13	/D	14	/E	15	/F
224- 24Ø		24Ø - 256		256 - 272		272 - 288	
16	/1Ø	17	/11	18	/12	18	/13
288 - 3Ø4		3Ø3 - 32Ø		32Ø - 336		336 - 352	
20	/14	21	/15	22	/16	23	/17
352 - 368		368 - 384		384 - 4ØØ		4ØØ - 416	
24	/18	25	/19	26	/1A	27	/1B
416 - 432		432 - 448		448 - 464		464 - 48Ø	
28	/1C	29	/1D				
48Ø - 496		496 - 512					

decimal value / Hexa-decimal value

X	Y
N - N+16KW	

LOCATION IN MEMORY

Note: 8 min for 1 WMD (P874,6) 18 min for 1 WMD (P871)

BBRAM - tested:

CHECK	STANDARD MODE	TEST	EXECUTE TIME FOR 16KW MODULE
Ø	Yes	All "Ø" All "1"	1 sec
1	Yes	Addressing Test	1 sec
2	Yes	Character Test	5 sec
3	Yes	Row disturb	6 sec
4	Yes	Column disturb	6 sec
5	No	Diagonal Test	1 min
6	No	Butterfly Test	2 min

Procedure 5111 991 10237
Listing 5111 991 10247
Program 5111 199 65477

Program MEM

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	818E	Write	LDR	A9, A11
0088	85A7	Load	STR	A13, A9
008A	91A0		ADKL	A9, 2
008C	0002			
008E	E992		CWR	A9, A12
0090	5C0A		RB (4)	Load
0092	5700		RF	* +2
0094	818E		LDR	A9, A11
0096	80A6	RDC	LDR*	A8, A9
0098	E896		CWR	A8, A13
009A	5002		RF(0)	Suit 3
009C	207F		HLT	Fault
009E	91A0	Suit 3	ADKL	A9, 2
00A0	0002			
00A2	E992		CWR	A9, A12
00A4	5C10		RB (4)	RDC
00A6	5F22		RB	Write

Start the program:

- Load the starting address in register A11
- Load the ending address in register A12
- Load the test-pattern in register A13
- Load the start-address of the program (/0086) into register A0
- Push the RUN button

After Start:

If no fault the program runs in loop

Fault: program stops at /009E

- A9 contains address of erronous memory location
- A8 contains read pattern
- A13 contains expected pattern

DUMP FACILITY

This program enables an area of memory to be printed out on either the ASR or PTS3100, or to be Displayed. It can be loaded either with the IPL routine or by hand using the control panel switches. Once loaded the following routine should be used:

- Load the starting address to be printed into register A7. *)
- Load the ending address of the area into register A8.
- Load the starting address of the program into register A0.
- Push the RUN button.

The program will stop when the last memory address has been either printed or displayed.

*) Bit 15 must be zero.

Program DUMP

Memory Address	Data	Program Instructions		
0080	FFFF		DATA	-/FFFF
0082	0000		DATA	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	47D0		CIO	A7,1,/10
008A	813C	WORD	LDR *	A1,A7
008C	0204		LDK	A2,4
008E	060F	CONT	LDK	A6,/F
0090	A604		ANR	A6,A1
0092	E558		LC	A5, TABLE, A6
0094	00BE			
0096	E549		SC	A5,BUFF + 1.A2
0098	00CF			
009A	39E4		SRC	A1,4

Memory Address	Data	Program Instructions		
009C	1A01		SUK	A2,1
009E	5C12		RB(NZ)	CONT
00A0	E348	OUT1	LC	A3,BUFF,A2
00A2	00CE			
00A4	4310		OTR	A3,0,/10
00A6	5C04		RB(NA)	* -2
00A8	1201		ADK	A2,1
00AA	EA20		CWK	A2,6
00AC	0006			
00AE	5C10		RB(NE)	OUT1
0080	1702		ADK	A7,2
00B2	EF02		CWR	A7,A8
00B4	5D2C		RB(NG)	WORD
00B6	4790		CIO	A7,0,/10
00B8	4FD0		SST	A7,/10
00BA	5C04		RB(NA)	* -2
00BC	5F3A		RB	START
00BE	3031	TABLE	DATA	'0123456789'
00C0	3233			
00C2	3435			
00C4	3637			
00C6	3839			
00C8	4142		DATA	'ABCDEF'
00CA	4344			
00CC	4546			
00CE	0D0A	BUFF	DATA	/0D0A

```
00000                          IDENT    MEM3
00001                 *MEMORY TEST FOR MEMORY FROM 32KW TILL END OF MEM
00002                 *
00003                 *(A1)=MOST SIGNIFICANT MEMORY ADDRESS
00004                 *(A2)=LEAST SIGNIFICANT MEMORY ADDRESS
00005                 *(A3)=BEGIN ADDRESS TO TEST (MOST SIGNIFICANT PART)
00006                 *(A5)=PAL.....,PAM OF MMU TABLE
00007                 *(A6)=TEST PATTERN (ROTATED)
00008                 *(A7)=TEST PHASE : 1, 2 OR 3
00009                 *(A8)=NUMBER OF COMPLETE TEST CYCLES
00010                 *(A9)=MEMORY END ADDRESS (MOST SIGN.)
00011                 *(A10)=MEMORY END ADDRESS LEAST SIGNIFICANT
00012                 *(A11)=
00013                 *(A12)=WANTED TEST PATTERN
00014                 *(A13)=TEST PATTERN (ROTATED), READ FROM MEMORY
00015                 *(A14)=WRITTEN DATA OF TEST-PHASE 1
00016                 *(A15)=READ DATA OF TEST-PHASE 1
00017                 *
00018                 *AFTER LOADING THE PROGRAM THE NEXT REGISTERS CAN BE CHANGED:
00019                 *    -A3 :MOST SIGNIFICANT PART OF BEGIN ADDRESS
00020                 *     A3 PRESET WITH /0001 = 32KW BASE
00021                 *    -A12:TEST PATTERN FOR TEST PHASE 2 & 3
00022                 *REGISTER A8 WILL COUNT THE NUMBER OF COMPLETE TEST CYCLES AND
00023                 * THE PROGRAM STAYS RUNNING UNTIL AN ERROR IS FOUND
00024                 *  REGISTERS A1 & A2 CONTAIN THE ERROR ADDRESS,
00025                 *             A7 CONTAINS THE TEST PHASE: 1= ALL /5555, /AAAA
00026                 *                                         2= WRITE TEST PATTERN
00027                 *                                         3= READ TEST PATTERN
00028                 *
00029  0000                          RES      /40
00030  0080  FFFF                    DATA     /FFFF,0
       0082  0000
00031  0084  208F             START  INH
00032  0086  80A0                    LDKL     A8,0
       0088  0000
00033  008A  0301                    LDK      A3,1
00034  008C  0701                    LDK      A7,1
00035  008E  84A0                    LDKL     A12,/3569              DEFAULT TEST PATTERN
       0090  3569
00036  0092  207F             RESTAR HLT
00037  0094  810C             NEXTPH LDR      A1,A3                  0000000000000001
00038  0096  8504             NEX32K LDR      A5,A1                  0000000000000001
00039  0098  3DE2                    SRC      A5,2                   0100000000000000
00040  009A  0400                    LDK      A4,0
00041  009C  8551             NEXWRD ST       A5,TABLE,A4
       009E  0126  R
00042  00A0  1402                    ADK      A4,2
00043  00A2  9520                    ADKL     A5,/400                INCREMENT PAL WITH 1
       00A4  0400
00044  00A6  EC20                    CWK      A4,32                  16 WORDS PREPARED
       00A8  0020
00045  00AA  5C10                    RB(NE)   NEXWRD
00046  00AC  8840                    TL       TABLE
       00AE  0126  R
00047  00B0  EF20                    CWK      A7,1                   TEST PHASE 1 OR HIGHER?
       00B2  0001
00048  00B4  5130                    RF(G)    TEST2
00049  00B6  0200             TEST1  LDK      A2,0                   PROGRAM ADDRESS 0
00050  00B8  86A0             TES32K LDKL     A14,/5555              CHECK FIRST 32K
       00BA  5555
00051  00BC  D6A9                    ESR      A14,A2                 WITH /5555 AND
00052  00BE  D7A8                    ELR      A15,A2
00053  00C0  EE9E                    CWR      A14,A15
00054  00C2  5412                    RF(NE)   MEMEND
00055  00C4  969A                    ADR      A14,A14
00056  00C6  D6A9                    ESR      A14,A2                 WITH /AAAA
00057  00C8  D7A8                    ELR      A15,A2
00058  00CA  EE9E                    CWR      A14,A15
00059  00CC  5408                    RF(NE)   MEMEND
00060  00CE  1202                    ADK      A2,2
00061  00D0  5C1A                    RB(NZ)   TES32K
00062  00D2  1101                    ADK      A1,1                   NEX 32K RELOAD THE TABLE
00063  00D4  5F40                    RB       NEX32K
00064  00D6  EFA0             MEMEND CWK      A15,0
       00D8  0000
00065  00DA  5448                    RF(NZ)   ERROR1
00066  00DC  8288                    LDR      A10,A2
00067  00DE  8184                    LDR      A9,A1                  (A9,A10)=MEMORY END ADDRESS
00068  00E0  0702                    LDK      A7,2                   FLAG FOR TESTPHASE 2
00069  00E2  8612                    LDR      A6,A12                 LOAD ROTATE REG WITH TEST PATTERN
00070  00E4  5F52                    RB       NEXTPH
00071  00E6  0200             TEST2  LDK      A2,0
00072  00E8  EF20                    CWK      A7,2                   PHASE 2 OR 3 ?
       00EA  0002
00073  00EC  5112                    RF(G)    TEST3
00074  00EE  D629             TES32  ESR      A6,A2
00075  00F0  3EE3                    SRC      A6,3
00076  00F2  1202                    ADK      A2,2
00077  00F4  5C08                    RB(NZ)   TES32
00078  00F6  1101                    ADK      A1,1
00079  00F8  E906                    CWR      A1,A9                  COMPARE END ADDR (N X 32K)
00080  00FA  5D66                    RB(NG)   NEX32K
00081  00FC  0703                    LDK      A7,3                   FLAG TEST PHASE 3
00082  00FE  5F6C                    RB       NEXTPH
```

```
00083  0100  0200       TEST3    LDK      A2,0
00084  0102  D5A8       TST32    ELR      A13,A2
00085  0104  ED98                CWR      A13,A6
00086  0106  540C                RF(NE)   ERROR3
00087  0108  3EE3                SRC      A6,3
00088  010A  1202                ADK      A2,2
00089  010C  5C0C                RB(NZ)   TST32
00090  010E  1101                ADK      A1,1
00091  0110  E906                CWR      A1,A9
00092  0112  5D7E                RB(NG)   NEX32K
00093  0114  EA0A       ERROR3   CWR      A2,A10
00094  0116  520C                RF(L)    ERROR1
00095  0118  E906                CWR      A1,A9
00096  011A  5208                RF(L)    ERROR1
00097  011C  0701                LDK      A7,1
00098  011E  90A0                ADKL     A8,1
       0120  0001
00099  0122  5F90                RB       NEXTPH
00100  0124  5F94       ERROR1   RB       RESTAR
00101  0126              TABLE    RES      16
00102                              END      START


          SYMBOL TABLE

  ERROR1  0124  R   ERROR3  0114  R   MEMEND  0006  R   NEX32K  0096  R
  NEXTPH  0094  R   NEXWRD  009C  R   RESTAR  0092  R   START   0084  R
  TABLE   0126  R   TES32   00EE  R   TES32K  0088  R   TEST1   0086  R
  TEST2   00E6  R   TEST3   0100  R   TST32   0102  R

          ASS.ERR.    00000
:EOF
PROG ELAPSED TIME:  00H-00M-42S-060MS-
```

Note: In the P876 this short routine can be used to find an erronous address in the CACHE memory at CIPG or CIPF of the CP2B. It is possible to disable only the CACHE at CIPF by removing the U-Links S12 (CACHE-A) and S13 (CACHE-B). In this way an error caused by CIP-F can be eliminated, so that the CIP-G card can be tested separately.

First run this test without CACHE memory (Switch off the CACHE by pressing the "0" and "MCL" buttons on FRCP).
After that run the test with CACHE memory (Switch on the CACHE by pressing the "0" and "RUN" buttons on FRCP).

If no errors occur the program runs repeatedly and the memory size can be read from register A9.
(A9 contains the total number of 32KW area's present)

If an error is detected. the program stops and information is found in the registers A2, A6, A13, A14, A15:

	TEST PHASE (A7)		
DESCRIPTION	1	2	3
ERROR ADDRESS CORRECT CONTENT ERRONOUS CONTENT	A2 A14 A15	A2 A6 A13	A2 A6 A13

* It is possible to disable only the CACHE at CIPF by removing the U-links S112 (CACHE-A) and S113 (CACHE-B). In this way an error caused by CIP-F can be eliminated, so that the CIP-G card can be tested separately.

11 MEMORY MANAGEMENT UNIT

SECTION	11.1	MEMORY MANAGEMENT UNIT IDENTIFICATIONS	PAGE 11-2
	11.2	MEMORY MANAGEMENT UNIT FUNCTIONS	11-2
	11.3	SHORT DESCRIPTION OF TESTPROGRAMS	11-5
	11.4	SHORT ROUTINE	11-8

LIST OF ILLUSTRATIONS

FIGURE	11.1	MEMORY MANAGEMENT	11-3
	11.2	PAGE FAULT SEQUENCE	11-4

11.1 MEMORY MANAGEMENT UNIT (MMU) - IDENTIFICATIONS

Type Number : Standard with P874 (MIOP), and P871/6 (integrated)

Testprogram : REPAF, REMMU1, PAF2B, MMU2B

Power Consumption : Refer to CPU (MIOP), see chapter 7, 8 and 9

11.2 MEMORY MANAGEMENT UNIT - FUNCTIONS

The Memory Management Unit (MMU) is a hardware facility which provides extended memory addressing and memory protection facilities for the P871/4/6 systems.

EXTENDED MEMORY ADDRESSING (TRANSLATION)

The principal function of the MMU is to extend the memory addressing up to 8M physical words (24 address bits). (See Figure 11.1)
The basic rules for the operation of this facility are as follows:

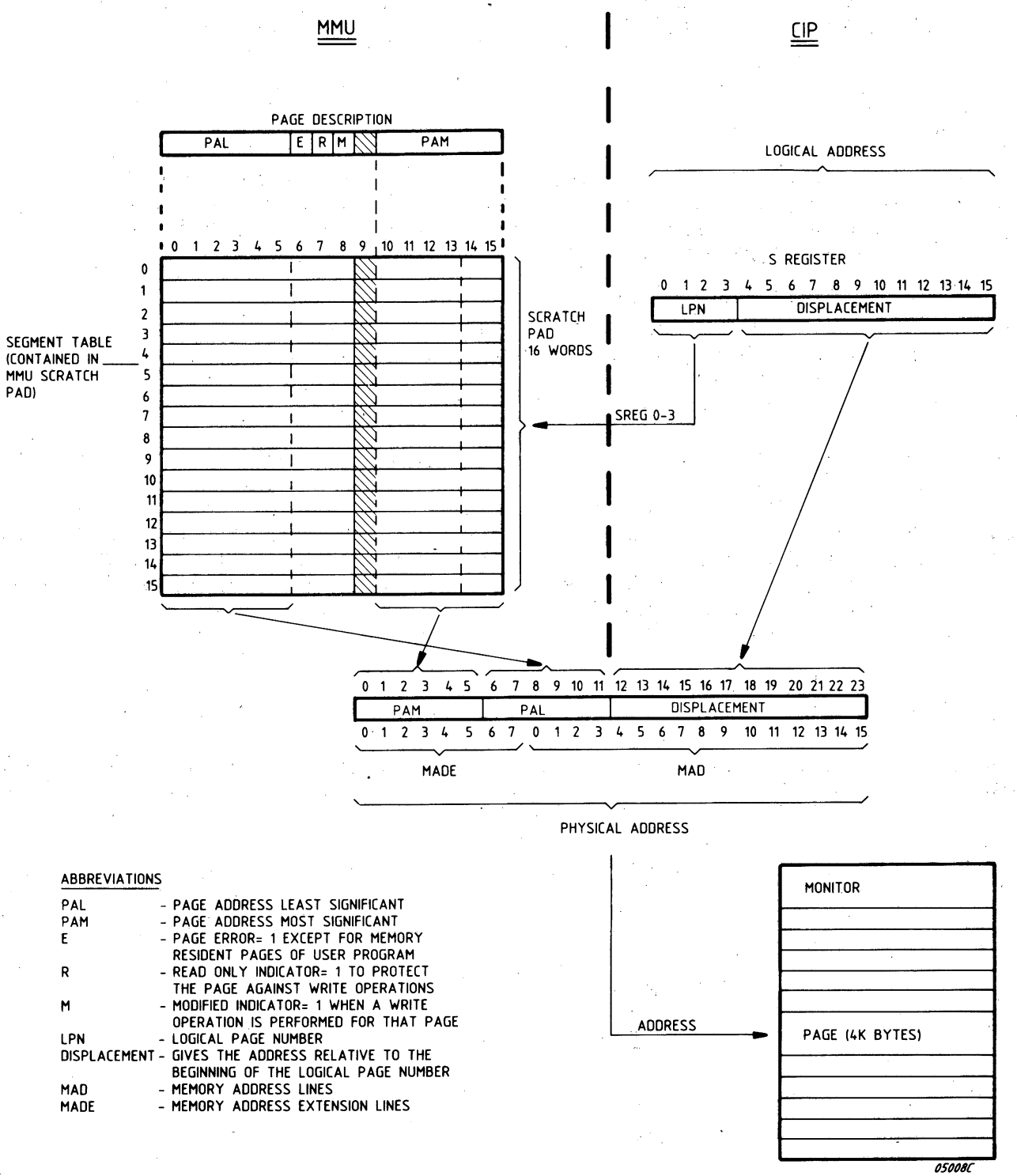
- A 16 word segment table is pre-loaded with page addresses by one Table Load Instruction.
- All CPU/Memory transfers via the MMU use the four most significant address lines (MAD0-3) to select the table segment (page 0-15). The content of each page gives the 12 most significant MAD address bits plus 3 control bits.
- The Table Store instruction is used by software to read the 16 word segment table for test purposes or for dynamic relocation.

MEMORY PROTECTION

For memory protection purposes 2 information bits are loaded into the segment table at the same time that the TL instruction loads the page addresses; these information bits are:

- Bit 6 (E) Page Error if 1, page restricted to system mode only.
- Bit 7 (R) Read Only Indicator = 1 to protect the page against Write operations If an address translation in User Mode attempts to Write on this page then the translation is blocked.

In both of these cases the MMU indicates to the CPU that a Page Fault (PAF) has occured.



ABBREVIATIONS

PAL	- PAGE ADDRESS LEAST SIGNIFICANT
PAM	- PAGE ADDRESS MOST SIGNIFICANT
E	- PAGE ERROR= 1 EXCEPT FOR MEMORY RESIDENT PAGES OF USER PROGRAM
R	- READ ONLY INDICATOR= 1 TO PROTECT THE PAGE AGAINST WRITE OPERATIONS
M	- MODIFIED INDICATOR= 1 WHEN A WRITE OPERATION IS PERFORMED FOR THAT PAGE
LPN	- LOGICAL PAGE NUMBER
DISPLACEMENT	- GIVES THE ADDRESS RELATIVE TO THE BEGINNING OF THE LOGICAL PAGE NUMBER
MAD	- MEMORY ADDRESS LINES
MADE	- MEMORY ADDRESS EXTENSION LINES

Figure 11.1 MEMORY MANAGEMENT

MODIFIED PAGE

This feature indicates to the operating system if a page needs to be "swapped out" or not. If it does not need to be "swapped out" then the new page can be overwritten so saving time. This possibility is indicated by bit 8 (M) which is set to "1" by the MMU whenever a Write operation (Store Instruction) is performed on a specific page.

PAGE FAULT

When an attempt is made to write into a protected page or access is made in user mode to a page that is restricted to system mode only, the MMU signal "Page Fault" initiates an interrupt TRAP Routine at the CPU. The sequence of events is indicated in the following Flow Chart:

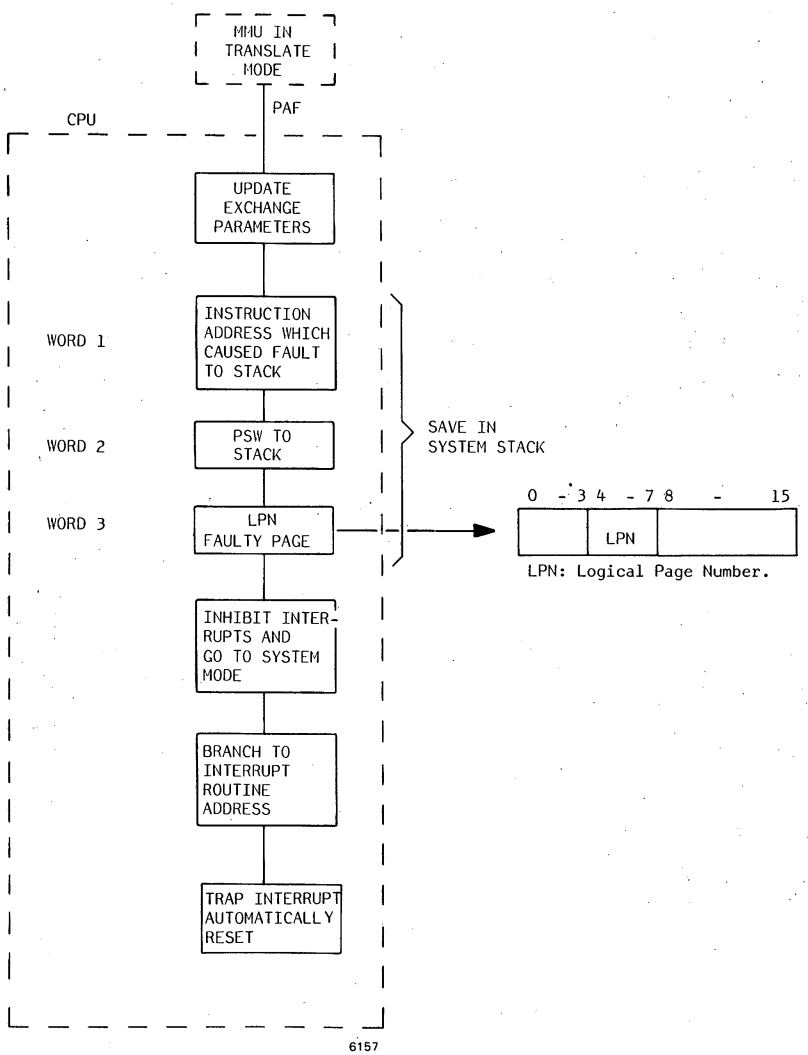


Figure 11.2 PAGE FAULT SEQUENCE

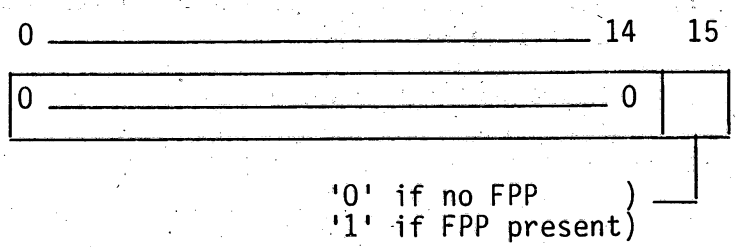
11.3 SHORT DESCRIPTION OF TESTPROGRAMS

PROGRAM REPAF(P874)
PAF2B(P871/6)
32 KW memory min.
test for page fault, RTC and PF/AR

. IPL

. Stop at /400

Modify register: A10



. MCL, RUN

- Switch on the RTC (LOCK for PF/AR)

. - The program loops continuously . /2B4 contains test loop counter = check on run-. (one loop lasts about 0.5 sec.).
- Error: program stops. A6 contains error info.
- Stop at /31A: reception of unexpected interrupt.
- /2B6 contains counter for no. of auto restarts.
- Restart address is /3EA (after power fail).

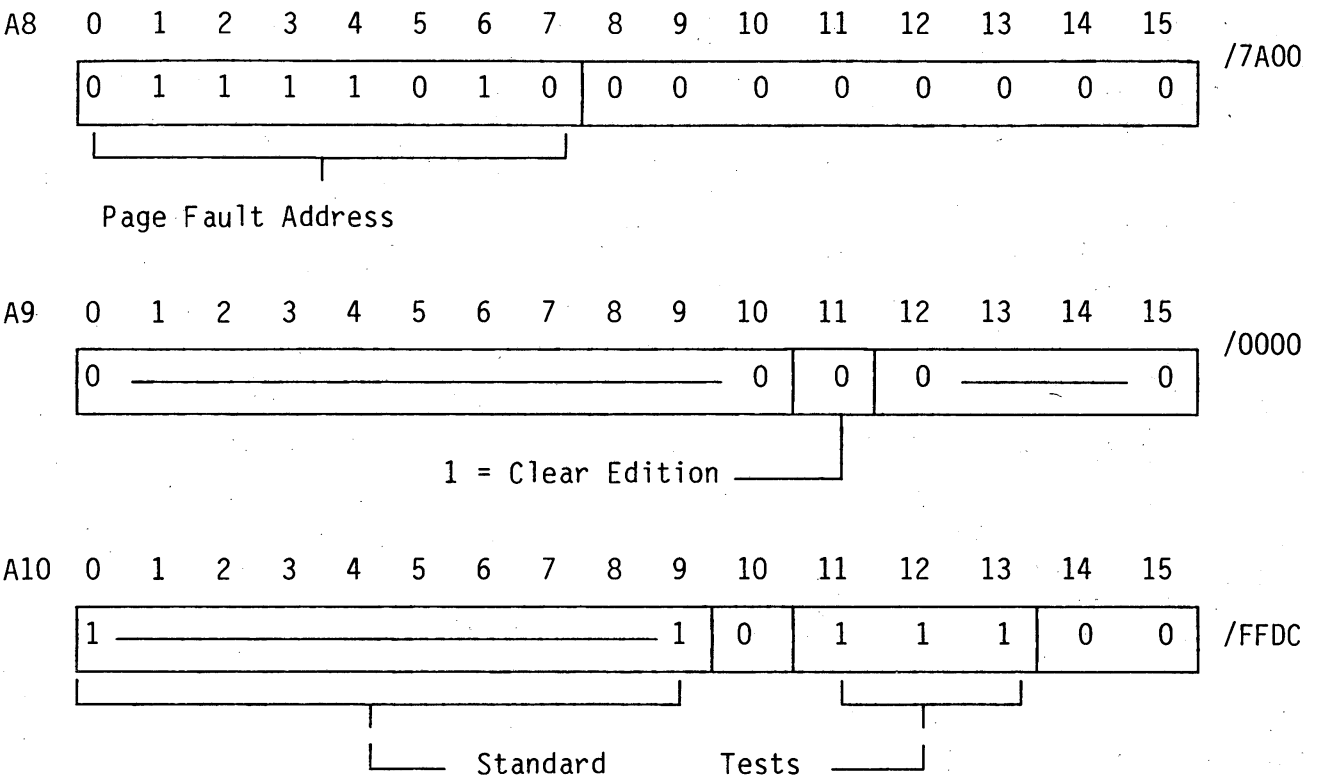
For more information see official description of testprograms.

PROGRAM REMMU1(P871/4) Memory size 32 KW min.
Test of MMU in memory size 0 - 32 KW

. IPL

. Stop at /700 = restart address = after reception of unexpected interrupt.

- Change registers:



Switch on RTC (PF/AR also possible).

. MCL, RUN

. /700 Normal end.

- /5E0 Info stop (A1 may contain info code).

- /5F0 Error stop A1 contains error code (see also official description of testprogram).

- Restart after power off: /6EE.

Note: Some checks are in inhibit mode. In such a case the power fail interrupt may be handled too late and auto restart fails.

Procedure : 5111 991 10392
Listing : 5111 991 10382
Program : 5111 199 64942

TESTPROGRAM MMU2B (P871/6)

Memory size 32KW minimum
PF/AR and RTC allowed

This program tests the memory management unit of the CP1BF and CP2B CIP's.
Procedure:

- IPL
- Change register contents:

```
      Ø  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15
A8:  | page fault trap addr.          | 0 ---------- 0 |  eg./7A00

      Ø  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15
A9:  | 1  N | 0 ---------- 0 | prog.   control  | Ø  Ø  0 |  eg./C000

        N = 0: CP1BF
        N = 1: CP2B

      0  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15
A10: | 1  1  1  1  1  1  1  1  1  1  1  1  1  1  1 | 0 |  eg. /FFFE
      ------------------------------------------------
                  checks to be executed
```

- start
  output message: (No. of CHECK executed)

IF 0000
IF 0001
...2
IF 0014

Program run takes about 2 seconds.

Note, After IPL, the program stops at /700 = program end = restart = interrupt
Restart after power off from /6EE.
Error stop = /5F0 ; information stop = /5E0

-- For further information, see the official testprogram description ---

Tested:
- IF 0000 check 00 : TLR, TSR, TL, TS : system mode
- IF 0001 check 01 : ELR, ESR, EL, ES : system mode
- IF 0002 check 02 : MVSU, MVUS : system mode
- IF 0003 check 03 : Privileged instructions : user mode
- IF 0004 check 04 : User program in successive pages
- IF 0005 check 05 : User program in random pages
- IF 0006 check 06 : Test bit Modify
- IF 0007 check 07 : Test bit Page Error
- IF 0008 check 08 : Test bit Read Only
- IF 0009 check 09 : System mode : non error performing
- IF 0010 check 10 : Test extended system mode
- IF 0011 check 11 : MVB, MVF, Page Fault resuming
- IF 0012 check 12 : ML, Page Fault resuming
- IF 0013 check 13 : Test bit read only if memory 32x
- IF 0014 check 14 : Test of stack overflow

Procedure : 5111 991 13081
Listing : 5111 991 13091
Program : 5111 199 56971

```
00000                                IDENT    MMU2C
00001                          *
00002                          *
00003                          *PROGRAM TO TEST MMU FUNCTIONS
00004                          *
00005                          *THE USER PART OF THIS PROGRAM WILL BE TRAPPED ON A NOT ALLOWED
00006                          *STORE OPERATION IN PAGE 2.
00007                          *EACH TIME THE CP-INT BUTTON IS PRESSED, THE PROGRAM WILL BE
00008                          *MODIFIED, GIVING TRAPS ON ACCESS PAGE 1 OR WRITE ACCESS PAGE 2
00009                          *WHEN THE PROGRAM IS STOPPED BY A HLT INSTRUCTION IT IS POSSIBLE
00010                          *TO CHECK THE SYSTEM STACK (A15) AND THE SEGMENT TABLE (/300).
00011                          *
00012        0006    CPLEV     EQU      6                    FOR P854: /E IF P858/P859
00013                          AORG     /100
00014                          *
00015                          *
00016  0100  8841    PROGINT   TS       /300                 SEGMENT TABLE TO MEMORY
       0102  0300
00017  0104  20F8              RIT      /1D
00018  0106  207F              HLT                           CHECKPOINT:TABLE + STACK
00019  0108  8840              TL       /200                 LOAD SEGMENT TABLE INTO MIOP
       010A  0200
00020  010C  87A0              LDKL     A15,/150             LOAD STACK POINTER
       010E  0150
00021  0110  8120              LDKL     A1,/FFE              PROGRAM COUNTER OF USER
       0112  0FFE
00022  0114  813F              STR      A1,A15               TO THE STACK
00023  0116  8120              LDKL     A1,/4041             PSW OF USER
       0118  4041
00024  011A  813F              STR      A1,A15               TO THE STACK
00025  011C  8120              LDKL     A1,/160              START ADDRESS TRAP ROUT.
       011E  0160
00026  0120  8141              ST       A1,/7A               PAGE FAULT TRAP ENTRY
       0122  007A
00027  0124  8120              LDKL     A1,/100              START ADDRESS PROG.INT ROUT.
       0126  0100
00028  0128  8141              ST       A1,2                 LEVEL 1
       012A  0002
00029  012C  8120              LDKL     A1,/400              START ADDRESS CPINT ROUTINE
       012E  0400
00030  0130  8141              ST       A1,CPLEV             LEVEL:P854=3,(P858/9=7)
       0132  0006
00031  0134  F03E              RTN      A15                  START USER PROGRAM (LEVEL=/10)
00032                          AORG     /160
00033                          *
00034                          *
00035  0160  8841    TRAP      TS       /300                 SEGMENT TABLE TO MEMORY
       0162  0300
00036  0164  207F              HLT                           CHECKPOINT:TABLE + STACK
00037  0166  8120              LDKL     A1,/200C             RESTART USER
       0168  200C
00038  016A  8141              ST       A1,/150              PROGRAM AT ADDRESS /200C (=/300C)
       016C  0150
00039  016E  813E              LDR*     A1,A15               A15 ADJUSTED +2 AFTER PAGE FAULT TRAP
00040  0170  F03E              RTN      A15
00041                          AORG     /200
00042                          *
00043                          *
00044  0200  0000    SEGTAB    DATA     /0000                SEGMENT TABLE PAGE 0
00045  0202  0400              DATA     /0400                PAGE 1
00046  0204  0D00              DATA     /0D00                PAGE 2
00047                          AORG     /400
00048                          *
00049                          *
00050  0400  8120    CPINT     LDKL     A1,/200              ROUTINE TO CHANGE TABLE :PAGE 1
       0402  0200
00051  0404  8141              XRS      A1,/202              BIT 6 (E) SET OR RESET
       0406  0202
00052  0408  200F              RIT      /0F                  RESET CONTROL PANEL INT.
00053  040A  F03E              RTN      A15                  GO BACK TO USER PROGRAM
00054                          AORG     /FFE
00055                          *
00056                          *
00057  0FFE  013F    USER      LDK      A1,/3F               PAGE 0 IS ACCESSED
00058  1000  1102    PAGE1     ADK      A1,2                 PAGE 1 IS ACCESSED
00059  1002  8F20              ABL      /2000                BRANCH TO PAGE 2 (/3000)
       1004  2000
00060                          AORG     /3000
00061                          *
00062                          *
00063  3000  8141    PAGE2     ST       A1,/500              STORE INTO PAGE 0
       3002  0500
00064  3004  8140              LD       A1,/2200             LOAD FROM PAGE 2
       3006  2200
00065  3008  8141              ST       A1,/2200             STORE INTO PAGE 2 (TRAPPED)
       300A  2200
00066  300C  2804              LKM                           CALL SYSTEM MODE VIA PROG. INT
00067  300E  0000              DATA     0
00068                          END
```

12 INPUT/OUTPUT PROCESSOR P843-120 (IOPZR)
P874 (MIOP)

SECTION	12.1	IOP IDENTIFICATION	PAGE 12-2
	12.2	INSTALLATION DETAILS IOPZR	12-3
	12.3	INTERFACE CONNECTIONS IOPZR	12-4
	12.4	HARDWARE SOFTWARE INTERFACE DETAILS	12-5

LIST OF ILLUSTRATIONS

FIGURE	12.1	U-LINK SETTING IOPZR	12-3

12.1 IOP IDENTIFICATIONS

Type number : P843-120 (IOPZR)
P857E MIOP, see also CPU chapter 8

Power consumption : +5Volt, 2.75Amp. (IOPZR)

12NC code on the sticker on the board.
IOPZR: 5111 199 6670x (5322 216 25446)

X = modification level.

12.2 INSTALLATION DETAILS IOPZR

U-links on IOPZR card to select:
- IOP address (MIOP card, if present, always is IOP address 0 and 1 for IOP-A and B).
- First or second level of priority for individual CU break requests (signal ERQN)
- Time delay for timing signal TSMN.

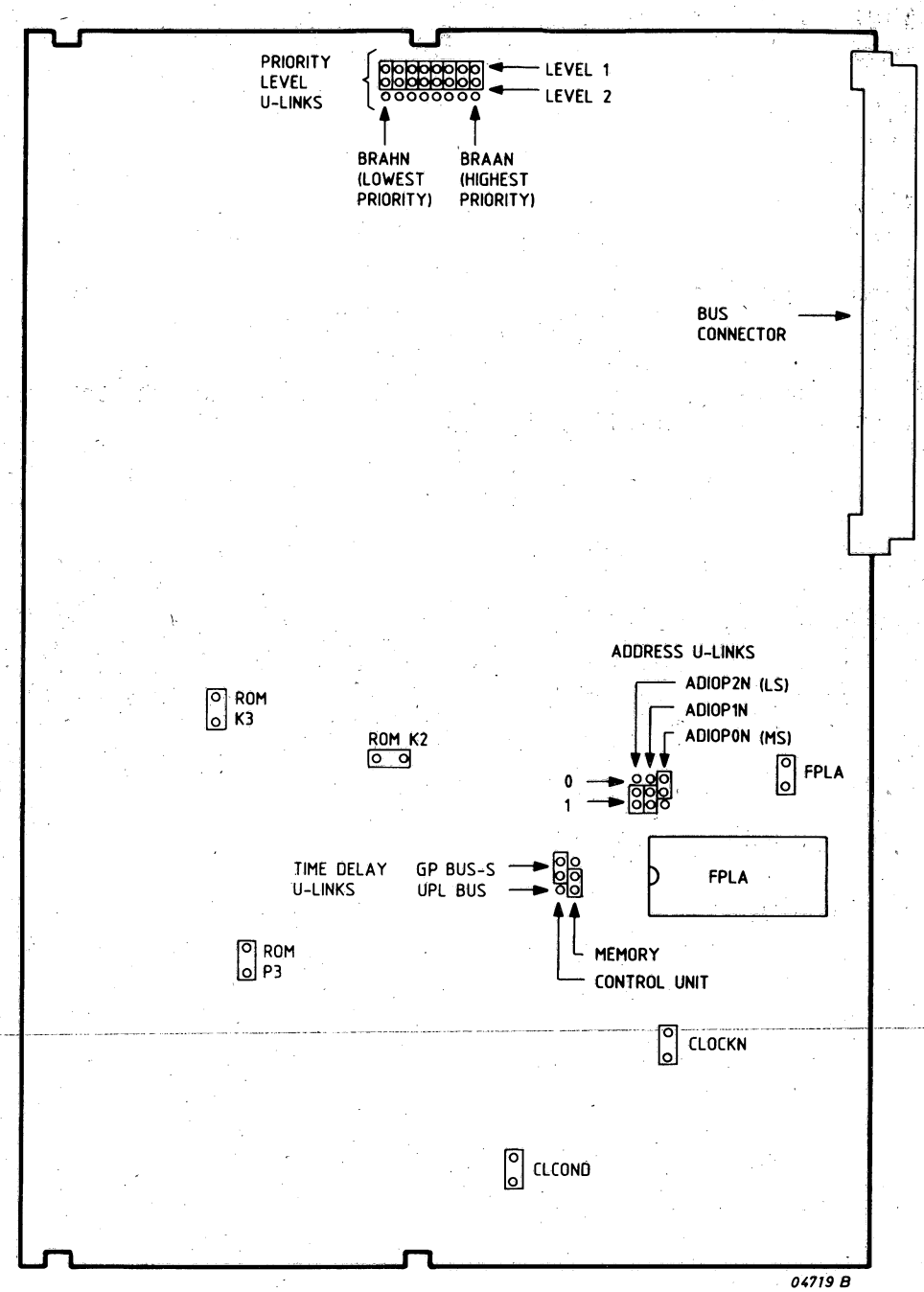


Figure 12.1 U-LINK SETTING IOPZR

Priority level U-links shown for all CU's at level 1. Address U-links shown for IOP address 3.
Test U-links (ROM K3, ROM K2, ROM P3, FPLA, CLOCKN, CLCOND) must be fitted when IOP is under normal operation.
- If both types of CU's (UPL and GP) are used with IOP, the CU-strap must be set in GP position (simular for memory strap).

12.3 INTERFACE CONNECTIONS IOPZR

The IOP communicates with the rest of the system via the UPL-bus. Break connections from the individual CU's are made by jump leads on the backpanel.
For master selection on the bus, OKO-OKI wiring must be present on the backpanel.

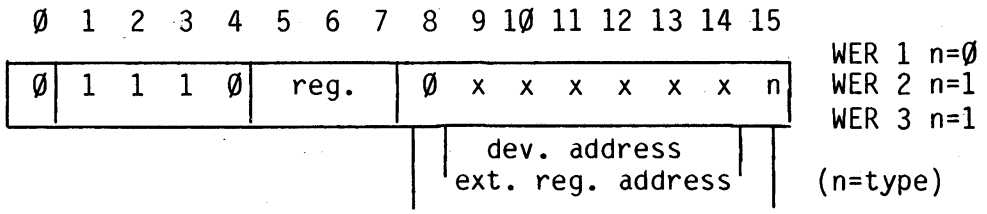
UPL backpanel

Signal:	Pin:
OKI	1BØ7
OKO	1BØ6
BRØØN	1B22
BRØ1N	1B23
BRØ2N	1B24
BRØ3N	1B25
BRØ4N	1B27
BRØ5N	1B28
BRØ6N	1B29
BRØ7N	1B3Ø

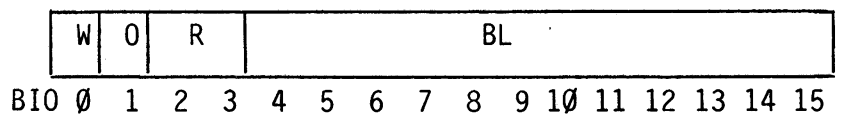
BUS signal ERQN (Pin 1BO1) is used for second level Break Priorities, only on IOPZR and not on MIOP. (see chapter 1; BUS ALLOCATION).

12.4 HARDWARE-SOFTWARE INTERFACE DETAILS

IOP Instructions: (MIOP, IOPZR):

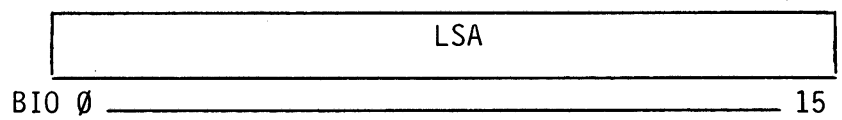


The 3 WER instructions must be programmed in a fixed sequence, the 3 following parameters being always sent in the same order:
Parameter 1: (WER 1 type Ø)



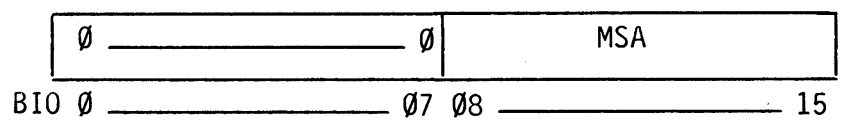
W : Word transfer indicator - if zero the transfer is 8 bit character oriented.
O : Output mode. When 1 the exchange is in output mode from the memory to the Control Unit.
R : Address bits for MADE 6,7 if no 3rd WER (memory not bigger than 256 kbytes).
BL: 12 bit length. Depending on the W indicator value, the block length is expressed either in number of words or in number of characters. If BL=Ø the effective length is 2^{12} words (or bytes).

Parameter 2: (WER 2 type 1)

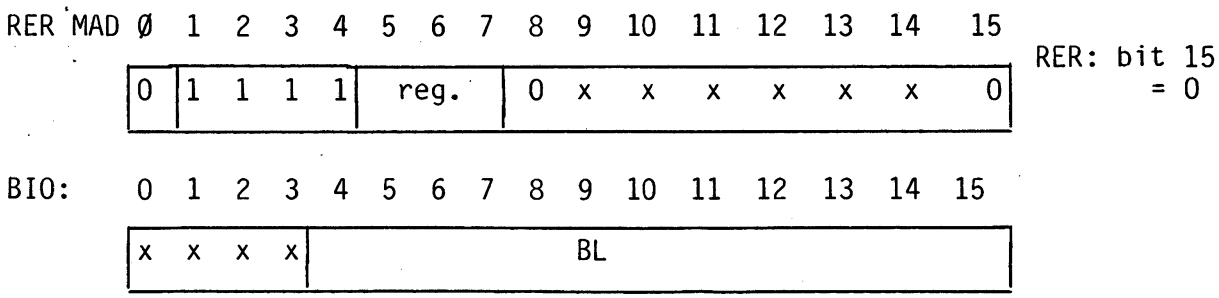


LSA: Least significant bits of the memory start address of the block to be read or written (to MAD Ø-15). A block can start at any byte boundary.

Parameter 3: (WER 3 type 1)



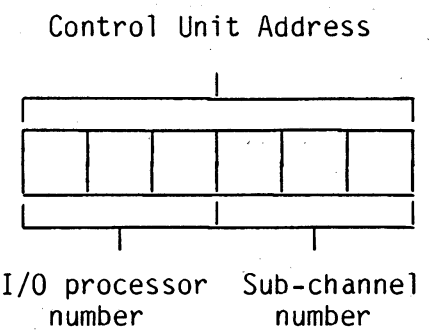
MSA: Most significant bits of the memory start address of the block (to MADE Ø-7). Only necessary if memory bigger than 256K bytes.



The remaining blocklength is sent to the specified register. RER is only allowed when the I/O transfer is finished.

RELATIONSHIP BETWEEN BREAK SIGNAL AND CONTROL UNIT ADDRESS

An I/O processor is coded with a 3-bit number which may range from 0 to 7 (coded by straps on the I/O processor) and each of the 8 subchannels associated with an I/O processor is also coded with a 3-bit number from 0 to 7.
The combined 6-bit number gives the address of the peripheral control unit as shown below:



This address is used by the WER instruction to load the 3 control words into the work register of the I/O processor.

The 8 incoming break request signals BR00 to BR07 to each I/O processor correspond to each subchannel in the I/O processor as follows:

BR00N corresponds to subchannel 0
BR07N corresponds to subchannel 7

BR00N has the highest priority and BR07N lowest.

13 SERIAL CONTROL UNIT P845-140 (SCUZ)

SECTION	13.1	SCUZ IDENTIFICATIONS	PAGE 13-2
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	13.3	V24 INTERFACE	13-6

13.1 SCUZ IDENTIFICATIONS

Type number : P845-140

Function : Asynchronous medium speed Control Unit for V24 or Current Loop interface.

Test program : BZSCU for serial V24 or current loop interface. (VDU, PER 3100)

I/O channel : Program Channel

Power consumption : + 5V, 700 mA
+12V, 40 mA
-12V, 40 mA

12NC code (on sticker) : SCUZ : 5111 199 6855x (5322 216 25125)
X = modification level

Devices :

P816-810	VDU	5111 199 54890
P816-820	VDU, block mode	5111 199 54880
P818-810	VDU	5111 199 54870
P818-820	VDU, block mode	5111 199 54860
P818-851	Keyboard P816/8	
P818-900	PCB for current loop, P816/8	
P842-001	PER 3100	

13.2 FACILITIES

- asynchronous data transfer (start/stop)
- half duplex
- data format 7 or 8 bit
- parity selection
- echo mode selection
- break key detection of peripheral
- data transfer speed 50- 19200 bits/sec.

13.3 INSTALLATION DETAILS

13.3.1 STRAP SETTING

The meaning of the straps (figure 13.1) is as follows:

SB1 = selects number of stop bits (1 or 2).

WL1 = selects number of data bits per character (7 or 8)

BD1 = recognition of a received character while CU is in output mode.

ECHO = selection of echo mode (received characters are transmitted back automatically)

CL1 = selects V24 or current loop interface.

CL2 = when CU is selected for current loop, this strap selects 2 or 4 wires interface.

TCP = test strap (external oscillator).

RCP = test strap (external oscillator).

CT133 = the signal "ready for receive" from the peripheral device can be selected.

ADA = selects the control unit address.

CPT = selects transmission speed (transmitter).

CPR = selects the transmission speed (receiver)

Notes: * Do not select address /10 (ADA) if the card is used in P854 systems.
* If the SCUZ is used in a system with a P876 CPU, this CPU must be strapped for a GPBS Bus application (bus timing delay).

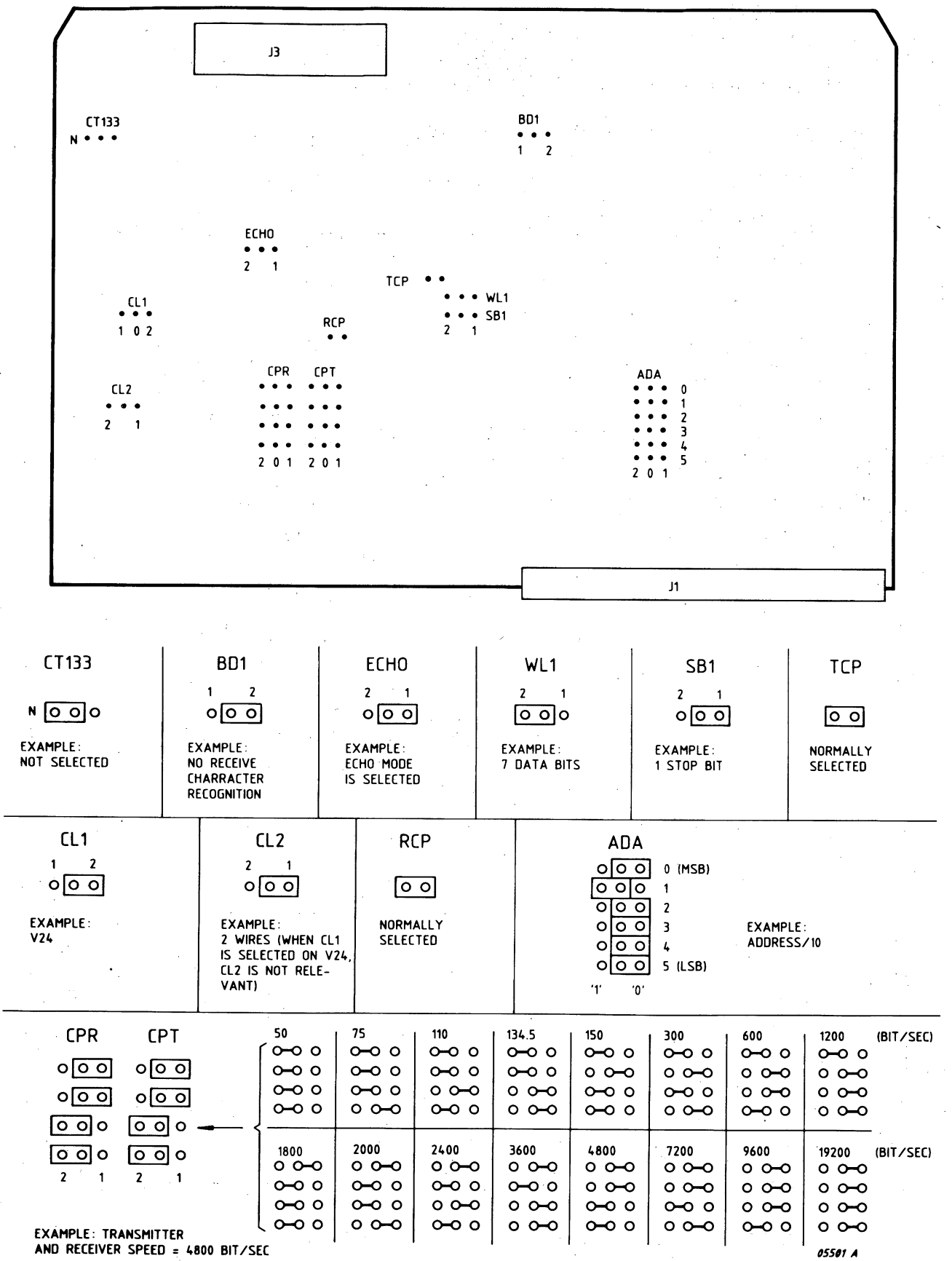


Figure 13.1 STRAP SETTING SCUZ

13.3.2 INTERRUPT WIRING

The following signals must be wired at the back side of the system rack:

- data and status interrupt : pin 1C05 to CPU
- operator panel interrupt (IRIN) : pin 1C04 to CPU
- reset break flip flop (BR1N) : from CPU to pin 1A04

In figure 1.6 is the overview of the interrupt wiring.

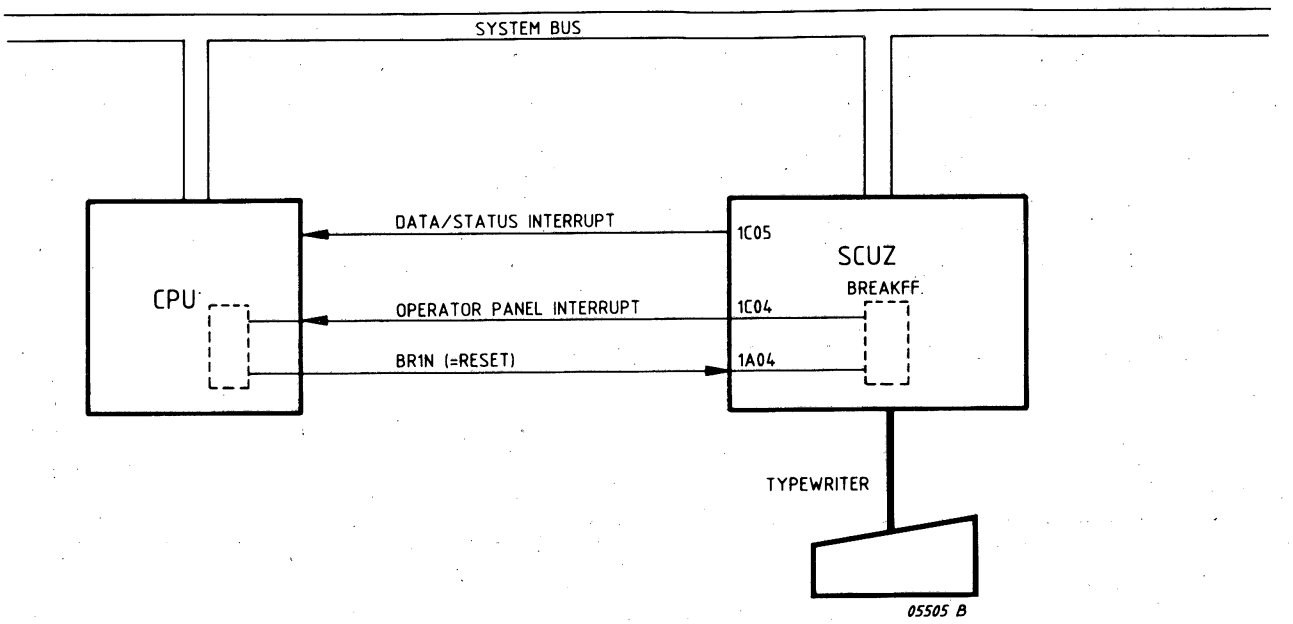


Figure 13.2 INTERRUPT WIRING

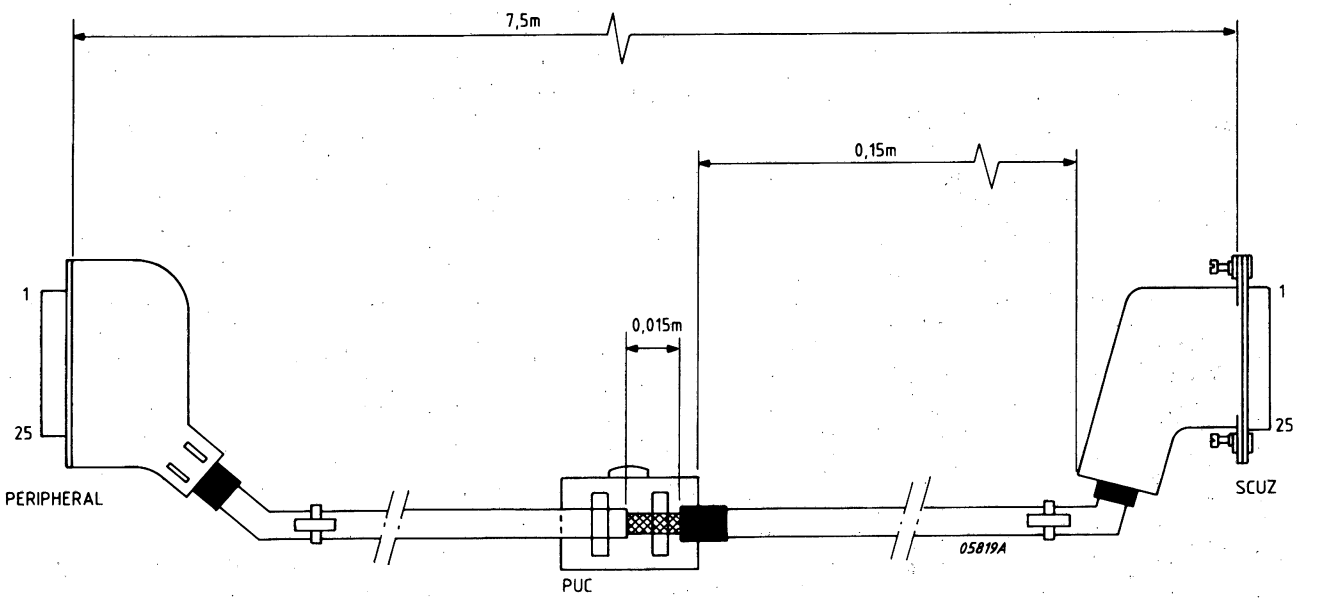


Figure 13.3 CABLE

Signals	SCUZ Connector J3	D8255 Deice Connector Per3100 (P817)	Remarks
Signal Ground	07		Strap
Return (MCLO)	11	11 (14)	Yellow
Received Data (CL1)	12	12 (16)	White
Return (MCL1)	13	13 (13)	Blue
Transmitted Data (CLO)	10	10 (12)	Red
Protective Earth			Connected to Braid

Table 13.1 CURRENT LOOP INTERFACE - 2 WIRE

Signals	SCUZ Connector J3	D8255 Device Connector	Remarks
Ground			Connected to Braid
		08	Strap
		09	
Transmitted Data (CLO)	10	10	Red
Return (MCLO)	11	11	Yellow
Signal Ground (CL1)	07		Strap
Received Data (CL1)	12	12	White
Return (MCL1)	13	13	Blue
		14	Strap
		15	
		03	Strap
		16	

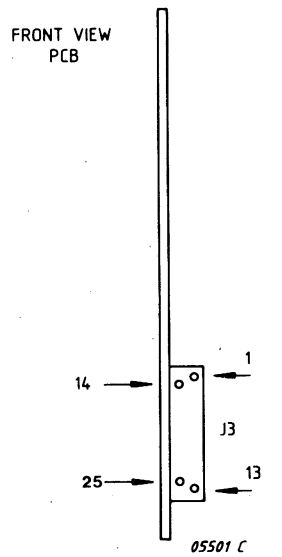


Table 13.2 CURRENT LOOP INTERFACE - 4 WIRE

Signals	SCUZ Connector J3	D8255 Device Connector	Remarks
CT101		01	Braid connected to Ground
CT102	07	07	Signal Earth or Common Return
CT103	02	03	Data SCUZ to Peripheral (Yel)
CT104	03	02	Data Peripheral to SCUZ (BLUE)
CT105		04	Strap
CT106		05	
CT107		06	Strap
CT108/2		20	
CT109		08	Strap
CT133	25	25	Ready for Receiving (White)

Table 13.3 V24 INTERFACE

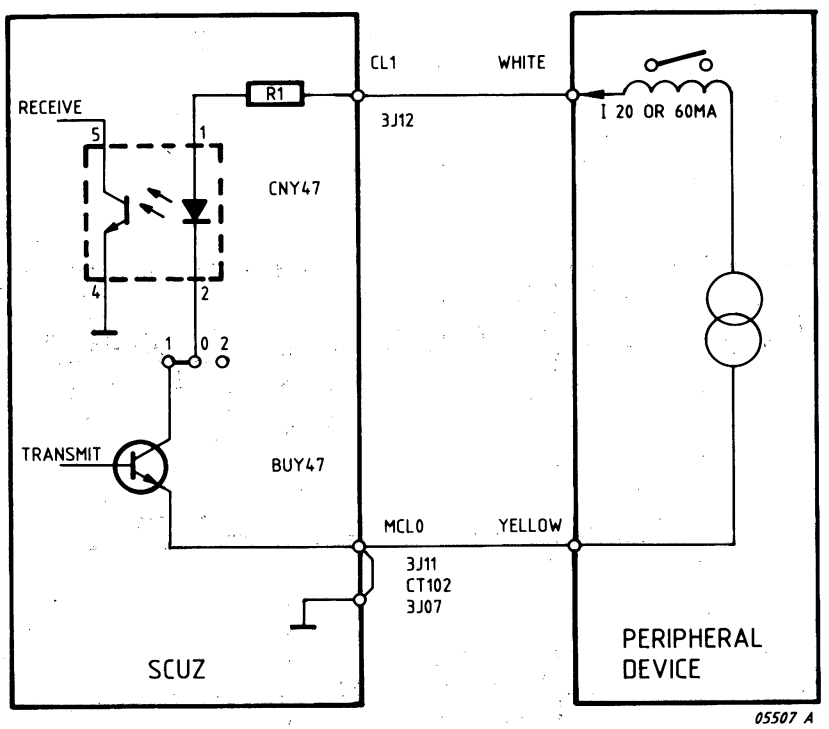


Figure 13.4 CURRENT LOOP- 2 WIRES

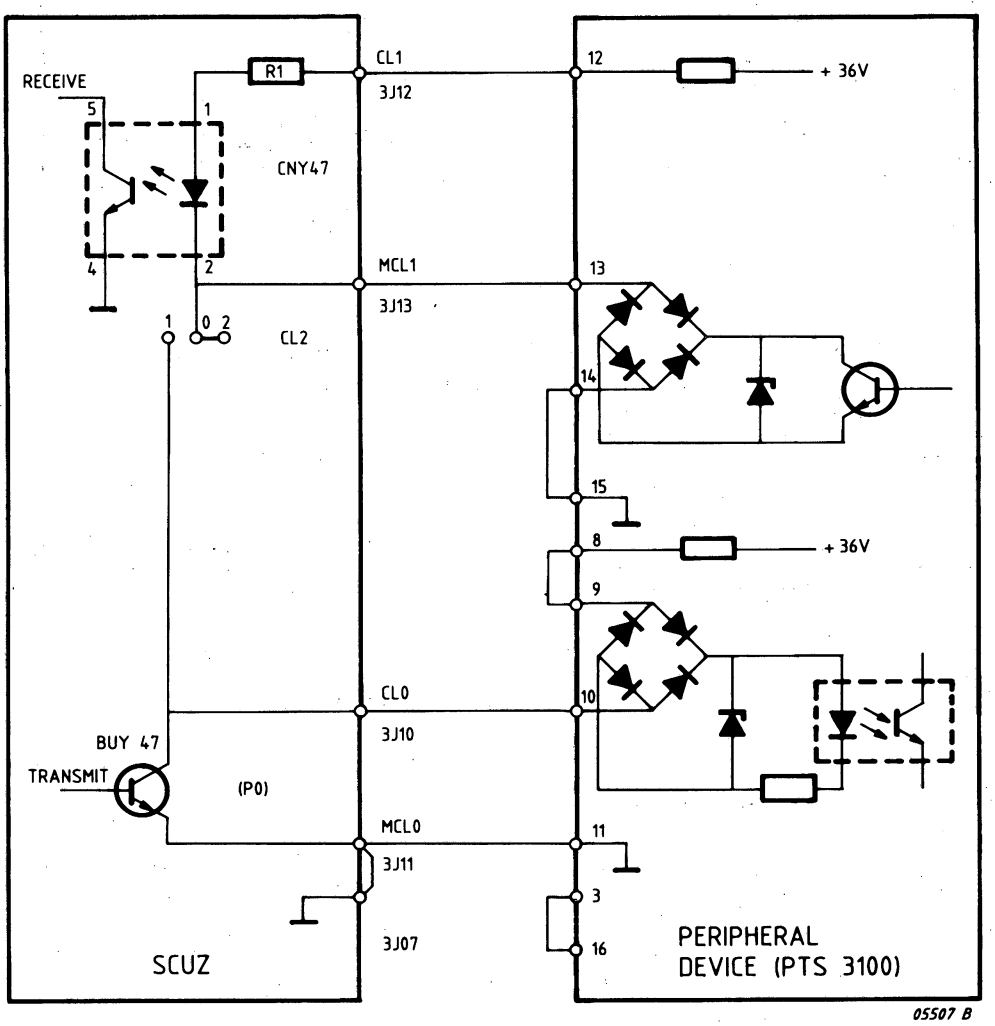


Figure 13.5 CURRENT LOOP - 4 WIRES

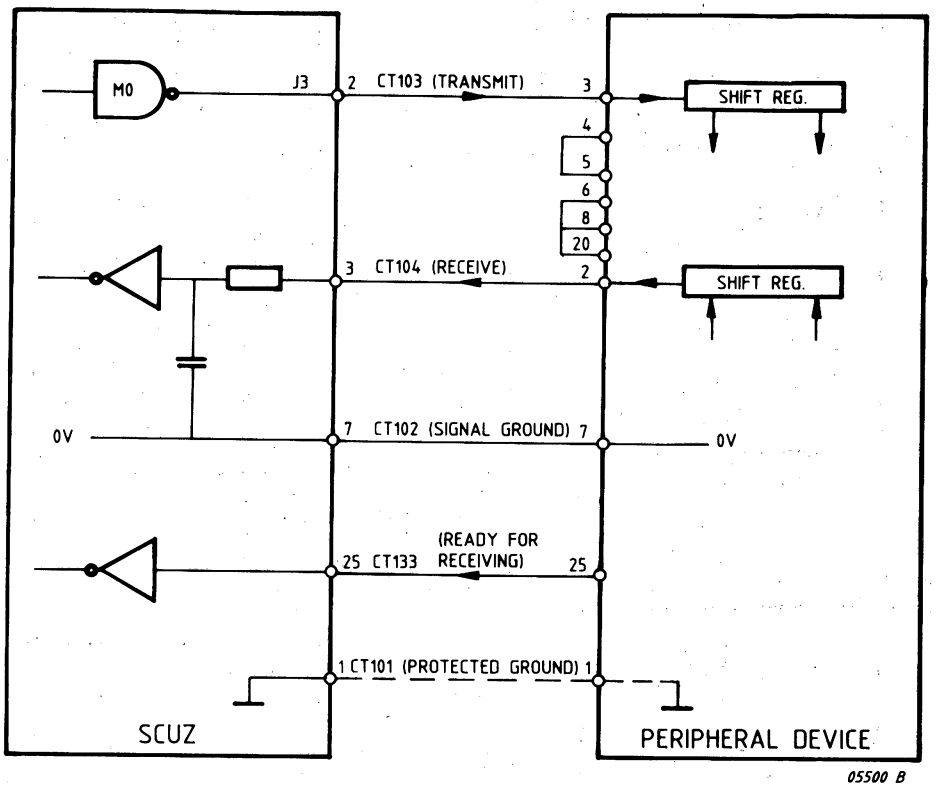


Figure 13.6 V24 INTERFACE

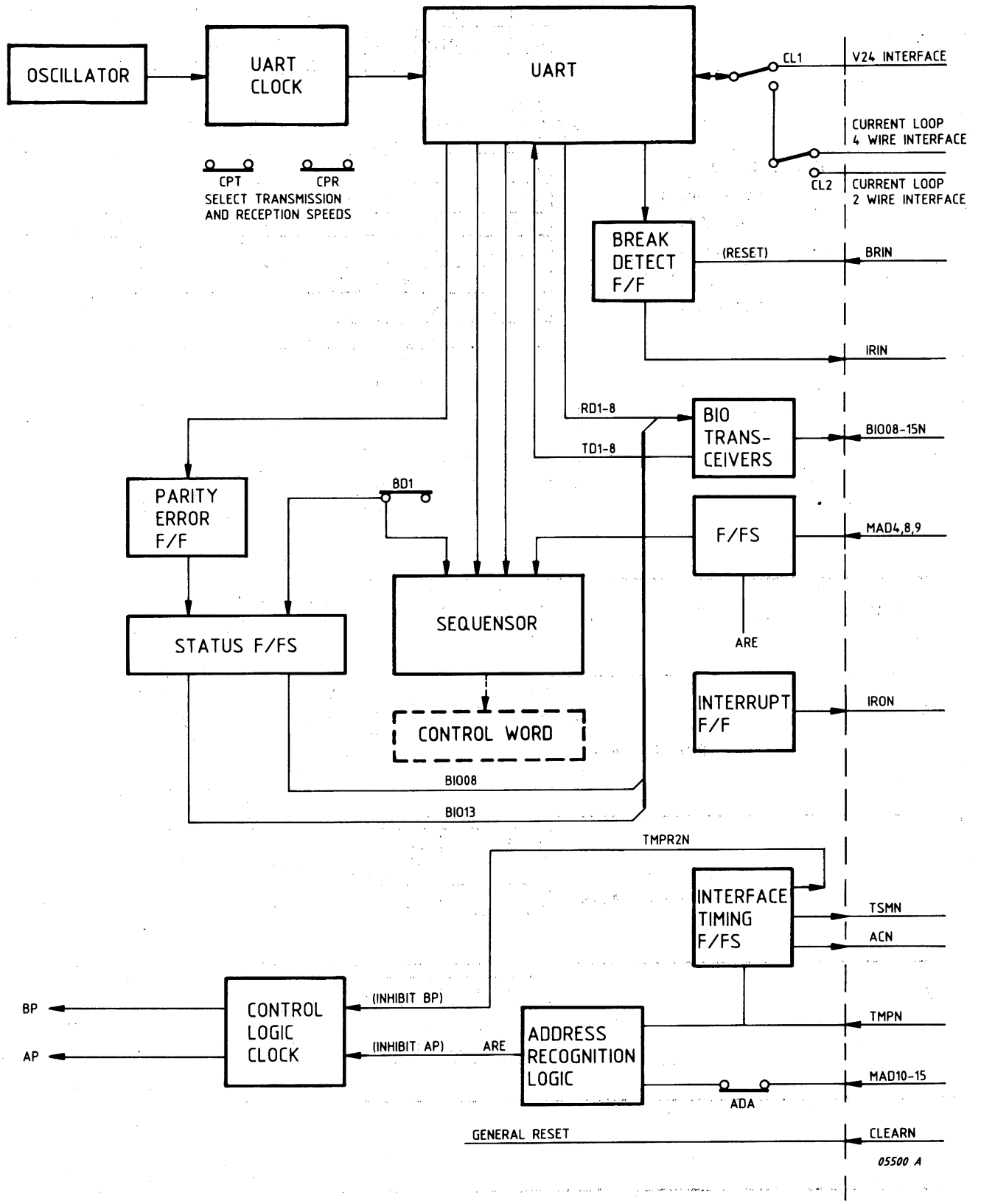


Figure 13.7 BLOCK DIAGRAM SCUZ

13.6 HARDWARE SOFTWARE INTERFACE DETAILS

13.6.1 COMMANDS

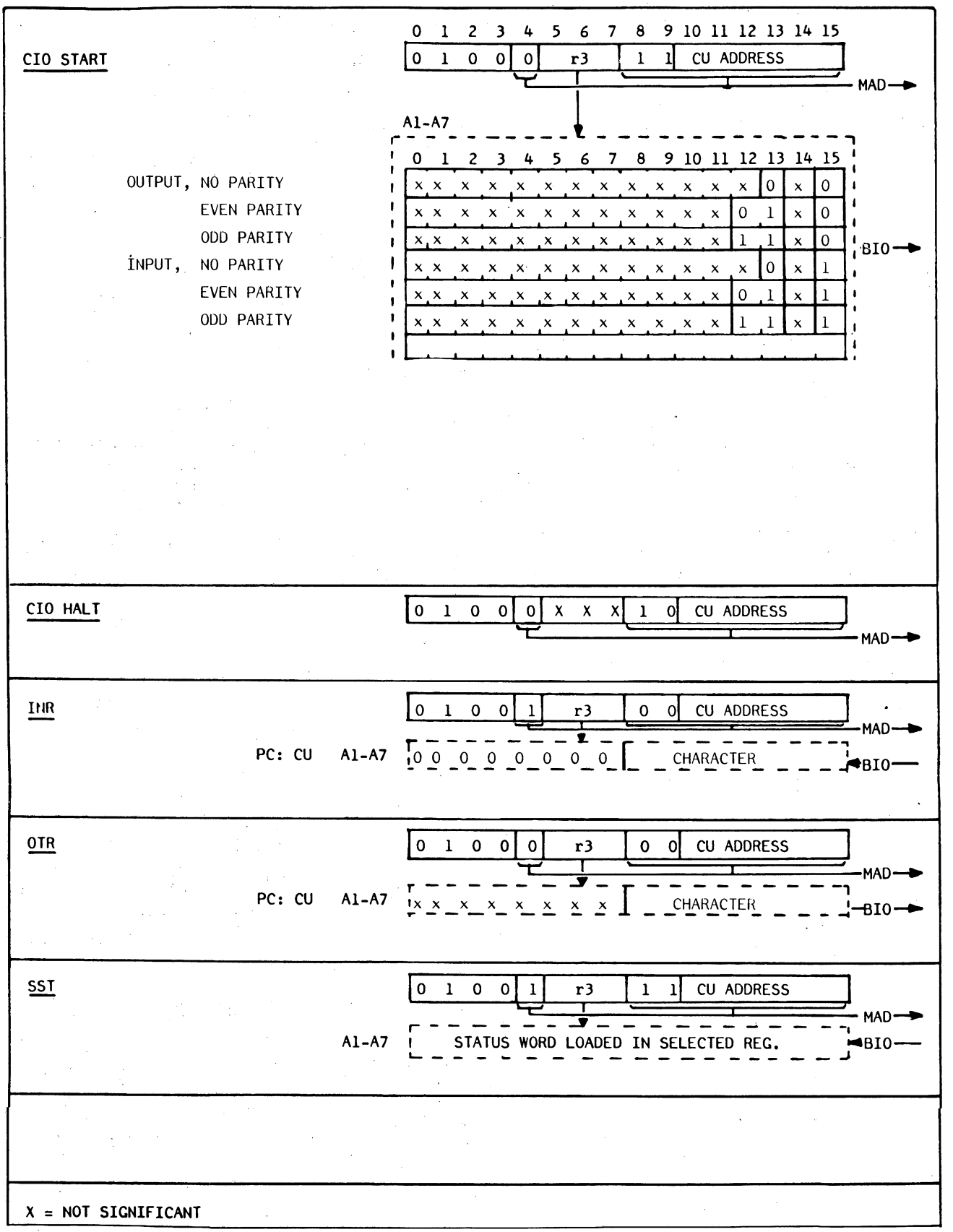


Figure 13.8 HARDWARE SOFTWARE INTERFACE SCUZ

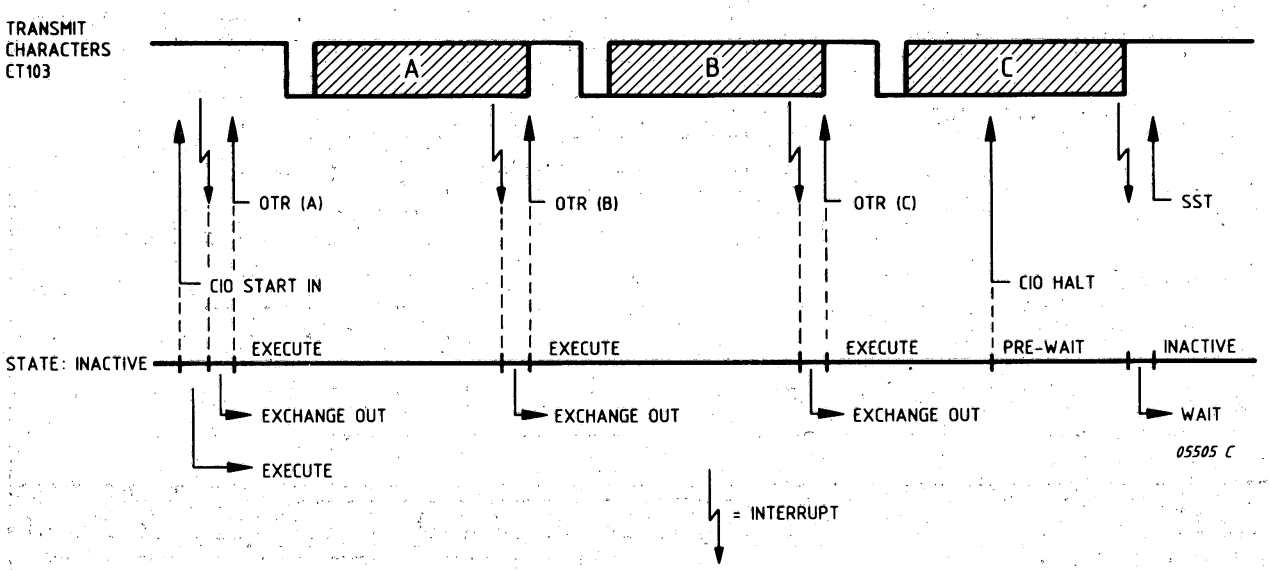
13.6.2 STATUSWORD:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0		0	0	0	0		0	0

Break Detection

parity error

OUTPUT MODE:



INPUT MODE:

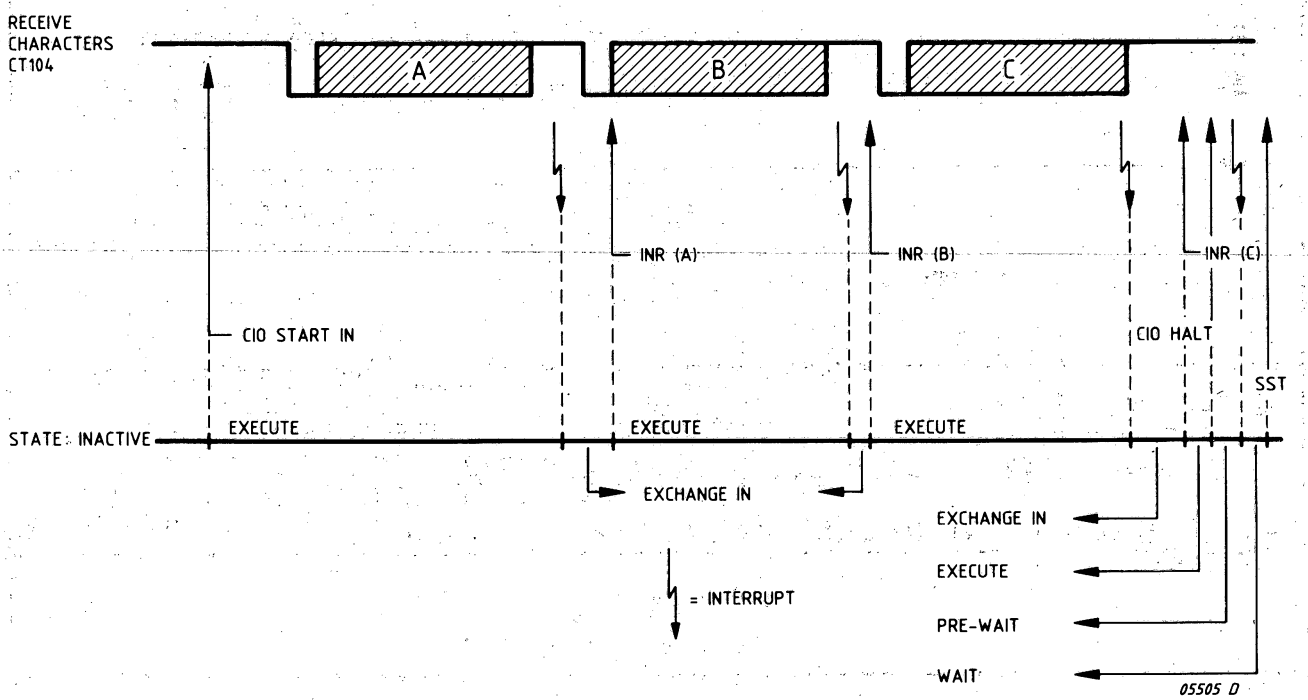


Figure 13.9 COMMAND TIMING

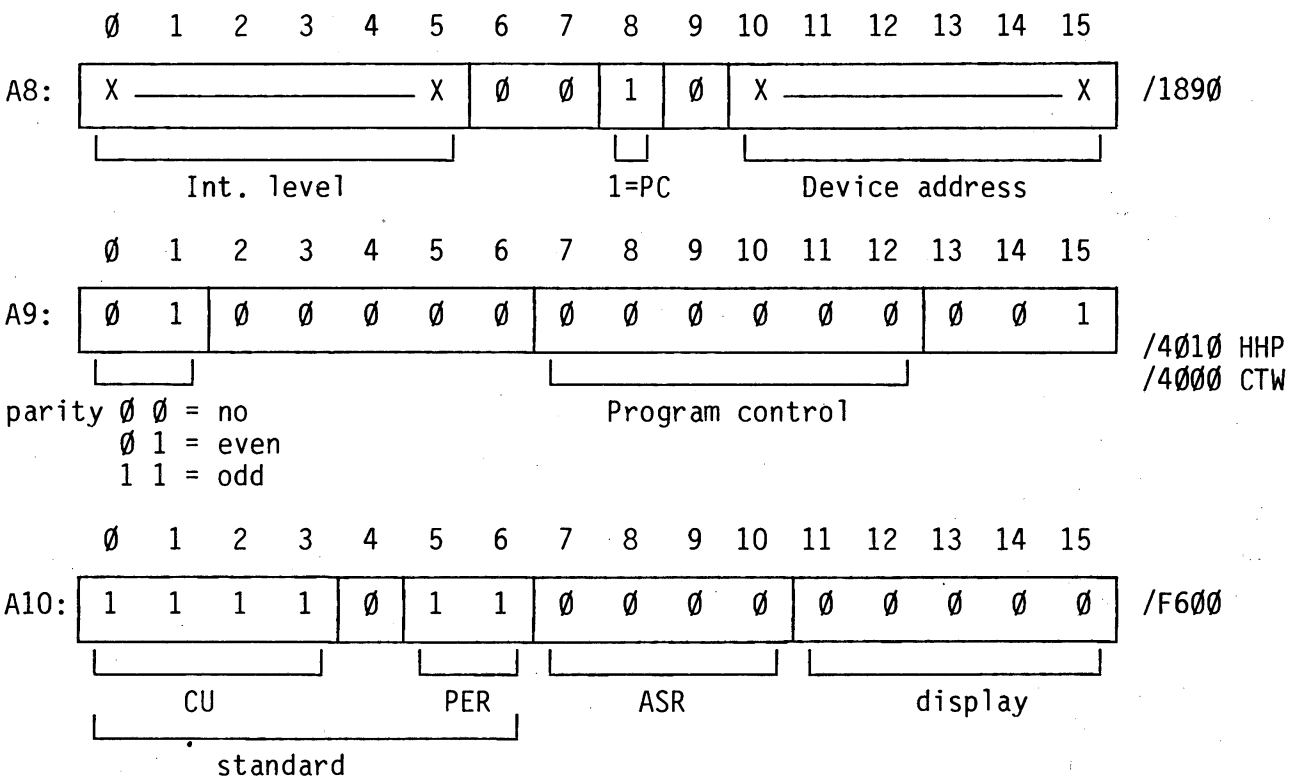
13.7 SHORT DESCRIPTION OF TESTPROGRAMS

TESTPROGRAM BZSCU

CTW: interrupt level 6
dev. address /1Ø not used on P874 (integrated CU = /10).
even parity
Transfer 96ØØ bps max.
RTC, PF/AR allowed.
- Intended for test of SCUZ card from level 5 and on.

Procedure:

- IPL
  RTC on
- Program displays /7ØØ (= restart, normal end of tests. Framing error and interrupt also return to /7ØØ.)
- Change registers



Type in: test 1, char. within 1Ø sec.
3, text, line feed, carr. return, '$' on CTW keyboard.
Error stop at /5FØ
Information stop at /5EØ
If VDU used as CTW for P857E CPU: - Do not use CT133
- Preset A10 with /A7DF (keyboard not tested)
This program may also be used to test the integrated V24-Control Unit of the P874 CPU.

BZSCU tested:

```
If ØØØØ  check Ø  : Output Mode Controller Test
If ØØØ1  check 1  : Input Mode Controller Test
If ØØØ2  check 2  : Inhibit Mode Controller Test
If ØØØ3  check 3  : Echo Mode Test
If ØØØ4  check 4  : Input Mode Parity Test
If ØØØ5  check 5  : PER 31ØØ Printer Function Test (11Ø characters)
If ØØØ6  check 6  : Character Loss Test (11Ø characters)
If ØØØ7  check 7  : ASR "Worst Pattern"
If ØØØ8  check 8  : ASR 75 character per line
If ØØØ9  check 9  : ASR "Dash-pot"
If ØØ10  check 10 : ASR "Punch" and "Reader" Test
If ØØ11  check 11 : Display, all display functions
If ØØ12  check 12 : Display, screen vertically test
If ØØ13  check 13 : Display, screen horizontally test
If ØØ14  check 14 : Display, oblique alignment test
If ØØ15  check 15 : Display, character lost test
```

Procedure	5111 991 1Ø191	= Procedure BZSCU	5111 991 Ø8377
		with addendum PTS8ØØØ	5111 991 11381
Listing	5111 991 1Ø2Ø1		
Program	5111 199 656Ø1		

13.8 SHORT ROUTINES

ASR, PTS 3100 AND DISPLAY

These peripherals and their CU's can be checked with the aid of two small programs called Line, and Echo, if the standard test program either cannot be loaded or if it will not run.

PROGRAM LINE

MEMORY ADDRESS	DATE	PROGRAM INSTRUCTION		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0200		LDK	A2, 0
008A	4BD0		SST	A3,/10
008C	42D0		CIO	A2,1,/10
008E	5C04		RB(NA)	* -2
0090	8520	OUTCR	LDKL	A5,/0A0D
0092	0A0D			
0094	4510	OUT	OTR	A5,0,/10
0096	5C04		RB(NA)	* -2
0098	3D68		SRL	A5,8
009A	5C08		RB(NZ)	OUT
009C	4610	OUTCH	OTR	A6,0,/10
009E	5C04		RB(NA)	* -2
00A0	1201		ADK	A2,1
00A2	EA1C		CWR	A2,A7
00A4	5C0A		RB(NE)	OUTCH
00A6	0200		LDK	A2,0
00A8	5F1A		RB	OUTCR

* Load the ASCII character in register A6
* Load the number of times you wish the character to be repeated into register 7
* Load the start address of the program into register A0 (/0086).
* Push the RUN button

MEMORY ADDRESS	DATA	PROGRAM INSTRUCTIONS		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0221	IN	LDK	A2,/21
008A	42D0		CIO	A2,1,/10
008C	5C04		RB(NA)	* -2
008E	4B10		INR	A3,0,/10
0090	5C04		RB(NA)	* -2
0092	4290		CIO	A2,0,/10
0094	4CD0		SST	A4,/10
0096	5C04		RB(NA)	* -2
0098	0200		LDK	A2,0
009A	42D0		CIO	A2,1,/10
009C	5C04		RB(NA)	* -2
009E	4310		OTR	A3,0,/10
00A0	5C04		RB(NA)	* -2
00A2	4290		CIO	A2,0,/10
00A4	4CD0		SST	A4,/10
00A6	5C04		RB)NA)	* -2
00A8	5F24		RB	IN

Program Echo:

Once loaded and started any input character from the keyboard will be printed, displayed or executed on the device.

14 TRANSLATOR UPL BUS TO GP BUS P843-117 (TUGP)
MAGNETIC TAPE CONTROL UNIT P830-060 (MTCU)

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14.1 TUGP IDENTIFICATIONS

Type numbers : P843-117 5111 199 67690 (5322 216 25527)
P843-117/01 TUGP-OPTION 5111 199 61570:

- Card TUGP 5111 199 67690
- Break Cable IOTZ (3m) 5111 199 71990 *
- Connector (J2) 2412 037 01014
- 8 strap wires, U-links

* Note: Break Cable MT (10m) with PUC: 5111 199 52370

- Testprogram : depending on connected Control Unit (s)
- Channel : depending on connected Control Unit (s)
- Channel : depending on connected Control Unit (s)

- Power Consumption : 5 VL, 1.5A

14.2 INSTALLATIONS DETAILS TUGP

For Installation Details refer to section 14.5:
Installation Details MTCU.

Normally the TUGP should be inserted into the last slot of the Logic Rack:
RA12F - slot 12
RAL22F - slot 23

A chip type SPC16/11 (Interrupt Handler Chip) can be inserted in the empty socket of the TUPG card.
12 NC IHC-chip (SPC 16/11): 5122 011 30760.

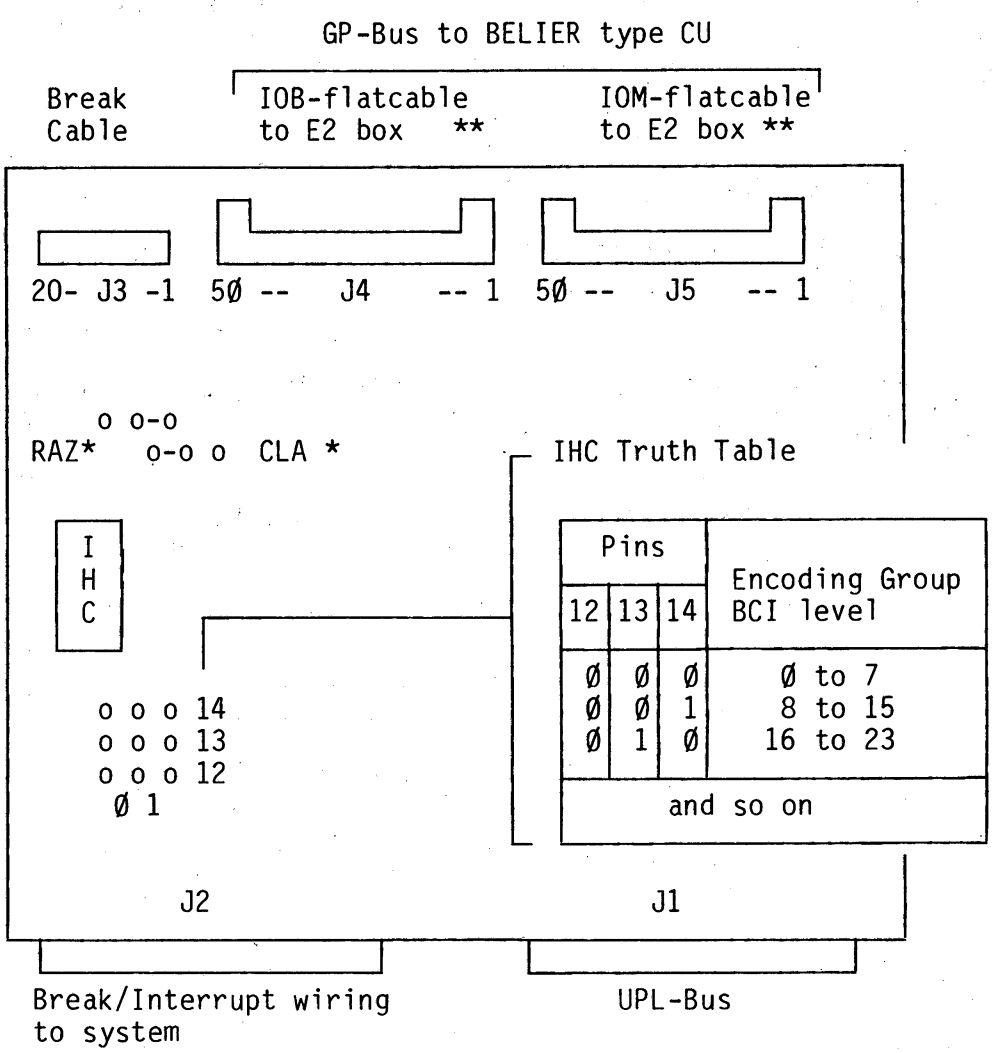
14.2.1 TUGP INTERRUPTS

The interrupt level of MTCU is new encoded:

. either by Interrupt Handler Chip (IHC) on BCI line between 0 and 63 (U-link setting).
. or by a single interrupt wire to the star interrupt system (level 4-31) from an intermediate level between 0 and 7 at the output of TUGP.

Note: as the required interrupt level cannot be selected on the TUGP board, an intermediate level must be used to transport between MTCU and TUGP. (eg. level 7).
Remove IHC chip if not used to avoid double interrupts.

14.2.2 TUGP U-LINK SETTING



* = mandatory position
** = red edge of cable

Figure 14.1 TUGP U-LINK SETTING

14.2.3 TUGP CONNECTIONS

The TUGP card can be mounted on any UPL-compatible backpanel, subject to the following constraint in respect of the length of the RSLN line (if RSLN is used in the extension box).

Power Supply RSLN emitter-follower output to Control Unit RSLN input:
- total length shorter than 5m.

When RSLN is not used by the GP Bus, the maximum permitted length of the GP Bus is 15 m.

INTERCONNECTIONS

Connector J1	UPL Bus
Connector J2	Break Lines and single-interrupt lines (if any) to UPL system
Connector J3	Standard P800 Break cable from extension rack
Connector J4	IOB Flat Cable Connections for GP Bus
Connector J5	IOM Flat Cable Connections for GP Bus

14.3 INTERFACE CONNECTIONS

Break Line

Pin No.	Signal	Function
J1B22	BRON	Break Request Not Lines (Not used - see connector J2)
B23	BR1N	
B24	BR2N	
B25	BR3N	
B27	BR4N	
B28	BR5N	
B29	BR6N	
B30	BR7N	

Table 14.1 TUGP CONNECTOR J1 (UPL-INTERFACE)

BREAK/INTERRUPT LINES TO CPU

Pin No.	Signal	Function
J2C01	IR0N	Interrupt Request Not (Single Interrupt Lines)
C02	IR2N	
C03	IR4N	
C04	IR6N	
C29	BR0N	Break Request Not (Break Request Lines)
C30	BR2N	
C31	BR4N	
C32	BR6N	
J2A01	IR1N	Interrupt Request Not (Single Interrupt Lines)
A02	IR3N	
A03	IR5N	
A04	IR7N	
A29	BR1N	Break Request Not (Break Request Lines)
A30	BR3N	
A31	BR5N	
A32	BR7N	

Table 14.2 TUGP CONNECTOR J2

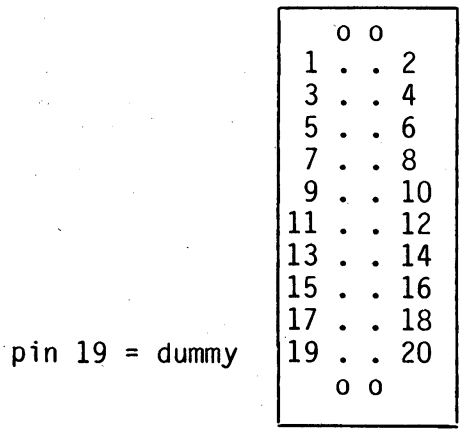
For MTCU, used device address /04, BR04N on pin 2C31 is connected to the IOP. For intermediate interrupt, level 7 on pin 2A04 may be chosen for interconnection to the CPU. U-links on the MTCU must have the same level.

TUGP CABLE CONNECTION TO EQUIPMENT BOX E2.

Pin No.	Signal	Function	Extension Box Pin	Extension Box Colour
J301	BR0N	Break Request Not (Break Request Lines and Screens) and Screens	A	Blanc
02	BR1N		C	Green
03	0V		B	Brown
04	0V		D	Yellow
05	BR2N		E	Grey
06	BR3N		G	Blue
07	0V		F	Rose
08	0V		H	Red
09	BR4N		J	Black
10	BR5N		L	Grey Rose
11	0V		K	Violet
12	0V		M	Blue Red
12	BR6N		N	Blanc Green
14	BR7N		R	Blanc Yellow
15	0V		P	Green Brown
16	0V		S	Yellow Brown
17				
18				
19		dummy		
20				

Table 14.3 TUGP CONNECTOR J3

J3 (contd)



Component side view Connector pinning

TUGP Cable Connection to Equipment Box E2, IOB

Pin No.	Signal	Function	Pin No.	Signal	Function
J401	OV		J426	BIO05N	
02	RSLN	Reset Line Not	27	OV	
03	OV		28	BIO04N	
04	PWFN	Power Failure Not	29	OV	
05	OV		30	BIO03N	Bus Input/
06	BIO15N		31	OV	Output
07	OV		32	BIO02N	Lines and
08	BIO14N		33	OV	Guards
09	OV		34	BIO01N	
10	BIO13N		35	OV	
11	OV		36	BIO00N	
12	BIO12N		37	OV	Interrupt
13	OV		38	BIEC5	Line and Guard
14	BIO11N		39	OV	Scan External
15	OV	Bus Input/Output	40	SCEIN	Int. and Guard
16	BIO10N	Lines and Guards	41	OV	
17	OV		42	BIEC3	
18	BIO09N		43	OV	
19	OV		44	BIEC4	
20	BIO08N		45	OV	Interrupt
21	OV		46	BIEC1	Lines and
22	BIO07N		47	OV	Guards
23	OV		48	BIEC2	
24	BIO06N		49	OV	
25	OV		50	BIEC0	

Max. cable length 14.5m, 12NC 5111 199 7778x (3m) or 5111 199 7777x (5m)

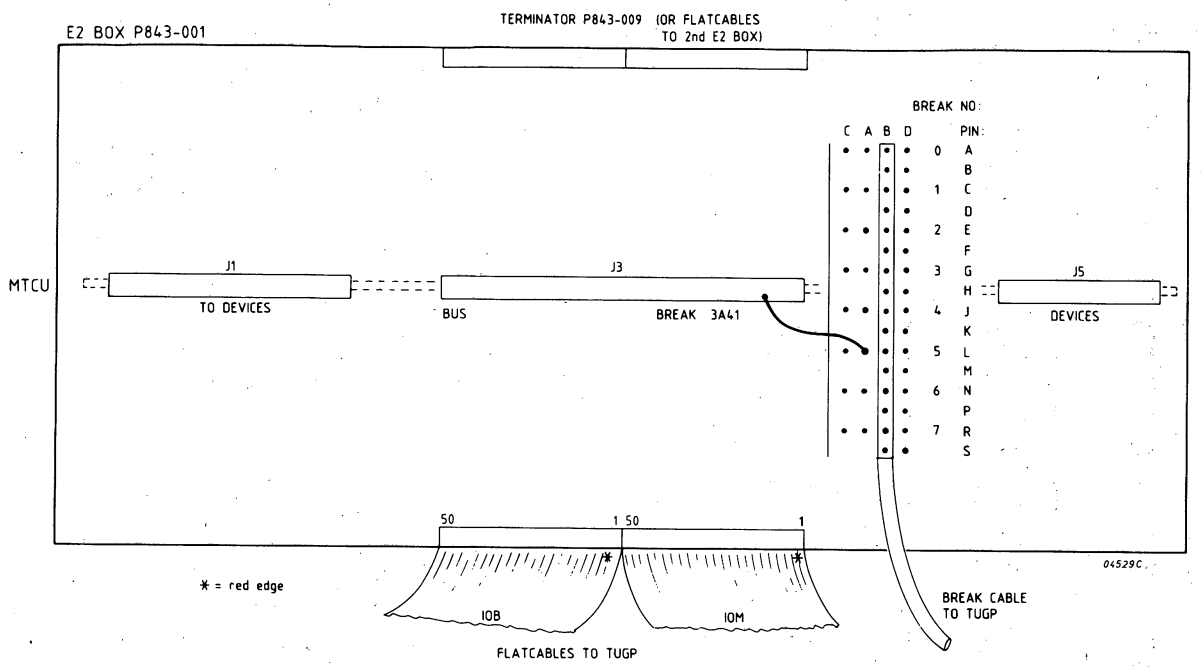
Table 14.4 TUGP CONNECTOR J4-IOB (GP INTERFACE)

TUGP CABLE CONNECTION TO EQUIPMENT BOX E2, IOM

Pin No.	Signal	Function	Pin No.	Signal	Function
J501	OV		J526	OV	
02	MAD04		27	CLEARN	
03	OV		28	OV	
04	MAD03		29	OV	
05	OV		30	TPMN	
06	MAD08		31	OV	
07	OV		32	OV	Control Signals and Guards
08	MAD09		33	TMPN	
09	OV		34	OV	
10	MAD10	Master Address	35	OV	
11	OV	and Guard Lines	36	TMEN	
12	MAD11		37	OV	
13	OV		38	OV	
14	MAD12		39	TRMN	
15	OV		40	OV	
16	MAD13		41	OV	
17	OV		42		
18	MAD14		43	OV	
19	OV		44		
20	MAD15		45	OV	
21	OV		46		
22	ACN	Accept Line and	47	OV	
23	OV	Guard	48		
24	OV		49	OV	
25	OV		50	+5VL	

Max. cable length 14.5m., 12NC 5111 199 7778x (3m) or 5111 199 7777x (5m)

Table 14.5 TUGP CONNECTOR J5-IOM (GP INTERFACE)



Internal connection:
pins row 'C' = 'D'
'A' = 'B'

If a 2nd E2 box is connected, the BREAKcable can be extended with Cable Break Extension (P843-031), by using row 'D'. For the used breaklevels on the 2nd box, interconnections must be made between row 'C' and 'A'.

Cable BREAK EXTENSION, 12 Nc: 5111 199 7767x (5m)

Figure 14.2 EQUIPMENT BOX E2 CONNECTIONS

14.4 MAGNETIC TAPE CONTROL UNIT - IDENTIFICATIONS

Type Number : P831-060 MTCU 5111 199 72460 (5322 216 25214)
Testprogram : BMAGT2
Channel : Hardware Channel (IOP, MIOP, IOPZR)
Break Connection 3A41
Power Consumption: 5 Volt, 2.7 Amp.

Devices : FORMATTER:
P831-030 - F649-60.30.5/1600

DRIVE:
P-831-006 - 6640/9/37.5 ips, PE

P831-006/01 FIRST TAPE DRIVE		
TU 9TR/37,5 IPS/1600 BPI	5111 010 02520	MAGNETIC TAPE 37,5 IPS
	5111 199 71380	ADAPTER MAGNETIC TAPE
	5111 199 81060	CABLE BM PEC
P831-006/11 EXT. TAPE DRIVE		
TU 9TR/37,5 IPS/1600 BPI	5111 010 02520	MAGNETIC TAPE 37,5 IPS
	5111 199 71380	ADAPTER MAGNETIC TAPE
	5111 199 81060	CABLE BM PEC
	5111 011 00850	MTA CABLE 102 200-02
P831-030/21 FORMATTER		
FORMATTER 37,5IPS	5111 010 02530	FORMATTER 37,5 IPS
	5111 199 71390	ADAPTATION FORMATTER
	5111 199 72060	CABLE CU-FORMATTER
	5111 199 81070	CABLE POWER UNIT
	5122 011 00840	TERMINATOR 10202
P831-060/01 MTCU		
CU MTU P831/002/004/006	5111 199 72460	CARD MTCU

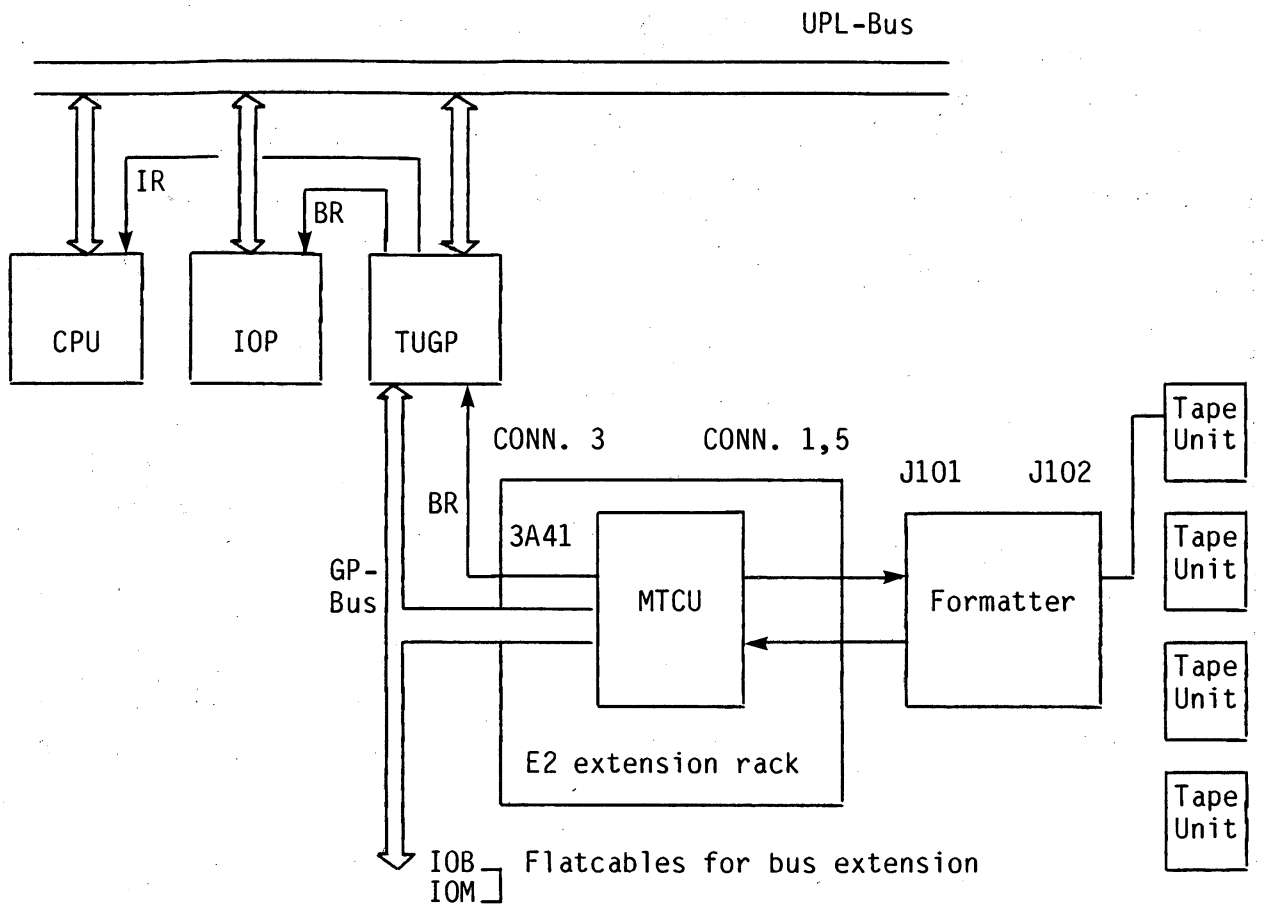


Figure 14.3 MAGNETIC TAPE CONTROL UNIT - SYSTEM CONFIGURATION

Configuration Description

The minimum configuration is:

- A basic cabinet plus Power supply with:
  . UPL CPU
  . Memory
  . IOP
  . TUGP
- An E2 extension cabinet with a Magnetic Tape Control unit.
- Magnetic Tape Peripheral(s) and Formatter.
- GP Bus cables (IOB and IOM), Break cable for E2 rack, GP Bus terminator.

Note: Selection switch, on NRZI- or PE-Write Cards in Formatter, must always be on position "0".

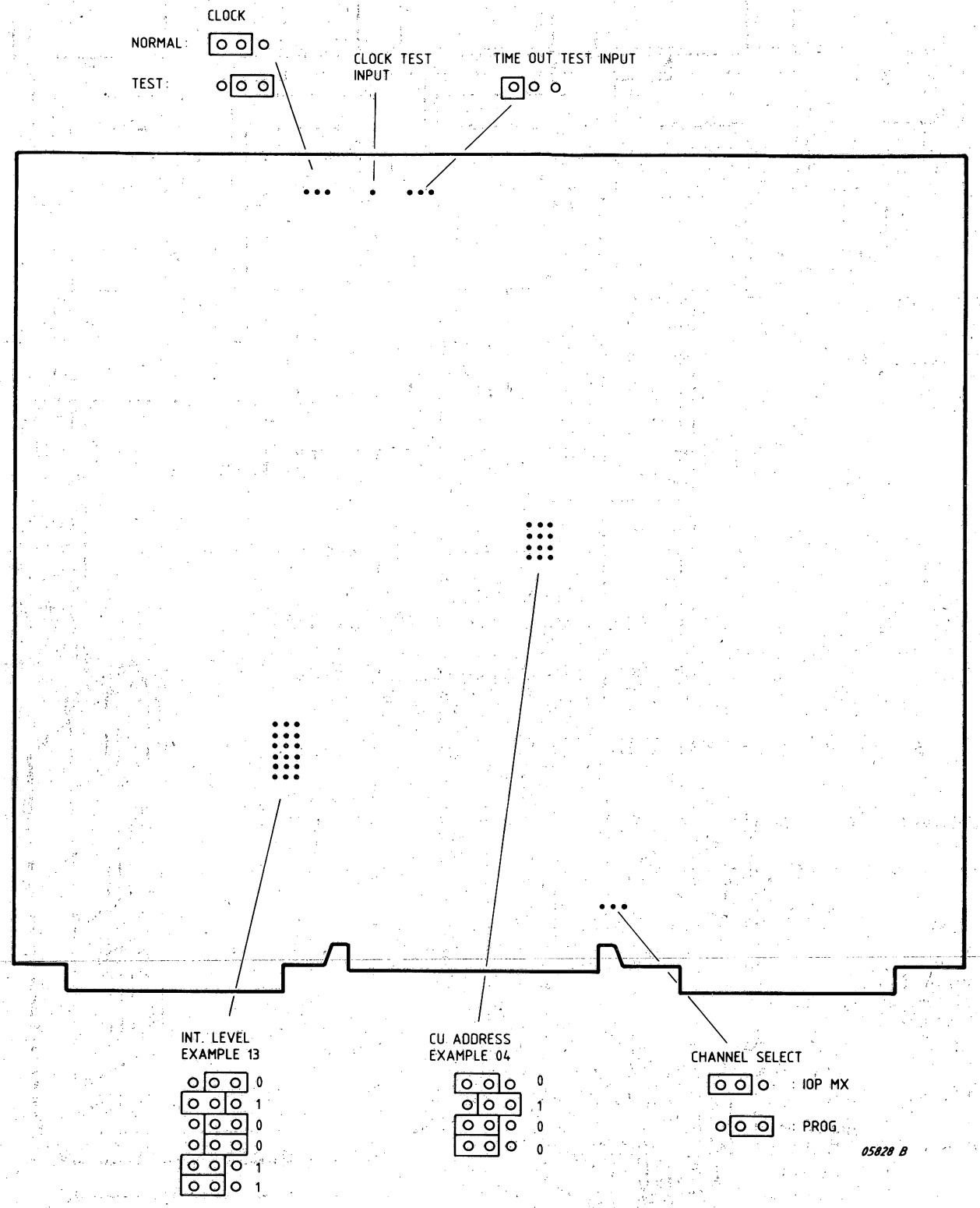


Figure 14.4 CARD LAYOUT MTCU

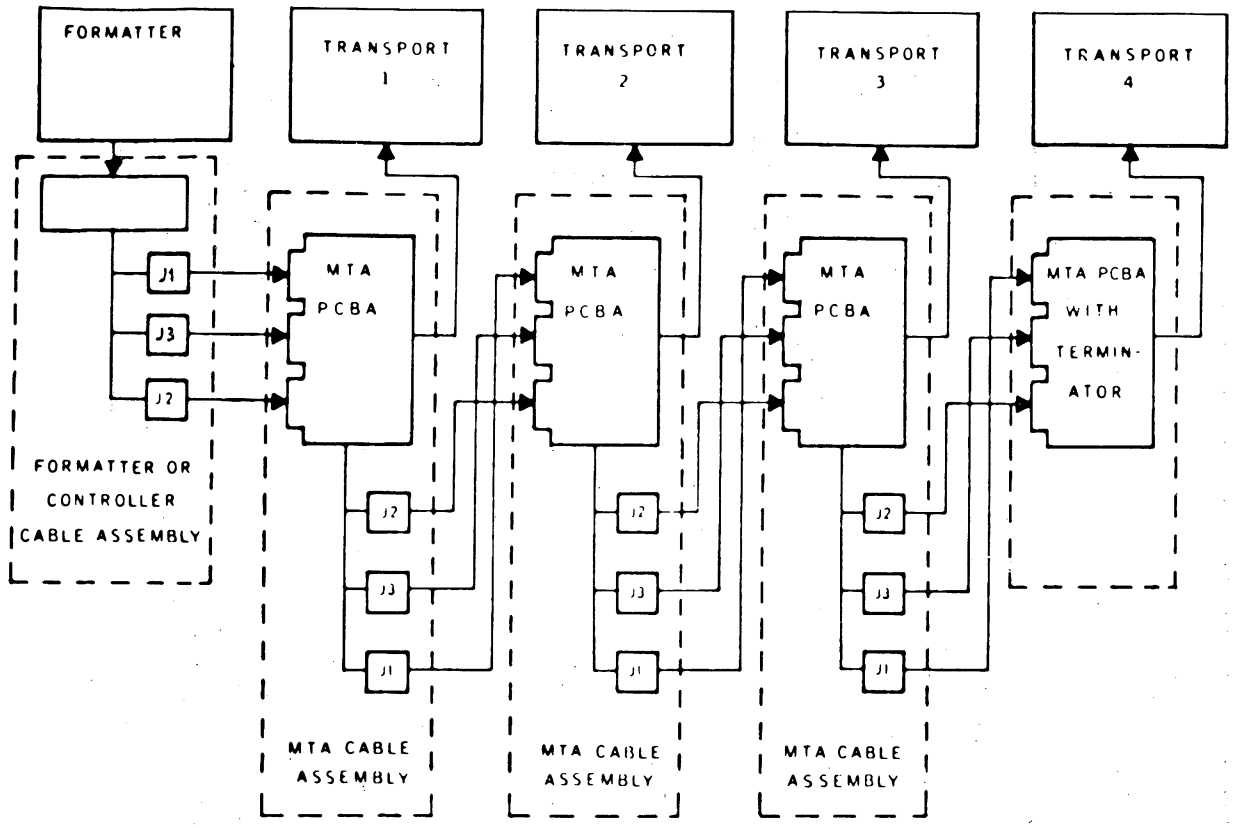


Figure 14.5 MTA SYSTEM DIAGRAM

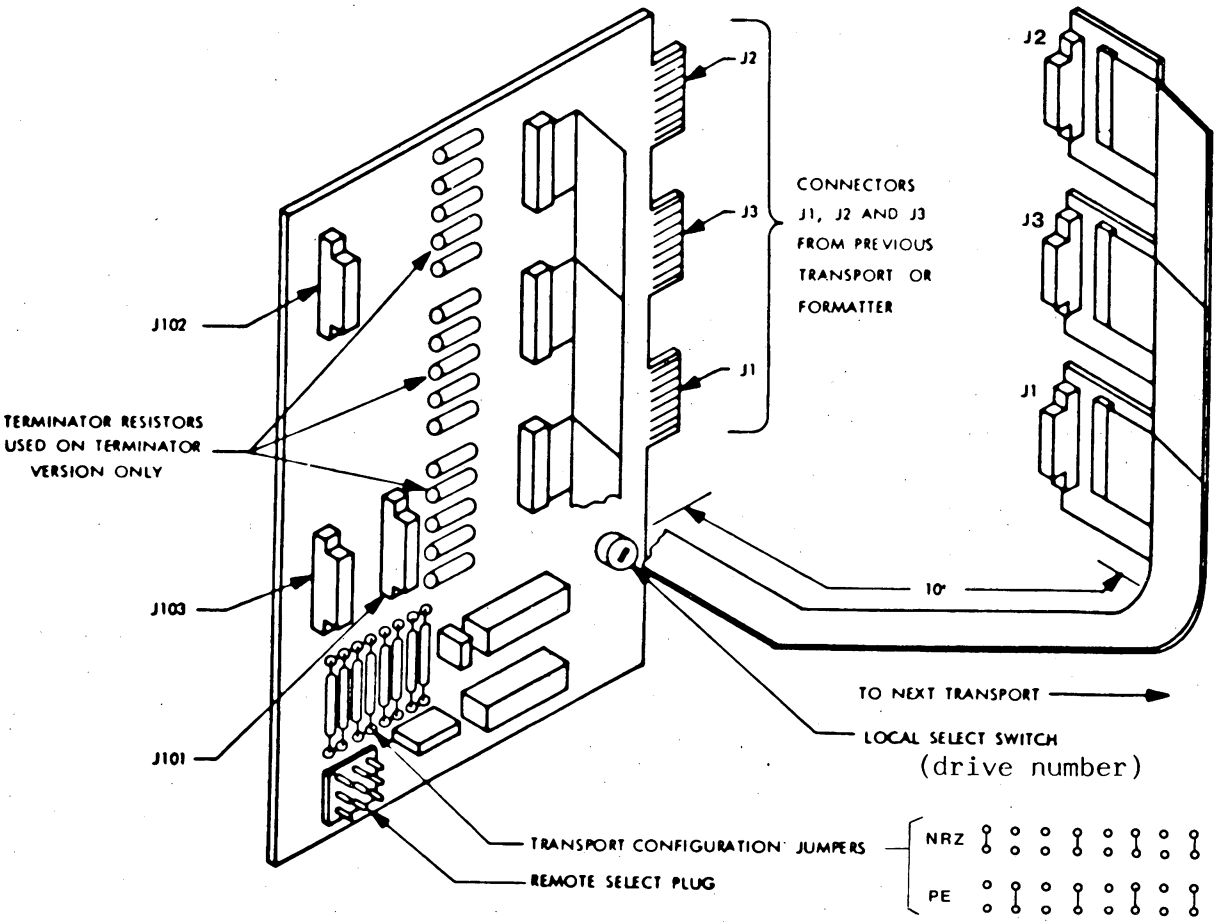


Figure 14.6 MTA CABLE ASSEMBLY

Formatter mating connector: 2VH50 - 1JV5
Controller mating connector

CU Connector 1		Signal	Formatter Card Connector J101		
Live Pin	Ground Pin		Live Pin	Ground Pin	
1301	1B03	IFPTN ←	A28	A29	file protected
A01	A03	IONLN ←	A27	A26	on line
A02	A03	IRDYN ←	B27	B26	ready
B02	B03	INRZN ←	A31	A32	NRZ drive
B04	B05	IFBYN ←	B22	B23	formatter busy
B06	B07	ICERN ←	B25	B26	corrected error (only PE)
B08	B09	IHERN ←	A24	A23	hard error
B10	B11	IFMKN ←	A25	A26	file mark read
B12	B13	IRSTRN ←	B36	B35	read strobe
A05	A04	IDBYN ←	A22	A23	Data busy
NRZ:checkchar!s A07	A06	ICCGIDTN ←	B24	B23	PE: identification burst
A09	A08	IEOTN ←	A30	A29	end of tape
A11	A10	ILDPN ←	B30	B29	load point
A13	A12	IWSTRN ←	A34	A35	write strobe
B25	B26	IGON →	A03	A02	go
A27	A26	ILOLN →	A10	B15	load on line command
B28	B29	IOFLN →	A12	A11	off-line command
A29	A28	IREWN →	B12	B11	rewind command
B30	B31	IERASEN →	B07	B08	erase command
A31	A30	IREVN →	B04	B05	reverse/forwards
B32	B33	IWFMN →	B06	B05	write file mark comm.
A33	A32	IWRTN →	A04	A05	write/read
B34	B35	IPARN →	B10	B11	parity
A35	A34	IDENTN →	A09	A08	write identif. burst
B36	B37	ILWDN →	B13	B14	last word
A37	A36	IFEN →	A13	A14	formatter enable

Table 14.6 DEVICE INTERFACE, CONNECTOR 1

CU Connector 5		Signal	Formatter Card Connector J101		
Live Pin	Ground Pin		Live Pin	Ground Pin	
5A33	5A34	ITAD1N →	B03	B02	transport address
B34	B33	ITAD0N →	A01	A02	
B32	B31	IW7N →	A21	A20	
A31	A32	IW6N →	B21	B20	
B30	B29	IW5N →	A19	A20	
A29	A30	IW4N →	B19	B20	write data lines
B28	B27	IW3N →	A18	A17	
A27	A28	IW2N →	B18	B17	
B26	B25	IW1N →	A16	A17	
A25	A26	IW0N →	B16	B17	
B13	B12	IR8N ←	A36	A35	
A12	A13	IR7N ←	A42	A41	
B11	B10	IR6N ←	B42	B41	
A10	A11	IR5N ←	A40	A41	
B09	B08	IR4N ←	B40	B41	read data lines
A08	A09	IR3N ←	A39	A38	
B07	B06	IR2N ←	B39	B38	
A06	A07	IR1N ←	A37	A38	
B05	B04	IR0N ←	B37	B38	

Table 14.7 DEVICE INTERFACE, CONNECTOR 5

Transport J103 Live	Transport J103 Ret		MTA II J3* Live	MTA II J3* Ret		Formatter J102 Live	Formatter J102 Ret	Signal
1	A	→	1	A	→	B1	B2	READ DATA PARITY (IRDP)
2	B	→	2	B	→	A1	A2	READ DATA STROBE (IRDS)**
3	C	→	3	C	→	B3	B2	READ DATA 0 (IRD0)
4	D	→	4	D	→	A3	A2	READ DATA 1 (IRD1)
8	J	→	8	J	→	A6	A5	READ DATA 2 (IRD2)
9	K	→	9	K	→	B7	A8	READ DATA 3 (IRD3)
10	L	→	10	L	→	A7	A8	NRZI (INRZ)
11	M	→	11	M	→	B9	B8	7-, 9-TRACK (I7TR/I9TR)**
12	N	→	12	N	→	A9	A8	SINGLE (ISGL)
13	P	→	13	P	→	B10	B11	SPEED (ISPD)
14	R	→	14	R	→	A10	A11	READ DATA 4 (IRD4)
15	S	→	15	S	→	B12	B11	READ DATA 5 (IRD5)
17	U	→	17	U	→	B13	B14	READ DATA 6 (IRD6)
18	V	→	18	V	→	A13	A14	READ DATA 7 (IRD7)

Note: The following pins provide +5v and ground from the Formatter to the MTA assemblies.

5	E	←	A48	B48	
6	F	←	A49	B49	
7	H	←	A50	B50	

*Read signals applied to J3 are also applied in parallel to J10 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Relevant to NRZI Operation Only.

Table 14.8 READ SIGNALS, TRANSPORT TO FORMATTER VIA MTA II

Formatter J102 Live	Formatter J102 Ret		MTA II J2 Live	MTA II J2 Ret		Transport J102 Live	Transport J102 Ret	Signal
B15	B14	→	A	1	→	A	1	WRITE DATA STROBE (IWDS)
B16	B17	→	C	3	→	C	3	WRITE AMPLIFIER RESET (IWARS)
B18	B17	→	E	5	→	E	5	READ THRESHOLD 1 (IRTH1)
A18	A17	→	F	6	→	F	6	READ THRESHOLD 2 (IRTH1)
A21	A20	→	L	10	→	L	10	WRITE DATA PARITY (IWDP)
B22	B23	→	M	11	→	M	11	WRITE DATA 0 (IWD0)
A22	A23	→	N	12	→	N	12	WRITE DATA 1 (IWD1)
B24	B23	→	P	13	→	P	13	WRITE DATA 2 (IWD2)
A24	A23	→	R	14	→	R	14	WRITE DATA 3 (IWD3)
B25	B26	→	S	15	→	S	15	WRITE DATA 4 (IWD4)
A25	A26	→	T	16	→	T	16	WRITE DATA 5 (IWD5)
B26	B26	→	U	17	→	U	17	WRITE DATA 6 (IWD6)
A27	A26	→	V	18	→	V	18	WRITE DATA 7 (IWD7)
						J101		
A42	A41	→	B	2	→	J	2	SELECT 1 (ISLT1)**
B43	B44	→	D	4	→	J	16	SELECT 2 (ISLT2)**
A43	A44	→	H	7	→	J	17	SELECT 3 (ISLT3)**

*Write signals applied to J2 are also applied in parallel to J12 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Provided through Select Switch

Table 14.9 WRITE SIGNALS, FORMATTER TO TRANSPORT VIA MTA II

Formatter J102			MTA II J1*			Transport J101		Signal
Live	Ret		Live	Ret		Live	Ret	
A28	A29	→	B	2	→	B	2	OVERWRITE (IOVW)
B30	B29	→	C	3	→	C	3	SYNCHRONOUS FORWARD Command (ISFC)
A30	A29	→	D	4	→	D	4	DATA DENSITY SELECT (IDDS)**
B31	B32	→	E	5	→	E	5	SYNCHRONOUS REVERSE Command (ISRC)
A31	A32	←	F	6	←	F	6	DATA DENSITY INDICATOR (IDDI)*
B33	B32	→	H	7	→	H	7	REWIND Command (IRWC)
B34	B35	→	K	9	→	K	9	SET WRITE STATUS (ISWS)
A34	A35	→	L	10	→	L	10	OFF-LINE Command (IOFC)/REWIND UNLOAD (IRWU)***
B36	B35	←	M	11	←	M	11	ON-LINE (IONL)
A36	A35	←	N	12	←	N	12	REWIND (IRWD)
B37	B38	←	P	13	←	P	13	FILE PROTECT (IFPT)
A37	A38	←	R	14	←	R	14	LOAD POINT (ILDP)
A39	A38	←	T	16	←	T	16	READY (IRDY)
B40	B41	←	U	17	←	U	17	END OF TAPE (IEOT)
B42	B41	→	J	8	→	J	8	SELECT 0 (ISLT0)****

*Control signals applied to J1 are also applied in parallel to J11 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Relevant to NRZI Operation Only.

***REWIND UNLOAD operation applies to T9000 series transports only.

****Provided through Select Switch.

Table 14.10 CONTROL SIGNALS, TRANSPORT/MTA II/FORMATTER

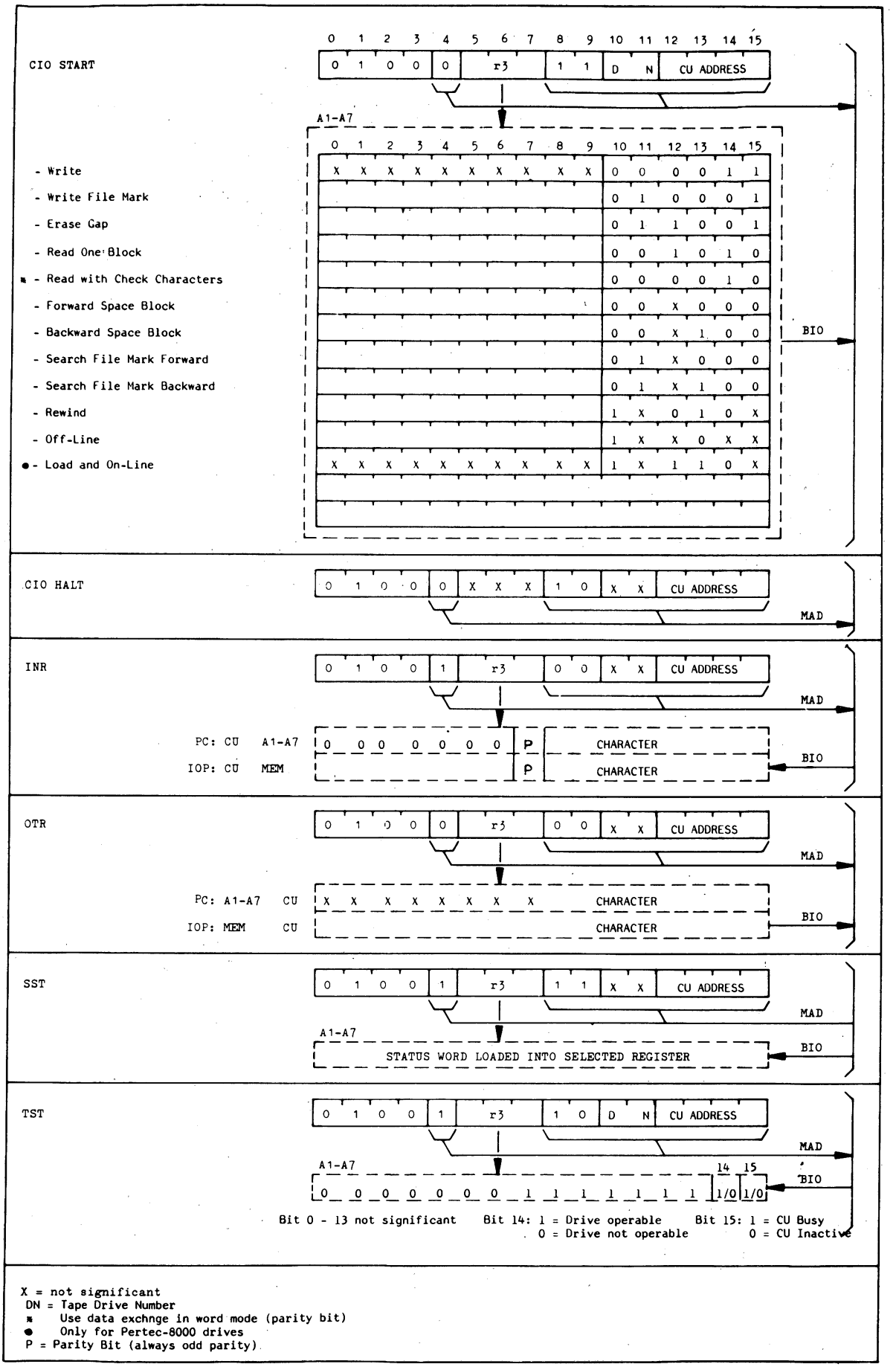
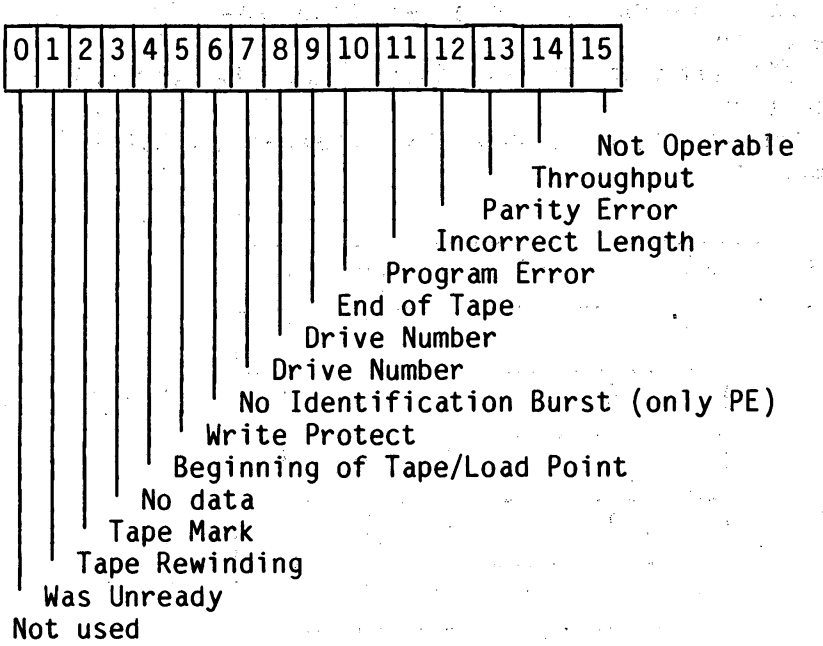


Figure 14.7 INSTRUCTION / COMMAND-WORD FORMATS

14.7.1 STATUS WORD



--15 Not Operable is set if the transport or formatter are not ready to receive a command. Some possible causes of this status are:

- Interlocks are not made
- Initial load is not complete
- The transport is not on line
- The formatter power is off

--14 Throughtput Error is set during Read or Write commands if the channel does not respond to a data request (BR) within the allowed time. The THRF flip-flop (logic f) is set if the data strobe (WSTR/RSTR) for a new character is received from the formatter while the CU is still in Exchange state to transfer the previous character.

--13 Data Fault is set during a Read, Write or Search command if a read error is detected by the formatter for any of the following reasons:

NRZI Mode
- Vertical parity error on data character
- Longitudinal parity error
- CRC parity error (detected during read forward commands only)

PE Mode
- False preamble detection
- False postamble detected
- Buffer overflow
- Multichannel dropout (with WRITE also single channel dropout)
- Parity error without associated channel dropout

--12 The Incorrect Length is set during a Read command with data transfer if the block length on the tape is different from the specified block length.

--11 Program Error

- An INR command is received from the channel during a Write data operation:
- An OTR command is received from the channel during a Read data operation:
- An invalid command code is received on BIO10-15 during a CIO-Start command:

BIOF 10	11	12	13	14	15
0	-	1	1	1	1
0	0	-	-	0	1
0	-	-	1	-	1
0	1	-	-	1	-
0	-	-	1	1	1

INVALID CODES

--10 End of Tape is set if the EOT mark is detected during any CIO-Start command in the forward direction.
If the EOTF is set during a forward Search File Mark command, the HALTF flip-flop is set and the operation stops.

--8,9 Tape Unit Address indicate the current tape transport address.

MAD 10-11 TADF 1-0 Status BIO 8-9	Tape Unit
0 0	0
0 1	1
1 0	2
1 1	3

--7 No Identification Burst is set if the identification burst is not detected during a forward command from the load point on a phase-encoded transport.

--6 File Protected/Write Unable is set whenever the CU receives a Write, Write File Mark or Erase Gap command for a transport that is file protected.

--5 Load Point is set if the transport is at load point when any backward command is received.
(Search or Space backward, Rewind, Load-and-On-Line).

--4 No Data if no data is detected within 20 seconds after sending the command to the transport. Note: No Data, ais also set if blocks are written or read, which are longer than 20 seconds in time.

--3 File Mark is set if a File Mark is detected during any Read, Space, Block or Search File Mark command.

- For NRZI-tapes, if an error is detected in the first character, and this character is followed by one other character only, the CU terminates the operation at the end of the first block, and sets bit 3 (File Mark) and bit 13 (Data Fault).

--2 Tape Rewinding. This status bit is set if the selected tape transport is executing a Rewind command.

--1 Tape was Not Ready is set when the tape transport changes from not-ready state of the completion of a Rewind operation or when an in-operable unit becomes operable.

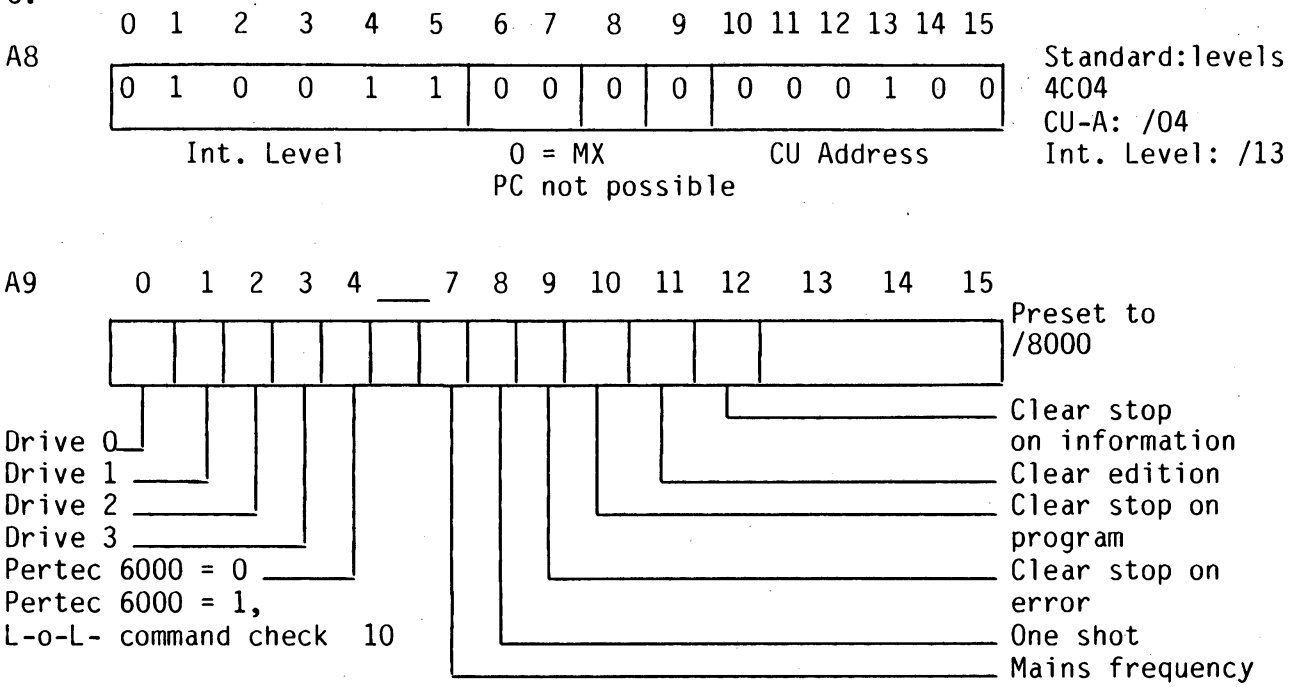
14.8 SHORT DESCRIPTION TESTPROGRAM

TESTPROGRAM BMAGT2 8K

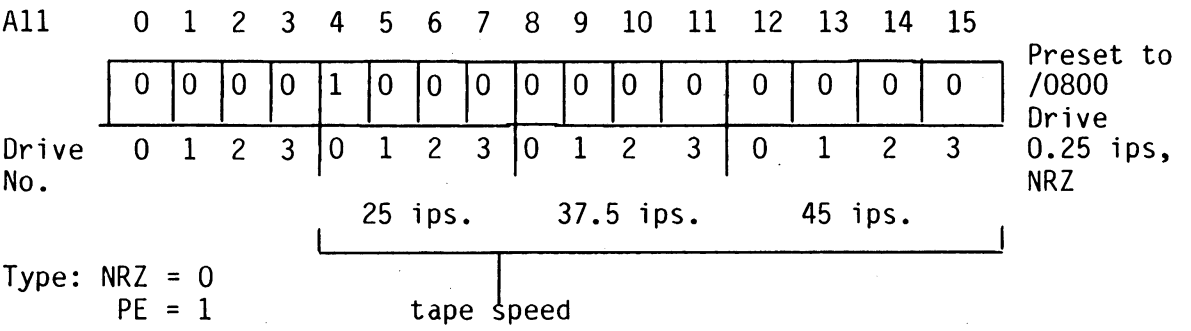
1. IPL
   The program stops at /700 (restart address and normal end).

2. Switch on RTC (PF/AR also possible).

3.



S = Standard setting
. = Optional setting



4. Depress MC, RUN

   Error stop at /5F0
   Restart after power-off at /6EA
   Interrupts return to /700
   Information stop at /5E0

For more information see official description of the testprogram.

BMAGT2 tested:

```
If ØØØØ  check Ø  : Controller Test 1st part
If ØØØ1  check 1  : Controller Test 2nd part
If ØØØ2  check 2  : Status bit test
If ØØØ3  check 3  : Write test with various lengths and patterns
If ØØØ4  check 4  : Reads and controls data written in check 3
If ØØØ5  check 5  : Space block Test
If ØØØ6  check 6  : File Mark (FM) Test
If ØØØ7  check 7  : Erase Function Test
If ØØØ8  check 8  : Status Test with operator action
                    (Write Unable; off line: not operable)
If ØØØ9  check 9  : End of tape test (status bit)
If ØØØA  check A
```

Procedure	5111 991 08655
Listing	5111 991 08667
Program	5111 199 70747

14.9 SHORT ROUTINES

```
         DATE  80-03-13          IDENT    WRITE


00000                            IDENT    WRITE
00001                    *
00002                    *
00003          0000      BEGIN    EQU      *
00004                            RORG     BEGIN+/80
00005                    *
00006                    *
00007                    *       LOAD THE TEST PATTERN IN REGISTER A8
00008                    *
00009                    *       LOAD THE WER PARAMETERS FOR THE WRITE ROUTINE IN REGISTER A7
00010                    *
00011  0080  FFFF                DATA     /FFFF
00012  0082  0000                DATA     0
00013  0084  207F        START   HLT
00014  0086  20BF                INH
00015                    *
00016                    *       THIS ROUTINE LOADS THE OUTPUT BUFFER WITH THE TEST PATTERN
00017                    *
00018  0088  8620                LDKL     A6,WRTBUF              LOAD THE BUFFER ADDRESS IN A6
       008A  00B6  R
00019  008C  80B9        STPAT   STR      A8,A6                  STORE TEST PATTERN
00020  008E  1602                ADK      A6,2                   UPDATE BUFFER ADDRESS AND
00021  0090  EE20                CWK      A6,/121A               COMPARE FOR BUFFER FULL
       0092  121A
00022  0094  5C0A                RB(NE)   STPAT                  IF NOT FULL CONTINUE LOADING
00023                    *
00024                    *       THIS ROUTINE WRITES BLOCKS OF DATA ON TAPE
00025                    *
00026  0096  7708        WRITE1  WER      A7,/8                  SEND WRITE CODE TO IOP
00027  0098  8620                LDKL     A6,WRTBUF              LOAD BUFFER ADDRESS AND
       009A  00B6  R
00028  009C  7609                WER      A6,/9                  SEND TO IOP
00029  009E  0603        WRITE2  LDK      A6,3                   LOAD WRITE A BLOCK COMMAND
00030  00A0  46C4                CIO      A6,1,/4                AND SEND TO MAG TAPE "1"
00031  00A2  5C04                RB(NA)   *-2
00032  00A4  4CC4                SST      A4,/4                  GET STATUS AFTER TRANSFER
00033  00A6  5C04                RB(NA)   *-2
00034  00A8  A420                ANKL     A4,/7F3F               SAVE BITS SET
       00AA  7F3F
00035  00AC  EC20                CWK      A4,0                   AND CHECK FOR ANY BITS SET
       00AE  0000
00036  00B0  5002                RF(E)    *+4                    IF NO CONTINUE
00037  00B2  207F                HLT                             IF YES HALT STATUS IN A4
00038  00B4  5F20                RB       WRITE1
00039                    *
00040  00B6              WRTBUF  RES      2050                   WRITE BUFFER
00041                            END      START
```

```
          DATE  80-03-13        IDENT    READ

00000                           IDENT    READ
00001                     *
00002                     *       THIS PROGRAM READS BLOCKS OF DATA FROM TAPE
00003                     *       AND THEN CHECKS IT AGAINST THE EXPECTED PATTERN
00004                     *
00005          C000       BEGIN   EQU      *
00006                             RORG     BEGIN+/80
00007                     *
00008                     *
00009                     *       LOAD THE EXPECTED PATTERN IN REGISTER A10
00010                     *
00011                     *
00012                     *       LOAD THE NUMBER OF CHARACTERS PER BLOCK IN REGISTER A8
00013                     *
00014                     *
00015                     *       LOAD THE WER PARAMETERS FOR A READ COMMAND IN REGISTER A7
00016                     *
00017                     *
00018  0080  FFFF                 DATA     /FFFF
00019  0082  0000                 DATA     0
00020  0084  207F       START     HLT
00021  0086  20BF                 INH
00022                     *
00023                     *       THIS ROUTINE READS A BLOCK OF DATA FROM TAPE
00024                     *
00025  0088  7708       READ      WER      A7,/8                 SEND READ PARAMETERS TO THE IOP
00026  008A  8620                 LDKL     A6,RDBUF              LOAD BUFFER ADDRESS
       008C  00C6  R
00027  008E  7609                 WER      A6,/9                 AND SEND TO IOP
00028  0090  060A                 LDK      A6,/A                 LOAD READ A BLOCK COMMAND
00029  0092  46C4                 CIO      A6,1,/4               AND SEND TO MAG TAPE UNIT
00030  0094  5C04                 RB(NA)   *-2
00031  0096  4CC4                 SST      A4,/4                 GET STATUS WHEN BLOCK READ
00032  0098  5C04                 RB(NA)   *-2
00033  009A  A420                 ANKL     A4,/7F3F
       009C  7F3F
00034  009E  EC20                 CWK      A4,0                  AND CHECK FOR ANY STATUS BITS SET
       00A0  0000
00035  00A2  500A                 RF(E)    *+12                  IF NO CONTINUE
00036  00A4  7E08                 RER      A6,/8                 CHECK IF ALL THE BLOCK HAS BEEN READ
00037  00A6  EE20                 CWK      A6,0
       00A8  0000
00038  00AA  5002                 RF(E)    *+4                   IF YES CONTINUE
00039  00AC  207F                 HLT                            IF NO HALT STATUS IN A4
00040                     *
00041                     *       THIS ROUTINE COMPARES DATA READ WITH DATA WRITTEN
00042                     *
00043  00AE  81A0                 LDKL     A9,RDBUF              LOAD ADDRESS OF READ BUFFER
       00B0  00C6  R
00044  00B2  8502                 LDR      A5,A8                 GET BLOCK LENGTH FROM A8
00045  00B4  EAA6       COMP1     CWR*     A10,A9                COMPARE DATA READ WITH DATA EXPECTED
00046  00B6  5002                 RF(E)    *+4                   IF EQUAL CONTINUE
00047  00B8  207F                 HLT                            IF NOT HALT
00048  00BA  91A0                 ADKL     A9,2                  UPDATE ADDRESS IN A9
       00BC  0002
00049  00BE  9D20                 SUKL     A5,2                  DECREMENT BLOCK LENGHT COUNTER
       00C0  0002
00050  00C2  5C10                 RB(NZ)   COMP1                 IF NOT ZERO DO ANOTHER COMPARE
00051  00C4  5F3E                 RB       READ                  READ NEXT BLOCK
00052                     *
00053  00C6              RDBUF     RES      2050                  READ BUFFER
00054                             END      START
```

```
          DATE  80-03-13        IDENT    MTTEST    ON PROGRAMMED CHANNEL

00000                           IDENT    MTTEST                ON PROGRAMMED CHANNEL
00001                    *TEST FOR ALL TAPEDRIVES
00002
00003                    *REPLACE HLTS AS FOLLOWS AND THE PROGRAM WIL
00004                    *WRITE DO BACKSPACE AND READ THE SAME BLOCK
00005                    *        HLT      ON ADDR. /009E        BY/0104
00006                    *        HLT      ON ADDR. /00A8        BY/5700
00007
00008                    *FOR RUNNING IN LOOP REPLACE ALSO
00009                    *        HLT      ON ADDR. /00CE        BY/5700
00010
00011
00012                    *WRITE TEST
00013                             AORG     /80
00014  0080  FFFF                DATA     /FFFF
00015  0082  0000                DATA     0
00016  0084  20BF       START    INH
00017  0086  8320                LDKL     A3,/FF                NUMBER OF CHARACTERS 256
       0088  00FF
00018  008A  02FF                LDK      A2,/FF                CHAR. ALL ONES
00019  008C  0103                LDK      A1,3                  WRITE COMMAND
00020  008E  41C4                CIO      A1,1,4                START CONTR. DRIVE 0
00021  0090  4204                OTR      A2,0,4                WRITE CHAR.
00022  0092  5C04                RB(4)    *-2
00023  0094  1B01                SUK      A3,1                  UPD. CHAR COUNTER
00024  0096  5C08                RB(4)    *-6                   NEXT OTR
00025  0098  4184                CIO      A1,0,4                STOP CONTROLLER
00026  009A  4CC4                SST      A4,4                  STATUS TO A4
00027  009C  5C04                RB(4)    *-2
00028  009E  207F                HLT                            STATUS IN A4
00029
00030                    *TAPE COMMANDS ROUTINE;
00031
00032                    *LOAD REGISTER A1 WITH:
00033                    *        REWIND   /0024
00034                    *        ERASE    /0019
00035                    *        WFM      /0011
00036                    *        FWD SPACE                      /0000
00037                    *        BWD SPACE                      /0004
00038                    *        SFM FWD  /0010
00039                    *        SFM BWD  /0014
00040                    *        OFF LINE /0020
00041
00042  00A0  20BF       TCR      INH
00043  00A2  41C4                CIO      A1,1,4                START FOR DRIVE 0
00044  00A4  4CC4                SST      A4,4                  STATUS TO A4
00045  00A6  5C04                RB(4)    *-2
00046  00A8  207F                HLT                            STATUS IN A4
00047
00048
00049                    *READ TEST  ONLY TO EXECUTE AFTER WRITE TEST
00050
00051  00AA  20BF       RT       INH
00052  00AC  0300                LDK      A3,0                  RESET CHARACTER COUNTER
00053  00AE  0500                LDK      A5,0                  RESET READ REGISTER
00054  00B0  8220                LDKL     A2,/1FF               EXPECTED CHAR WITH PARITY
       00B2  01FF
00055  00B4  010A                LDK      A1,/A                 READ COMMAND
00056  00B6  41C4                CIO      A1,1,4                START CONTR DRIVE 0
00057  00B8  4D04       INR      INR      A5,0,4                READ CHAR
00058  00BA  5C04                RB(4)    *-2
00059  00BC  ED08                CWR      A5,A2                 CHARACTER SAME?
00060  00BE  5412                RF(4)    DATAF                 NO GO TO FAULT
00061  00C0  1301                ADK      A3,1                  INCREMENT CHARACTER COUNTER
00062  00C2  EB20                CWK      A3,/FF                ARE THERE 256 ALREADY?
       00C4  00FF
00063  00C6  5C10                RB(4)    INR                   NEXT CHAR.
00064  00C8  4184                CIO      A1,0,4                STOP CONTROLLER
00065  00CA  4CC4       SST      SST      A4,4                  STATUS TO A4
00066  00CC  5C04                RB(4)    *-2
00067  00CE  207F                HLT                            STATUS IN A4
00068  00D0  5F4E                RB       START                 TO WRITE TEST
00069  00D2  207F       DATAF    HLT                            RECEIVED CHAR IN A5,
00070                                                           EXPECTED IN A2, FOR STATUS PUSH RUN
00071  00D4  5F0C                RB       SST
00072
00073
00074                    *IF PROGRAM LOOPS ON INR; LESS CHARACTERS IN THE BLOCK THAN EXPECTED
00075                    *NUMBER OF CHARACTERS IN A3
00076
00077                             END      START
```

16 FLEXIBLE DISC CONTROL UNIT P830-150 (F1MZA)

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	16.3	INSTALLATION DETAILS	16-4
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16.1 FLEXIBLE DISC CONTROL UNIT (F1MZA) - IDENTIFICATIONS

Type Number : P830-150 (F1MZA)
Testprogram : BF1MZ
Channel : IOP/MIOP only. Break connection: 1A05, Interrupt: 1C05

Power Consumption: +5 Volt, 2 Amp.

12NC code on the sticker on the board: FIMZA-5111 199 58690 (5322 216 21286)

F1MZ- 5111 199 6752x (5322 216 25612) can also be used (older version of F1MZA)

X = modification level.

Devices : CDC 9406 (max.2) or CDC 9404 (max 4), with doorlock option see chapter 3, FLOPPY RACK or RACK RAWIST.

Cables : Cable Floppy (2 drives) - 5111 199 71030
Cable Floppy (4 drives) - 5111 199 71020

Discettes(1M) : Set of 10 Discettes - 8709 001 10503
Discettes($\frac{1}{4}$M) : Set of 10 Discettes - 8709 001 10203

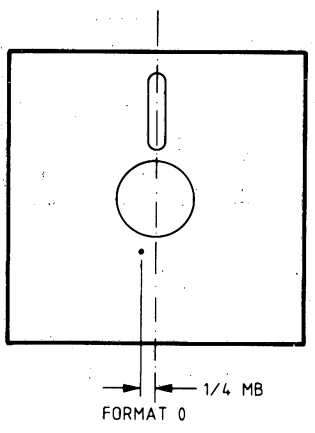
A chip, type 16/11 (Interrupt Handler Chip) can be inserted in the socket of the F1MZ(A) card.
12NC IHC-chip (SPC16/11): 5122 011 30760
If this chip is installed, pin 1C05 must be disconnected and the level is strapped by 6 U-links on the F1MZ(A).

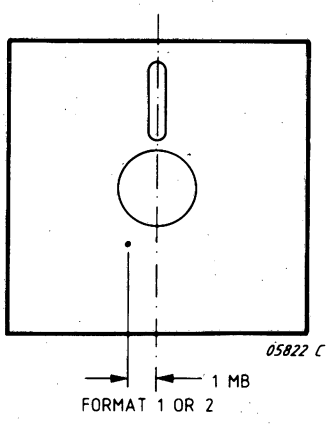
16.2 FORMATS AND DISCETTES:

Format 0	Format 1	Format 2
1 sided discette single density 1 head	2 sided discette double density 2 heads	2 sided discette double density 2 heads
77 track (0 -76) track 0 - Index 1 - 73 or 74 - Data tracks 75,76 - Spare	77 cylinders total (0 - 76) cylinder 0 - Index 1 - 74 - Data cyl 75,76 - Spare	77 cylinders total (0 -76) cylinder 0 - Index 1 - 74 - Data cyl 75, 76 - Spare
26 sectors/track 128 bytes/sector	26 sectors/track * 256 bytes/sector	8 sectors/track 1024 bytes/sector
total 'data' capacity 246,272 bytes	total 'data' capacity 985, 088 bytes	total 'data' capacity 1,212,416 bytes
drive types CDC 9404 or CDC 9406	drive type CDC 9406	drive type CDC 9406
discette type - 20 cm, IBM, 1-sided P/N 2305830 (or equiv.)	discette type - 20 cm/8 IBM, 2-sided P/N 1766872 (or equiv.)	discette type - 20 cm/8" IBM 2-sided P/N 1669045 (or equiv.)
IBM systems using this format - IBM 3740, IBM 5320, IBM 1, all systems using IBM "Standard Data Interchange	IBM systems using this format - IBM 34-2	IBM systems using this format - IBM 34-2

* Note: Format 1 - Cyl. 0, head 0 is formatted as for format 0
(i.e. 26 sectors/track, 128 bytes/sector)
Format 2 - Cyl. 0, head 0 as for format 0
Cyl. 0, head 1 as for format 1

Table 16.1 FORMATS AND DISCETTES





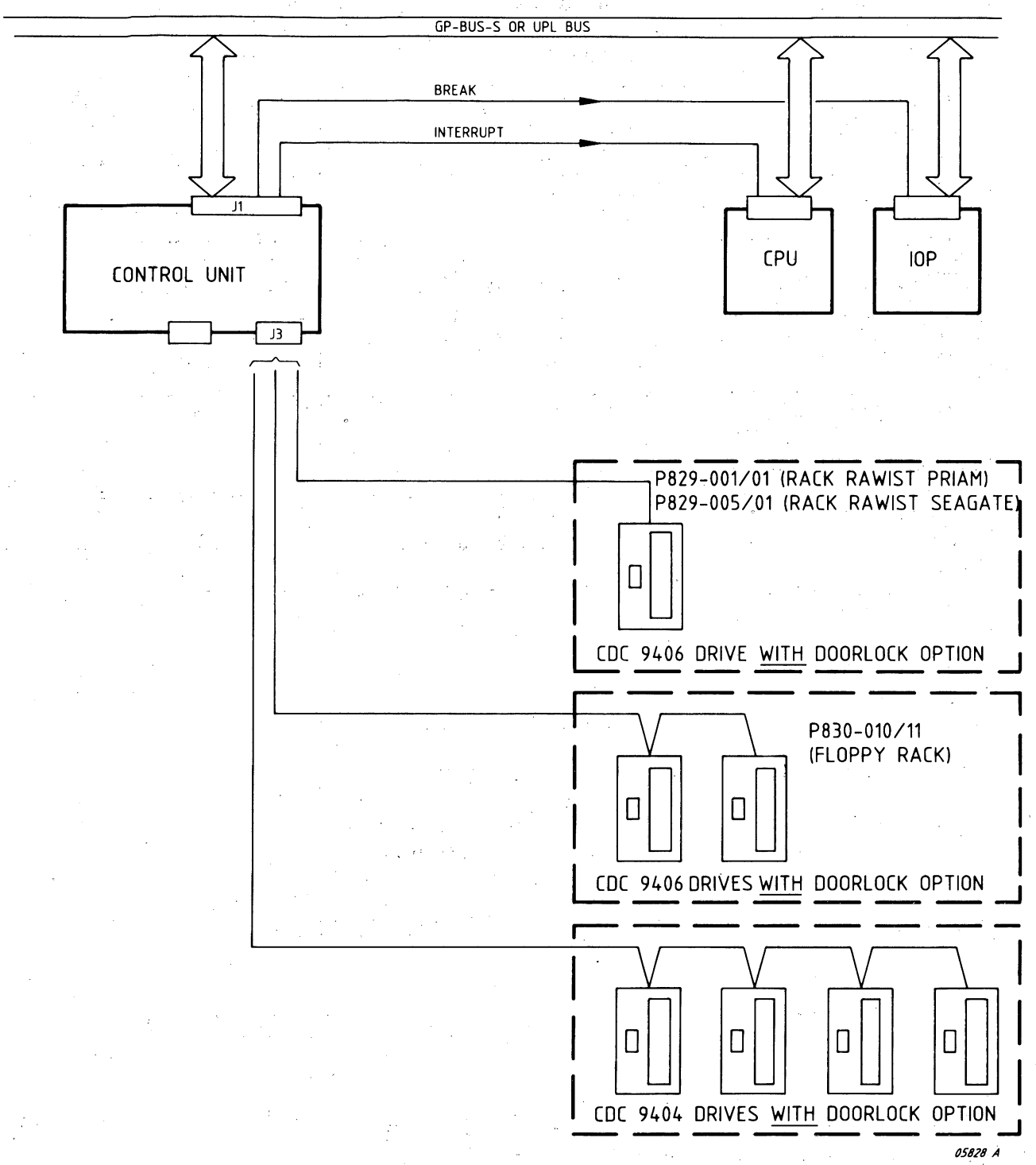
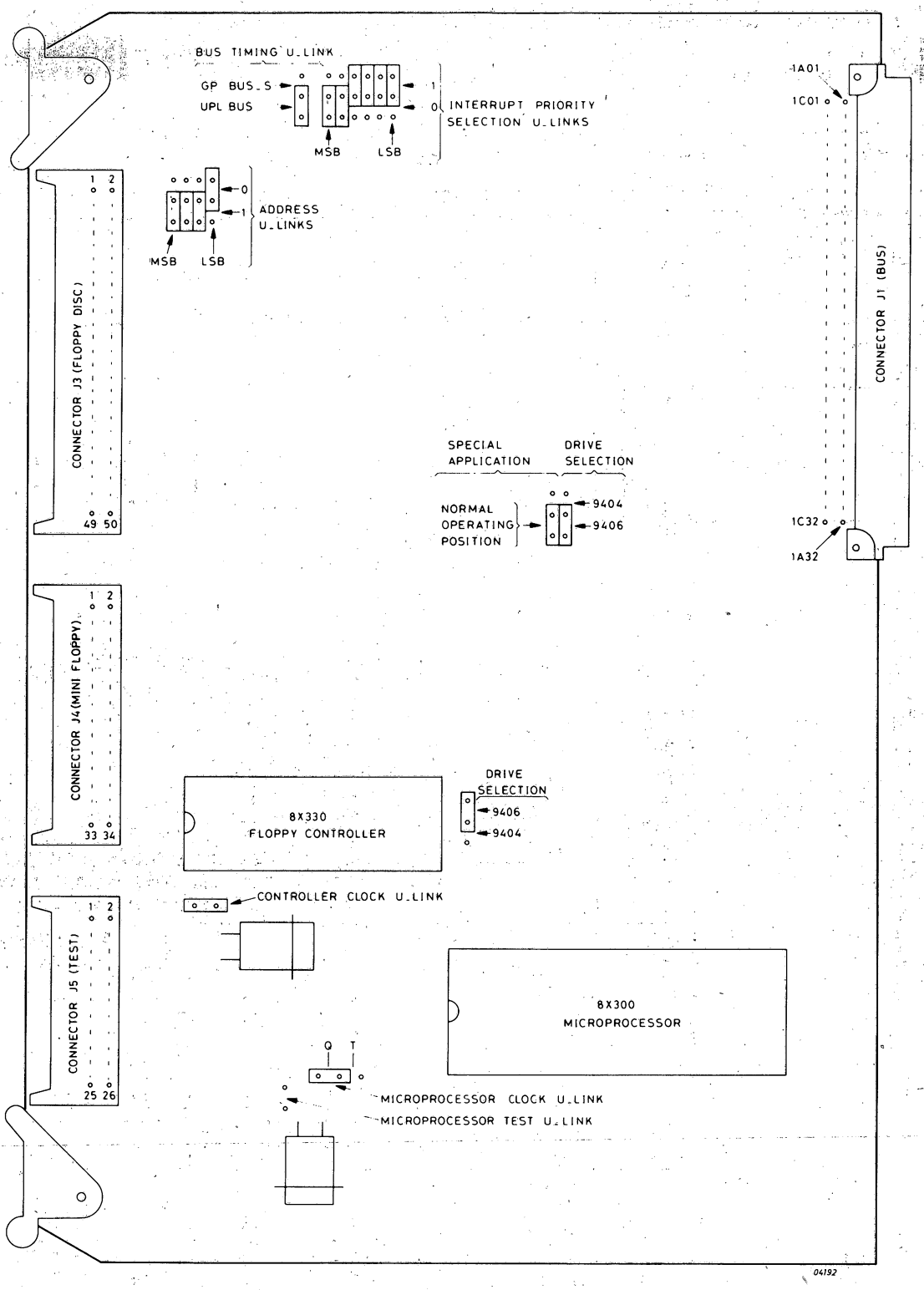


Figure 16.1 POSITION OF CU IN THE SYSTEM



Connector J4 not present on F1MZA
Interrupt U-links for priority level 15 (001111)
Address U-link shown for CU address 14 (1110)
Bus timing link shown for use of CU with UPL Bus
Drive selection links (2) for use with type 9406 drive
Special application link shown in its normal operating position
Microprocessor clock link shown in position for normal operation
Controller clock link normally fitted, microprocessor test link not normally fitted. Two U links for clock on F1MA instead of one only.

Figure 16.2 U-LINK SETTING F1MZ (A)

16.4 INTERFACE CONNECTIONS

CU-Drive Interface

Pin No.	Signal Mnemonic	Signal Function	
3J01-43, 49 (odd numbers)	0V	Ground	
3J02	RDLN	Read data/clock composite signal	
3J04	HLN	Head load signal	
3J06	TRON	Track Zero detect	
3J08	INDN	Index Pulse	
3J10	LWCN	Low write current select	
3J12	STEPN	Each pulse of STEPN moves the head one track	
3J14	DIRN	in the direction specified by DIRN	
3J16	WEN	Write Enable signal	
3J18	WDN	Write Data signal	
3J20	SELON	Drive unit 1 ready selection signal	
3J22	SEL1N	Drive unit 2 ready selection signal	
3J24	SEL2N	Drive unit 3 ready selection signal	
3J26	SEL3N	Drive unit 4 ready selection signal	
5A28	RDYON	Drive unit 1 ready signal	
3J30	RDY1N	Drive unit 2 ready signal	
3J32	RDY2N	Drive unit 3 ready signal	
3J34	RDY3N	Drive unit 4 ready signal	
3J36	WPRN	Write protected disc	
3J38, 44, 46	--	Not Used	
3J40	DC40N	Unit 1 door lock (9404)	Head Select (9406)
3J42	DC42N	Unit 2 door lock (9404)	Unit 1 door lock (9406)
3J45	--	Not used (9404)	Special applications
3J47	--	Not used (9404)	(see table below)
3J48	DC48N	Unit 3 door lock (9404)	Unit 2 door lock (9406)
3J50	DC50N	Unit 4 door lock (9404)	Discette type (9406)

Note: F1MZA has pin numbering according to Double Euro standard for J3.
Refer to chapter 9.3 : Interfaces.

SPECIAL APPLICATIONS

CU signal name	Pin No.	CU function with 9404	9404 drive signal name	CU function with 9406	9406 drive signal name
DC40N	40	Lock unit 0	Lock unit 1	Head select	Head select
DC42N	42	Lock unit 1	Lock unit 2	Lock unit 0	Lock unit 1
DC45N	45	--	Ground	Lock unit 2	Ground
DC47N	47	--	Ground	Lock unit 3	Ground
DC48N	48	Lock unit 2	Lock unit 3	Lock unit 1	Lock unit 2
DC50N	50	Lock unit 3	Lock unit 4	Disc type	Disc type

Table 16.2 CONNECTIONS TO FLOPPY DISC DRIVES (CONNECTOR J3)

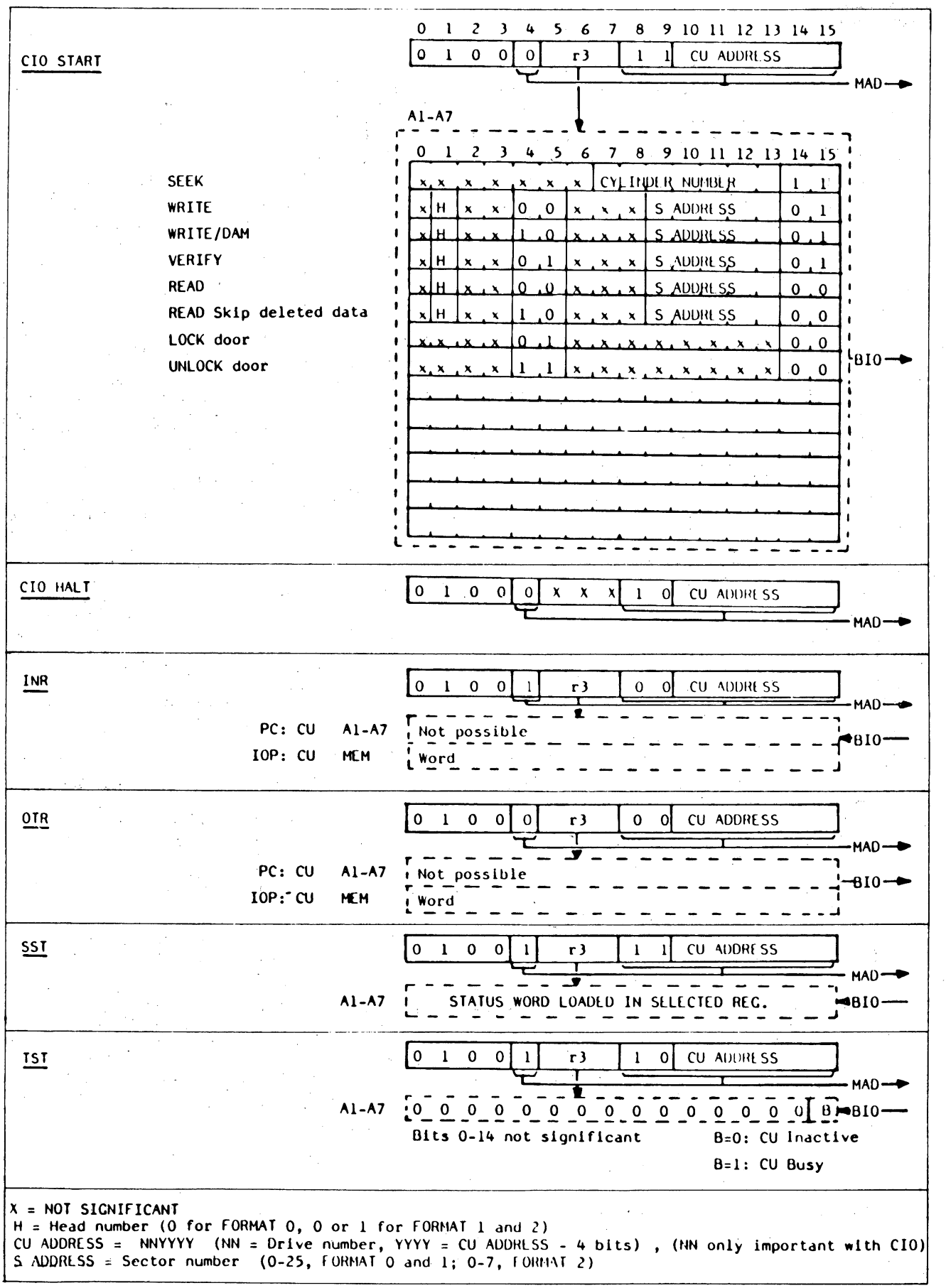


Figure 16.3 INSTRUCTION/COMMAND-WORD FORMATS

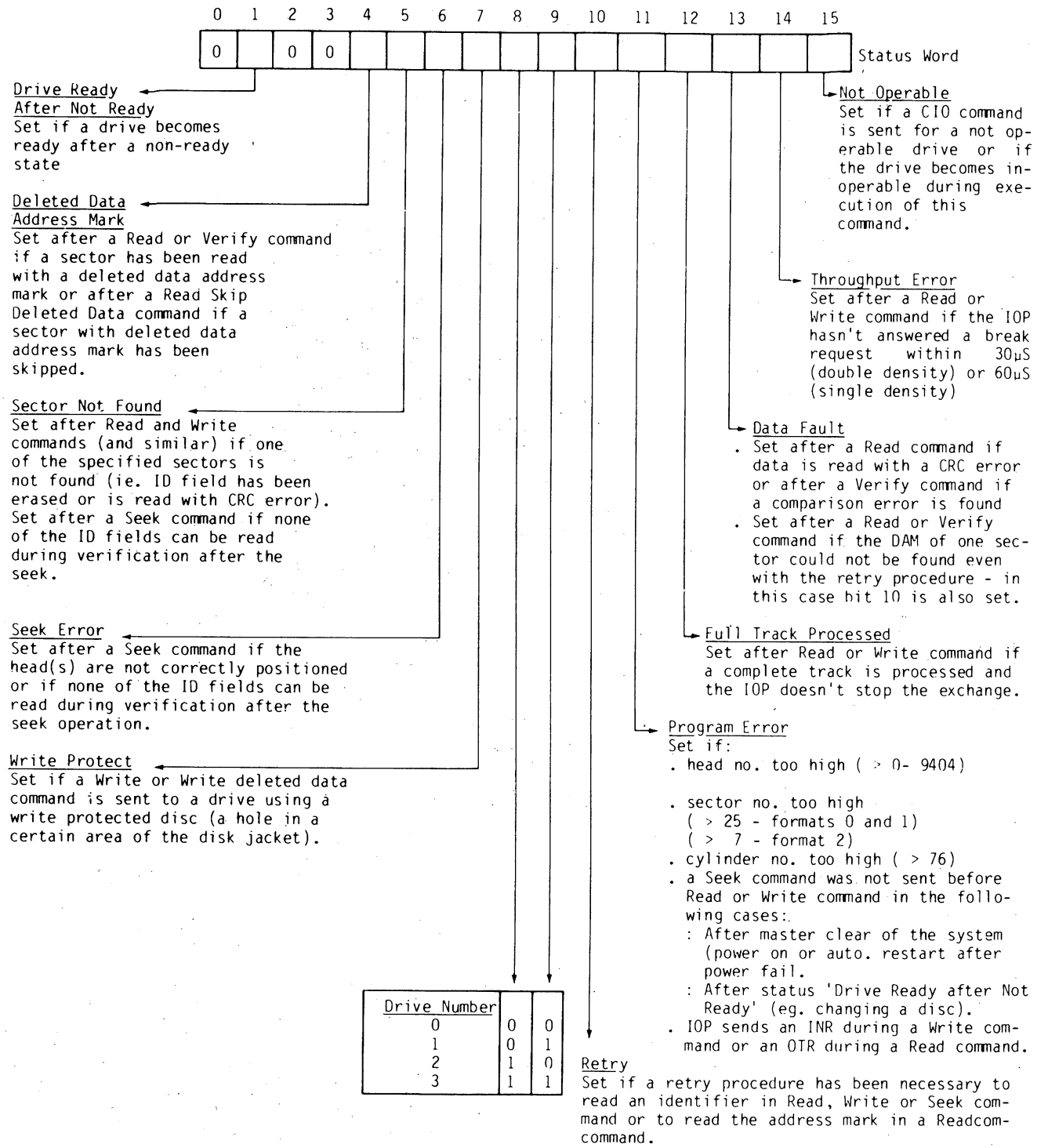


Figure 16.4 EXPLANATION OF STATUS WORD

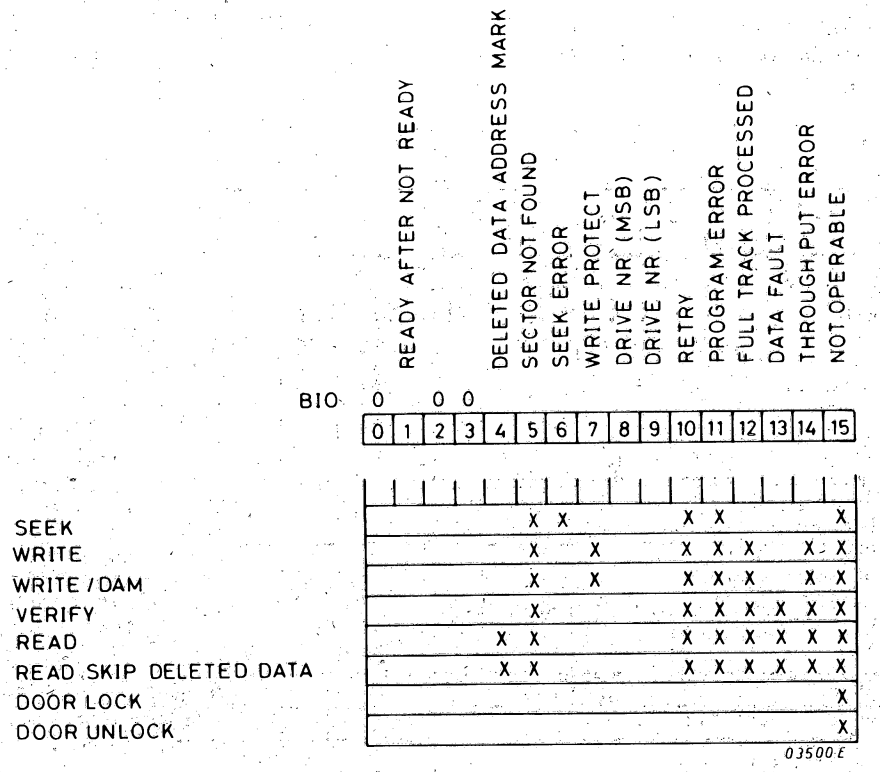


Figure 16.5 STATUS WORD: POSSIBLE CONFIGURATION

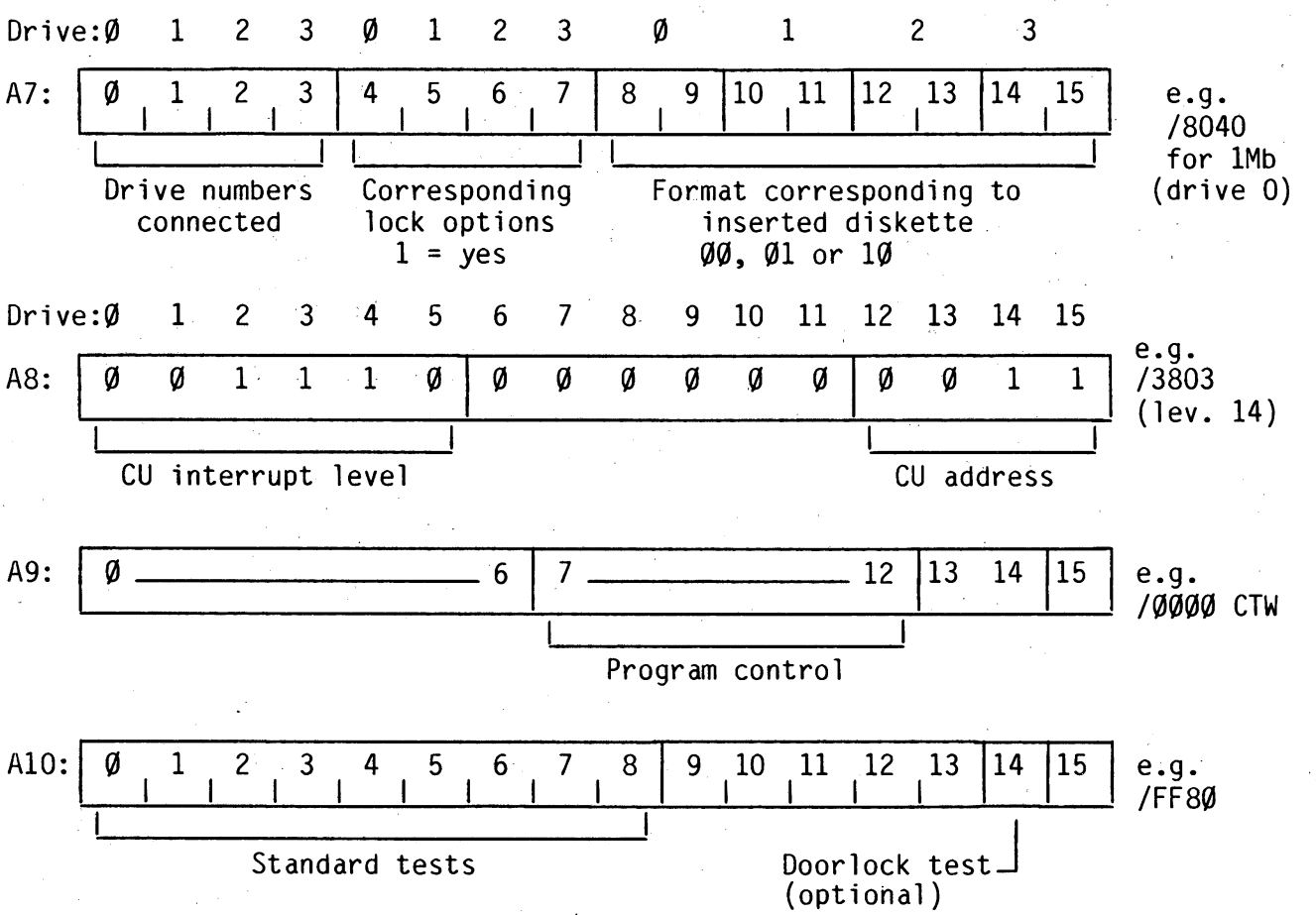
16.6 SHORT DESCRIPTION OF TEST PROGRAMS

TESTPROGRAM BF1MZ

For testing floppy drives connected to the 1Mb CU
RTC and PF/AR allowed

Procedure:

- IPL
  Program displays /7ØØ = restart point = stop on interrupt
- ==== Load Scratch Diskette! ====
- Registers:



- RTC on
  /7ØØ is normal end (restart) of program
  /5EØ is information stop
  /5FØ is error stop

For further information see the official description of the testprograms.

BF1MZ tested:

The Testprogram can perform the following 9 checks:

Check Ø - IFØØØØ Control Unit Test
Check 1 - IFØØØ1 Control Unit Test (contd)
Check 2 - IFØØØ2 Write on entire diskette
Check 3 - IFØØØ3 Write on sectors sequentially and verify the entire track
Check 4 - IFØØØ4 Write an entire track and verify sectors sequentially
Check 5 - IFØØØ5 Write statement initialized with IOP Read
Check 6 - IFØØØ6 Write a buffer shorter than the sector length
Check 7 - IFØØØ7 Write and read deleted data address marks
Check 8 - IFØØØ8 Random seek commands
Check E - IFØØØE Door lock/unlock test

The Check Ø must only be run once after the MC button is pushed and the loop on test option is not available.
The Check E is considered as an optional check (i.e. it can only be performed with drives having the LOCK option) and must be run separately.

Procedure	5111 991 11085
Listing	5111 991 11095
Program	5111 199 63385

```
00000                           IDENT    ADJF1M
00001                  *PROGRAM TO ADJUST 1M FLOPPY P800 SYSTEMS
00002                  *
00003                  * AFTER IPL THE PROGRAM STOPS
00004                  *
00005                  * LOAD ALIGNMENT FLOPPY IN DRIVE 0
00006                  *
00007                  * PROGRAM SELECTION AFTER EACH TIME THE PROGRAM STOPS:
00008                  *   (REG A1)   1: ALIGNMENT HEAD 0 (CYLINDER 38)
00009                  *
00010                  *              3: INDEX TO BURST ADJUSTM. HEAD 0 (CYL. 1)
00011                  *
00012                  *           BEFORE NEXT STEP, LOAD A SCRATCH FLOPPY
00013                  *              5: CYLINDER ZERO ADJUSTMENT (400 X SEEK BETWEEN CYL 0 AND 1)
00014                  *           BEFORE NEXT STEP, LOAD ALIGNMENT FLOPPY AGAIN
00015                  *              6: CHECK ALIGNMENT HEAD 0
00016                  *
00017                  *
00018                  *            > 7: STOP, UNLOAD THE HEADS
00019                  * TO START PRESS RUN BUTTON
00020                  ************************************************************
00021  0000                            RES      /40
00022  0080  FFFF                      DATA     /FFFF,0
       0082  0000
00023        0003      ADR      EQU      3
00024  0084  20BF      START    INH
00025  0086  0101               LDK      A1,1                  DEFAULT SELECTION PROG 1
00026  0088  207F      INPUT    HLT
00027  008A  4FC3               SST      A7,ADR                RESET READY INT JUST IN CASE
00028  008C  2107               ANK      A1,7                  MASK VALUE 1 TILL 7
00029  008E  8204               LDR      A2,A1
00030  0090  580A               RB(Z)    INPUT                 WRONG BIT
00031  0092  1A01               SUK      A2,1                  PROG 1?
00032  0094  5016               RF(Z)    PROG1
00033  0096  1A01               SUK      A2,1                  2?
00034  0098  5020               RF(Z)    PROG2
00035  009A  1A01               SUK      A2,1                  3?
00036  009C  5022               RF(Z)    PROG3
00037  009E  1A01               SUK      A2,1                  4?
00038  00A0  502C               RF(Z)    PROG4
00039  00A2  1A01               SUK      A2,1                  5?
00040  00A4  502E               RF(Z)    PROG5
00041  00A6  1A01               SUK      A2,1                  6?
00042  00A8  503E               RF(Z)    PROG6
00043                  *
00044                  *****HEAD 1 ALIGNMENT CHECK*****
00045                  *
00046  00AA  570E      PROG7    RF       PROG2
00047                  *
00048                  *****HEAD 0 ALIGNMENT*****
00049                  *
00050  00AC  0200      PROG1    LDK      A2,0                  READ HEAD 0
00051  00AE  0498               LDK      A4,/98                SEEK CYL 38
00052  00B0  44C3               CIO      A4,1,ADR              EXEC SEEK COMM
00053  00B2  4FC3               SST      A7,ADR
00054  00B4  5C04               RB(NA)   *-2
00055  00B6  42C3               CIO      A2,1,ADR              EXEC READ COMM
00056  00B8  5F32               RB       INPUT
00057                  *
00058                  *****HEAD 1 ALIGNMENT*****
00059                  *
00060  00BA  8220      PROG2    LDKL     A2,/4000              READ HEAD 1
       00BC  4000
00061  00BE  5F12               RB       PROG1+2
00062                  *
00063                  *****INDEX TO BURST HEAD 0 ADJUST*****
00064                  *
00065  00C0  0200      PROG3    LDK      A2,0                  READ HEAD 0
00066  00C2  0407               LDK      A4,7                  SEEK CYL 1
00067  00C4  44C3               CIO      A4,1,ADR
00068  00C6  4FC3               SST      A7,ADR
00069  00C8  5C04               RB(NA)   *-2
00070  00CA  42C3               CIO      A2,1,ADR              READ
00071  00CC  5F46               RB       INPUT
00072                  *
00073                  *****INDEX TO BURST CHECK HEAD 1*****
00074                  *
00075  00CE  8220      PROG4    LDKL     A2,/4000              READ HEAD 1
       00D0  4000
00076  00D2  5F12               RB       PROG3+2
00077                  *
00078                  *****CYLINDER 0 ADJUSTMENT*****
00079                  *
00080  00D4  8220      PROG5    LDKL     A2,800                400 TIMES REPEAT SEEK
       00D6  0320
00081  00D8  0403               LDK      A4,3                  SEEK CYL 0
00082  00DA  44C3               CIO      A4,1,ADR
00083  00DC  4FC3               SST      A7,ADR
00084  00DE  5C04               RB(NA)   *-2
00085  00E0  340C               XRK      A4,/C                 SEEK CYL 3, 0, 3, ETC.
00086  00E2  1A01               SUK      A2,1
00087  00E4  5C0C               RB(NZ)   PROG5+6               400 TIMES ?
00088  00E6  5F60               RB       INPUT                 NEXT STEP
00089                  *
00090                  *****HEAD 0 ALIGNMENT CHECK*****
00091                  *
00092  00E8  5F3E      PROG6    RB       PROG1
00093                           END      START
```

```
00000                           IDENT    F1SEEK
00001                   * SEEK TEST FOR F1M-Z (FLOPPY CU 1MB)
00002                   * SEEKS BETWEEN CYL 00 AND 32
00003                   * DRIVE 0 ONLY. STATUS IN A5
00004                   * IF SEEKING, YOU HEAR THE REGULAR MOVEMENT
00005                   *
00006                   * REG A4 IS PRESET BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00007                   *            /0003    0 0 0 0 0 0 0 0 0 0  0  0  0  0  1  1
00008                   *                                          ----------------
00009                   *                                          SEEK CYLINDER NUMBER
00010          0003     DA       EQU      3
00011   0000            RES      /40
00012   0080   FFFF     DATA     DATA     /FFFF
00013   0082   0000     DATA     0
00014   0084   0403     START    LDK      A4,3
00015   0086   207F              HLT
00016   0088   208F              INH
00017   008A   44C3     RET      CIO      A4,1,DA              SEEK
00018   008C   5C04              RB(4)    *-2
00019   008E   4DC3              SST      A5,DA                STATUS
00020   0090   5C04              RB(4)    *-2
00021   0092   8514              LDR      A5,A5                SET CR ACCORDING STATUS
00022   0094   5104              RF(1)    ST
00023   0096   3480              XRK      A4,/80               CHANGE CYL 00 - 32, ETC
00024   0098   5F10              RB       RET
00025   009A   207F     ST       HLT
00026                            END      START


00000                           IDENT    F1LOOP
00001                   *
00002                   * PROGRAM TO WRITE AND READ A SECTOR CONTINUOUSLY (CU 1MB)
00003                   * WRITE BUFFER /200 UP UNTIL /27E
00004                   * READ BUFFER /300 UP UNTIL /37E
00005                   * DRIVE 0 ONLY.  REG A5 CONTAINS STATUS
00006                   *
00007                   *    PRESET A1: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00008                   *             /0001  0 0 0 0 0 0 0 0 0 0  0  0  0  0  1
00009                   *              =CIO     -                 I-----------I     -
00010                   *                     HEAD               SECTORNO.         WRITE
00011                   *
00012                   *           A2: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00013                   *            /C040  1 1 0 0 0 0 0 0 0 1  0  0  0  0  0  0
00014                   *             =WER1   -               I--------------------I
00015                   *                    WRITE                BLOCK LENGTH
00016                   *
00017                   *           A3: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00018                   *            /0200  0 0 0 0 0 0 1 0 0 0  0  0  0  0  0  0
00019                   *             =WER2 I-----------------------------------I
00020                   *                                BUFFER  ADDRESS
00021                   *
00022                   *           A4: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00023                   *            /0003  0 0 0 0 0 0 0 0 0 0  0  0  0  0  1  1
00024                   *            =SEEK                 I-----------------I
00025                   *                                    CYL NUMBER
00026                   *
00027                   * CHECK CORRECT RUNNING:STOP PROGRAM , COMPARE IF /200 AND ON
00028                   * EQUALS /300 AND ON.
00029                   *    NOTE: DISCETTE FORMAT 0,SS,SD  26 SECTORS,64 WORDS/SECTOR
00030                   * ERROR: STATUS STOP AT /BC (/00BE AT HHP):A5 CONTAINS STATUS WORD
00031                   *
00032          0003     DA       EQU      3
00033   0000            RES      /40
00034   0080   FFFF     DATA     DATA     /FFFF
00035   0082   0000     DATA     0
00036   0084   0101     START    LDK      A1,1                 PRESET REG
00037   0086   8220              LDKL     A2,/C040
        0088   C040
00038   008A   8320              LDKL     A3,/200
        008C   0200
00039   008E   0403              LDK      A4,3
00040   0090   207F              HLT
00041   0092   20BF              INH
00042   0094   44C3              CIO      A4,1,DA              SEEK
00043   0096   5C04              RB(4)    *-2
00044   0098   4DC3              SST      A5,DA                STATUS
00045   009A   5C04              RB(4)    *-2
00046   009C   8514              LDR      A5,A5
00047   009E   511C              RF(1)    ST                   STATUS FAULT
00048   00A0   7206     RET      WER      A2,DA+DA
00049   00A2   7307              WER      A3,DA+DA+1
00050   00A4   41C3              CIO      A1,1,DA              PREPARE WRITE (OR READ)
00051   00A6   5C04              RB(4)    *-2
00052   00A8   4DC3              SST      A5,DA                STATUS
00053   00AA   5C04              RB(4)    *-2
00054   00AC   8514              LDR      A5,A5
00055   00AE   510C              RF(1)    ST                   STATUS FAULT
00056   00B0   3101              XRK      A1,1
00057   00B2   8220              XRKL     A2,/4000             CHANGE WRITE TO READ,VICE VERSA
        00B4   4000
00058   00B6   8320              XRKL     A3,/0100
        00B8   0100
00059   00BA   5F1C              RB       RET
00060   00BC   207F     ST       HLT
00061                            END      START
```

This program can be used in case program load fails.
The program READF1 checks on read errors and can be used to distinguish read errors and software problems.

```
00000                          IDENT    READF1
00001                  *
00002                  *  READ CHECK ON IDENTIFIERS AND DATA
00003                  *   0.25 DISCETTES AND 1M (26 SECTORS)
00004                  *
00005                  *  STATUS BITS:
00006                  *                    5  SECTOR NOT FOUND
00007                  *                    6  SEEK ERROR
00008                  *                   10  RETRY
00009                  *                   13  DATA ERROR
00010                  *                   14  THROUGHPUT ERROR
00011                  *                   15  NOT OPERABLE
00012                  *                    4   CONTINUE (DDAM FOUND)
00013                  *
00014          0003    DA        EQU       3
00015  0000            RES       /40
00016  0080  FFFF      DATA      /FFFF,0
       0082  0000
00017  0084  207F      START     HLT
00018  0086  208F                INH
00019  0088  87A0                LDKL      A15,/180              STACK
       008A  0180
00020  008C  4DC3                SST       A5,DA
00021  008E  0100                LDK       A1,0                  SELECT HEAD 0
00022                  *********SEEK**********
00023  0090  0403      HEAD      LDK       A4,3                  CYL 0
00024  0092  44C3      NXTCY     CIO       A4,1,DA               SEEK
00025  0094  F7A1                CF        A15,STATUS
       0096  00BA  R
00026                  **********READ**********
00027  0098  8220                LDKL      A2,/8D00
       009A  8D00
00028  009C  7206                WER       A2,DA+DA
00029  009E  8320                LDKL      A3,/200               DATA BUF ADDR
       00A0  0200
00030  00A2  7307                WER       A3,DA+DA+1
00031  00A4  41C3                CIO       A1,1,DA               READ FROM DRIVE 0
00032  00A6  F7A1                CF        A15,STATUS
       00A8  00BA  R
00033  00AA  1404      ON        ADK       A4,4                  NEXT CYL
00034  00AC  EC20                CWK       A4,/133               CYL 76?
       00AE  0133
00035  00B0  5A20                RB(2)     NXTCY
00036  00B2  9120                ADKL      A1,/4000              HEAD 1
       00B4  4000
00037  00B6  5928                RB(1)     HEAD
00038  00B8  5F36                RB        START
00039                  *
00040  00BA  4DC3      STATUS    SST       A5,DA
00041  00BC  5C04                RB(4)     *-2
00042  00BE  A520                ANKL      A5,/0E27
       00C0  0E27
00043  00C2  5002                RF(0)     RTN
00044  00C4  207F                HLT
00045  00C6  F03E      RTN       RTN       A15
00046                          END       START
```

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18.1 DISC CONTROL UNIT - IDENTIFICATIONS

Type number : P824-140 (CDDZ)

Test programs : X1215: BZCDD1
X1216: BZ1216

Channel : Hardware channel MIOP, IOPZR

Break-connection : 1A05

Interrupt-connection : 1C05

Power Consumption : 5 Volt, 2.9 Amp

12NC code on the sticker on the board:

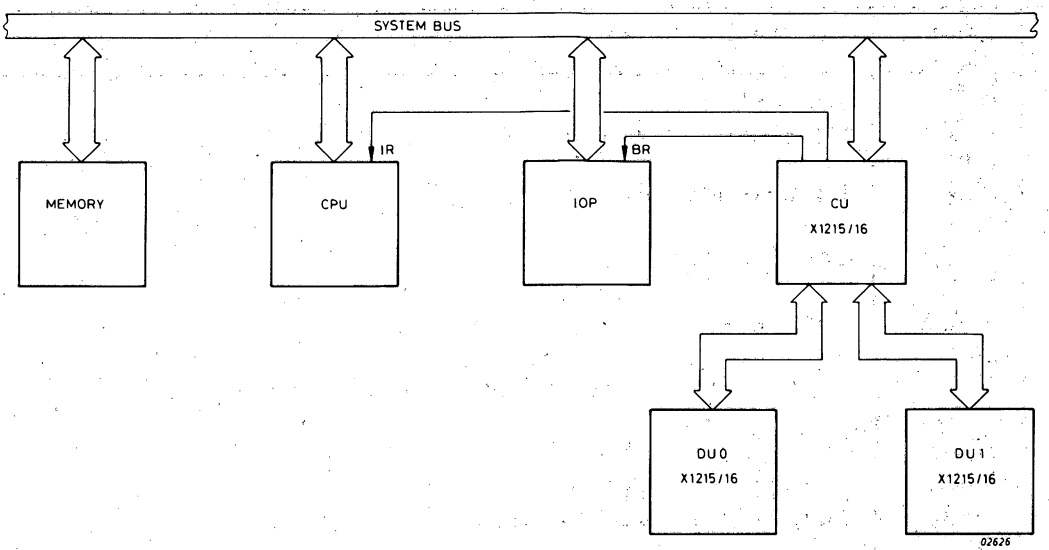
CDDZ: 5111 199 6698x (5322 216 25617)
5111 199 6224x (5322 216 21032)

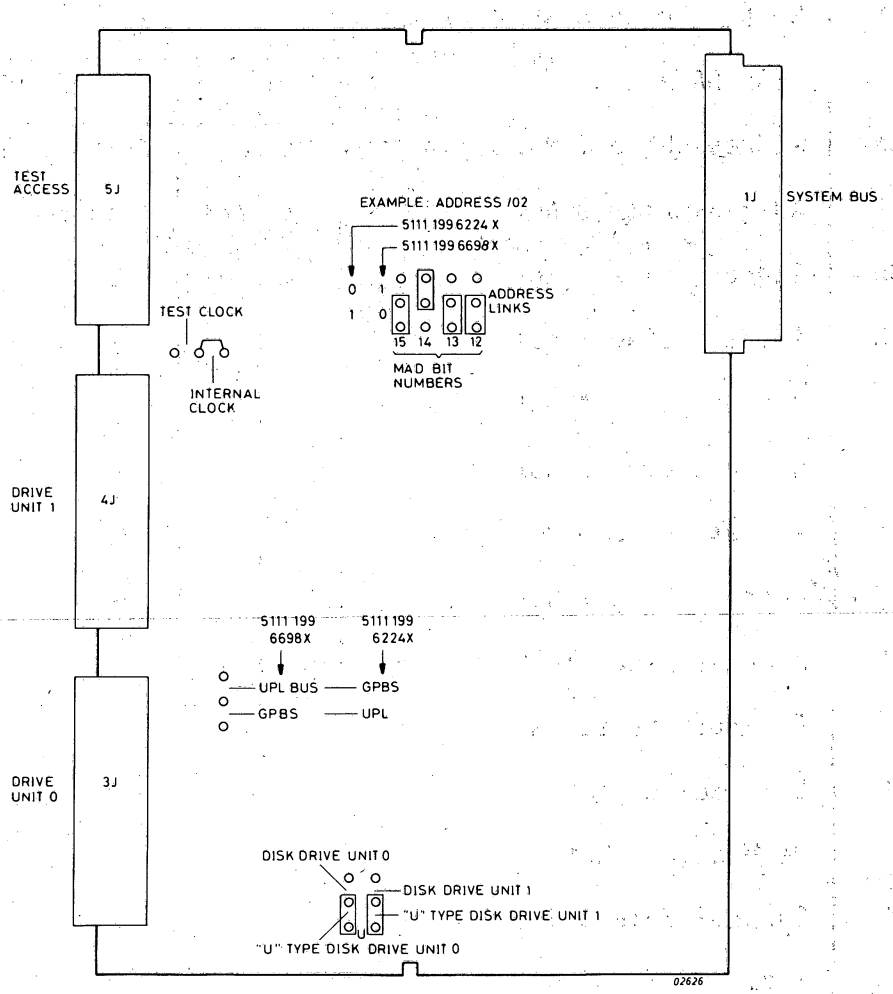
X = Modification level.

Devices : 2x X1215(2.7M6) - P824 - 012 or
2x X1216(5.4M6) - P824 - 014

Cables to device : Cable 3.5m 5111 199 63020
Cable 7.5m 5111 199 63030

Disc Cartridge : P824-100/01
Disc 16 sect, 2.5/5 MB 8709 001 20201





NOTE: A "U" TYPE DISK DRIVE UNIT IS ONE WHICH STOPS ON AN ERROR AND WHICH RESTARTS AUTOMATICALLY AFTER AN ERROR CONDITION HAS BEEN RECTIFIED

Figure 18.1 C.U. IN SYSTEM AND U-LINK SETTING

Pin No.	Signal	Function
J3-01	GND.	
02	CONN	Cylinder On Not
03	GND.	
04	URN	Unit Ready Not
05	GND.	
06	USA1N	Unsafe Action 1
07	GND.	
08	USA2N	Unsafe Action 2
09	GND.	
10	ATON	(Pin 10 is connected but signal ATON is not used)
11	GND.	
12	IPFON	Index Pulse Fixed Not
13	GND.	
14	IPCON	Index Pulse Cartridge Not
15	GND.	
16	SPFON	Sector Pulse Fixed Not
17	GND.	
18	SPCON	Sector Pulse Cartridge Not
19	GND.	
20	RDON	READ DATA Not
21	GND.	
22	AL0ON	Address Line 0 Not
23	GND.	
24	AL1ON	Address Line 1 Not
25	GND.	
26	AL2ON	Address Line 2 Not
27	GND.	
28	AL3ON	Address Line 3 Not
29	GND.	
30	AL4ON	Address Line 4 Not
31	GND.	
32	AL5ON	Address Line 5 Not
33	GND.	
34	AL6ON	Address Line 6 Not
35	GND.	
36	AL7ON	Address Line 7 Not
37	GND.	
38	AHOON	Address Line High Not
39	GND.	
40	CSON	Cylinder Select Not
41	GND.	
42	USLON	Unit Select Not
43	GND.	
44	HSON	Head Select Not
45	GND.	
46	CTSON	Control Select Not
47	GND.	
48	STOPO	Stop
49	GND.	
50	WDLON	WRITE DATA Not

CSON	MSON	CTSON
1	0/1	Write Enable
2	2/3	Read Enable
4	-	Seek
8	-	-
16	-	Erase Enable
32	-	Seek (NOT USED)
64	-	Seek-To-Zero
128	-	-
256	-	-

Table 18.1 DRIVE UNIT 0 - INTERFACE CONNECTOR J3

Pin No.	Signal	Function
J4-01	GND.	
02	CONN	Cylinder On Not
03	GND.	
04	URN	Unit Ready Not
05	GND.	
06	USA1N	Unsafe Action 1
07	GND.	
08	USA2N	Unsafe Action 2
09	GND.	
10	AT1N	(Pin 10 is connected but signal AT1N is not used)
11	GND.	
12	IPF1N	Index Pulse Fixed Not
13	GND.	
14	IPC1N	Index Pulse Cartridge Not
15	GND.	
16	SPF1N	Sector Pulse Fixed Not
17	GND.	
18	SPC1N	Sector Pulse Cartridge Not
19	GND.	
20	RD1N	READ DATA Not
21	GND.	
22	AL01N	Address Line 0 Not
23	GND.	
24	AL11N	Address Line 1 Not
25	GND.	
26	AL21N	Address Line 2 Not
27	GND.	
28	AL31N	Address Line 3 Not
29	GND.	
30	AL41N	Address Line 4 Not
31	GND.	
32	AL51N	Address Line 5 Not
33	GND.	
34	AL61N	Address Line 6 Not
35	GND.	
36	AL71N	Address Line 7 Not
37	GND.	
38	AH01N	Address Line High Not
39	GND.	
40	CS1N	Cylinder Select Not
41	GND.	
42	USL1N	Unit Select Not
43	GND.	
44	HS1N	Head Select Not
45	GND.	
46	CTS1N	Control Select Not
47	GND.	
48	STOP1	Stop
49	GND.	
50	WDL1N	WRITE DATA Not

CS1N	MS1N	CTS1N
1	0/1	Write Enable
2	2/3	Read Enable
4	-	Seek
8	-	-
16	-	Erase Enable
32	-	Seek (NOT USED)
64	-	Seek-To-Zero
128	-	-
256	-	-

Table 18.2 DRIVE UNIT 1 - INTERFACE CONNECTOR J4

PIN NUMBER CU	PIN NUMBER DRIVE
1	32
2	29
3	5
4	2
5	37
6	34
7	7
8	3
9	31
10	28
11	38
12	35
13	27
14	24
15	33
16	30
17	26
18	23
19	4
20	1
21	51
22	48
23	50
24	47
25	49
26	46
27	57
28	54
29	56
30	53
31	55
32	52
33	64
34	60
35	63
36	59
37	43
38	40
39	13
40	10
41	39
42	36
43	14
44	11
45	21
46	17
47	62
48	58
49	12
50	8

Table 18.3 CABLE CDDZ - Drive X1215/6:

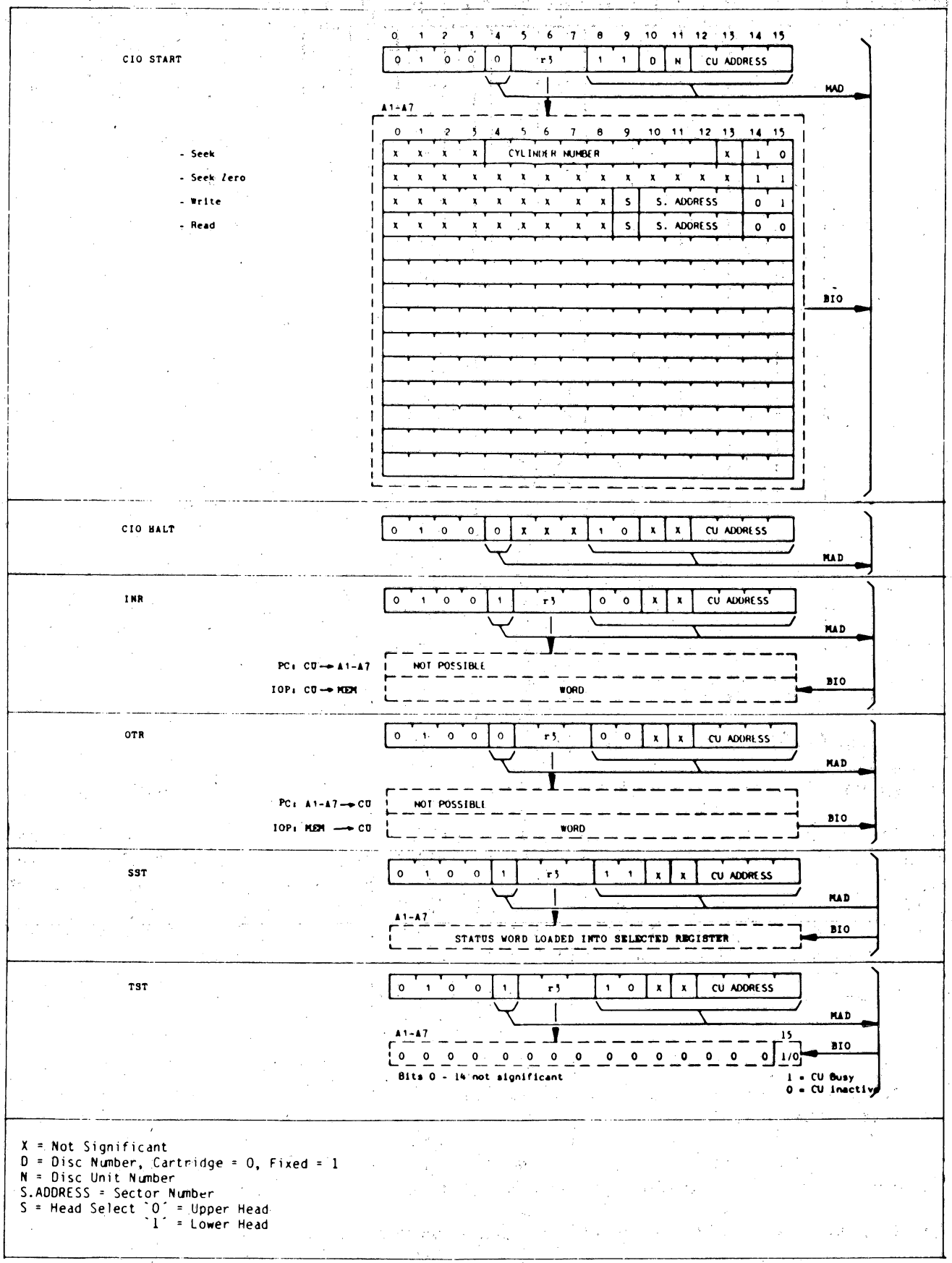
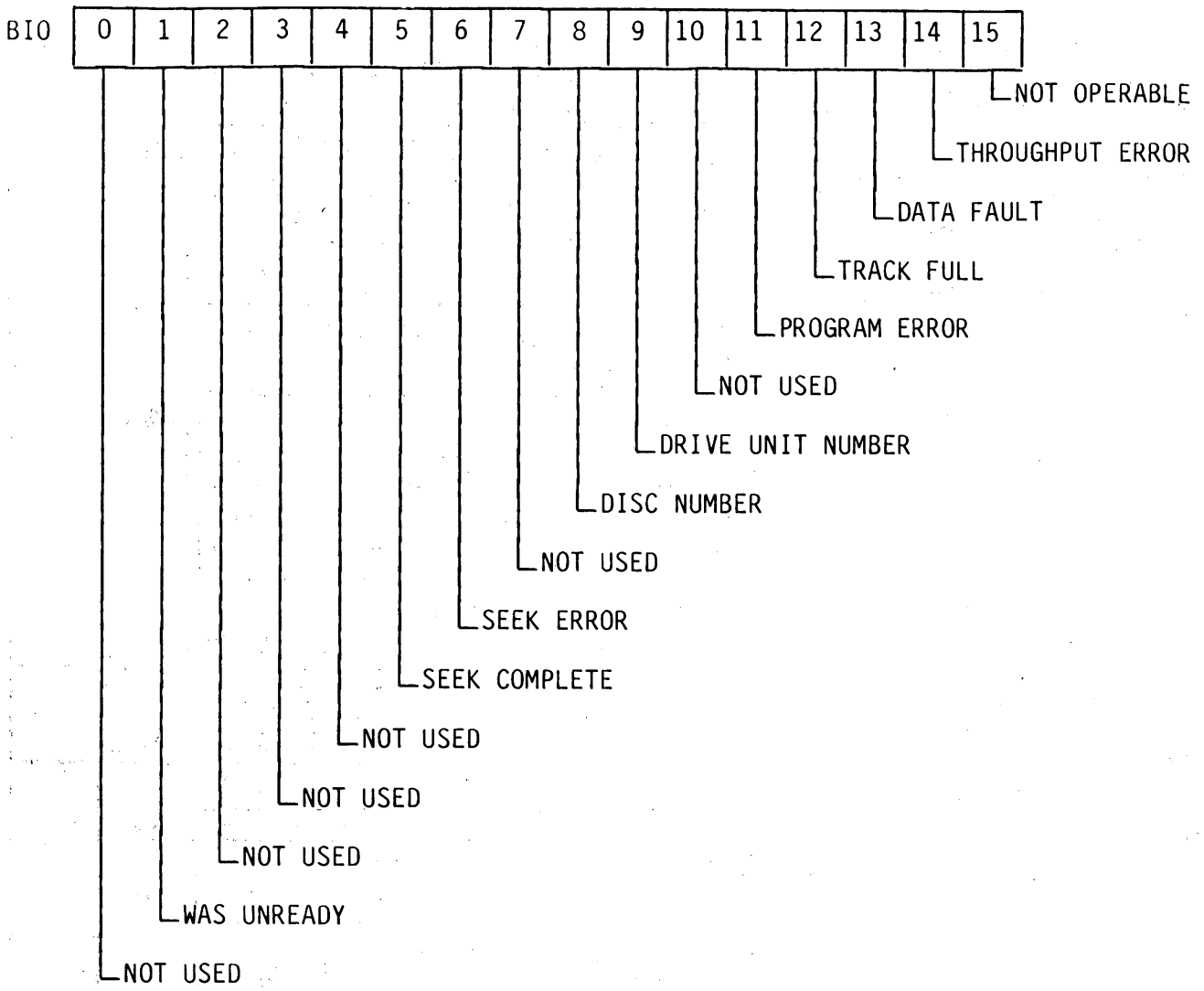


Figure 18.2 INSTRUCTION/COMMAND-WORD FORMATS

18.4.1 STATUS WORD



Bit 15 Not Operable - is set if the drive (indicated in bit 9) is not operable.

Bit 14 Throughput Error - is set during a write operation if both words in the Input Data Buffer have been written to disk and serialization of the current word is completed before the IOP has answered the exchange data request with an OTR. It is set during a read operation if neither word in the Read Data Buffer have been transferred to memory and deserialization of the current word has ended before the IOP has answered the exchange data request with an INR.

Bit 13 Data Fault - is set when the LRC check fails at the end of a read operation.

Bit 12 Track Full - is set after a read or write command if the sector given inside the command is reached again after one revolution, without signal end of transfer from the IOP.

Bit 11 Program Error - is set if the CU receives an OTR command during a read operation or an INR during a write operation.

Bit 9 Drive Unit Number - is set for drive number 1.

Bit 8 Disk Number - is set for the fixed disk. The disk number is valid only after a read or write operation, after a seek or ready interrupt bit 8 will always be zero.

Bit 6 Seek Error - is set if an error has been detected or the drive becomes inoperable during a seek operation.

Bit 5 Seek Complete - is set if the seek operation is complete whether or not errors were detected.

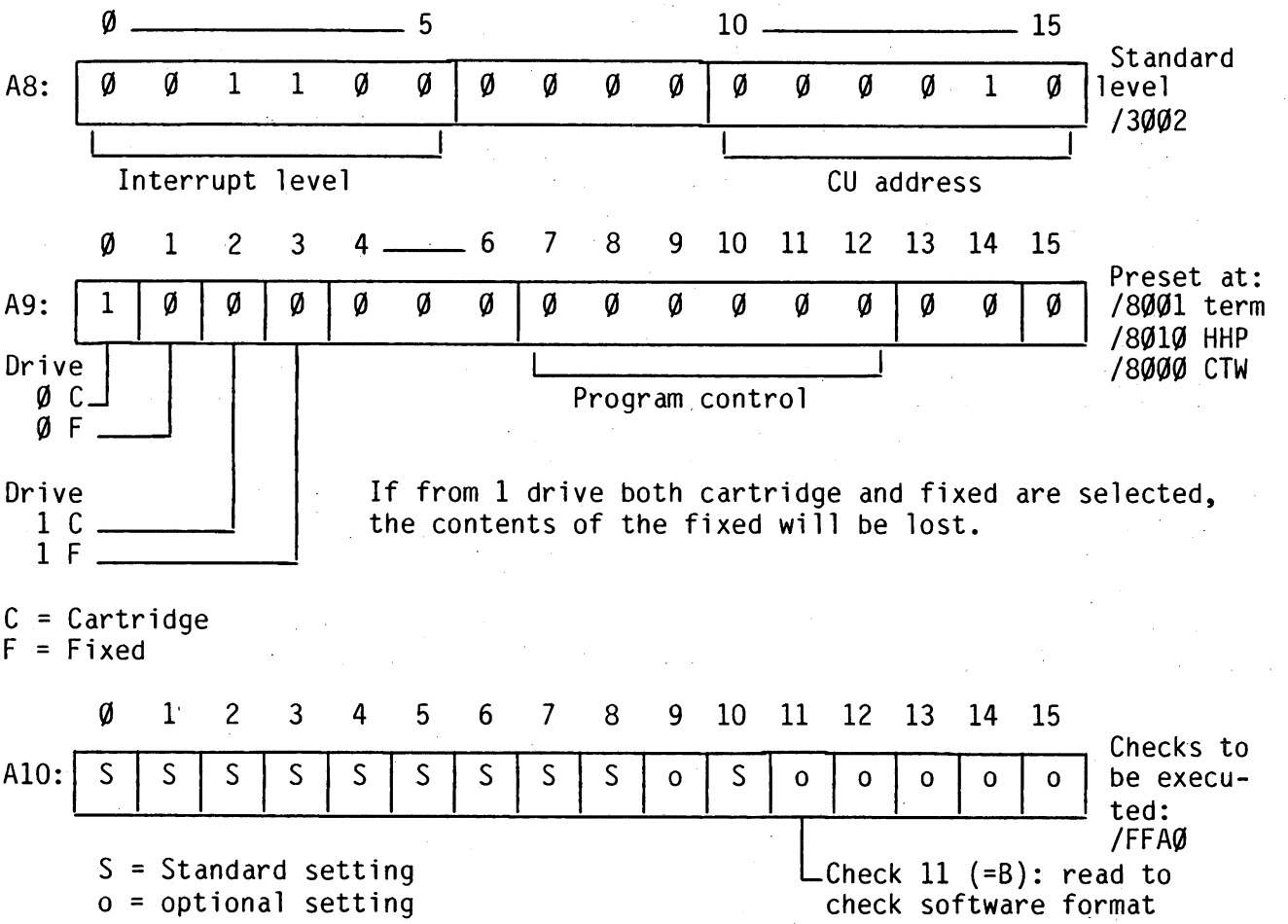
Bit 1 Was Unready - is set if during scanning a change of status has occured from not operable, to operable.

18.5 SHORT DESCRIPTION TEST-PROGRAM

TESTPROGRAM BZCDD1 8K for P824-012 (2,7Mb)
BZ1216 for P824-014 (5,4Mb)

Procedure:

- IPL
  Program displays /7ØØ (= restart point and normal end)
  Rwitch on RTC (PF/AR also possible)
- ==== Load Scratch Cartridge! ====



C = Cartridge
F = Fixed

Error stop at /5FØ
Interrupts return to /7ØØ
Information stop at /5EØ

For more information see official description of testprogram.

BZCDD1 and BZ1216 - tested

Checks Ø through B
These times are only given as an identification and can vary according to the CPU and memory type.

CHECK	DURATION FOR ONE DISC	STANDARD	
CHKØØ	3 mn	Yes	Saving fixed disc on mobile disc (Software format)
CHKØ1	5 s	Yes	Test of controller status
CHKØ2	20 s	Yes	Seek test with timing check
CHKØ3	40 s	Yes	Write and read test on one cylinder
CHKØ4	2 mn	Yes	Write and read test of all disc sector
CHKØ5	1 s	Yes	Read all sector track Ø with chaining command
CHKØ6	1 s	Yes	Write all sector track Ø with chaining command
CHKØ7	1 mn	Yes	Read test of all disc sectors (compatibility test)
CHKØ8	1 mn	Yes	Seek test - checking the identifier
CHKØ9		No	Seek error - not operable and head selection test
CHKØA	3 mn	Yes	Restituting fixed disc
CHKØB	1 mn	No	Read to check one disc (Software format)

Service Routine
It permits seeks, writes or reads to be executed. It starts in /2ØØØ after having initialized some registers. See official testprogram description.

BZCDD1:		BZ1216:	
Procedure	5111 991 11013	Procedure	5111 991 11034
Listing	5111 991 11003	Listing	5111 991 11024
Program	5111 199 63683	Program	5111 199 64654

```
        DATE  80-03-13        IDENT    SEEK

00000                         IDENT    SEEK
00001                  * PROGRAM USABLE INSTEAD OF AN EXERSISER
00002
00003                  *        LOAD START CYLINDER IN REG A1
00004                  *        LOAD LAST CYLINDER IN REG A2
00005                  *        LOAD STEPPING INCREMENT IN REG A3
00006                  *        LOAD TIME DELAY IN REG A6
00007                  *        DISC DRIVE 0 IS ADDRESSED  OTHERWISE CHAGE DEVICE ADDRESSES
00008
00009                           AORG     /80
00010  0080  FFFF               DATA     /FFFF
00011  0082  0000               DATA     0
00012  0084  207F        START  HLT
00013  0086  20BF               INH
00014  0088  8404        CIO    LDR      A4,A1
00015  008A  3C43        CIO1   SLL      A4,3
00016  008C  1402               ADK      A4,2
00017  008E  44C2               CIO      A4,1,2
00018  0090  4DC2               SST      A5,2
00019  0092  5C04               RB(4)    *-2
00020  0094  E718               ECR      A7,A6
00021  0096  1F01               SUK      A7,1
00022  0098  5E04               RB(6)    *-2
00023  009A  ED20               CWK      A5,/400
       009C  0400
00024  009E  5002               RF(0)    CONT
00025  00A0  207F               HLT                              STATUS ERROR SEE A5
00026  00A2  3C43        CONT   SRL      A4,3
00027  00A4  940C               ADR      A4,A3
00028  00A6  EC08               CWR      A4,A2
00029  00A8  5922               RB(1)    CIO
00030  00AA  5F22               RB       CIO1
00031
00032                           EJECT
00033                  *EXAMPLE
00034                  *FOR CERTAIN ADJUSTMENTS SEEK FROM 0 TO 64 IN LOOP
00035                  *LOAD THE REGISTERS AS FOLLOWS:
00036                  *        LOAD A1 WITH 0
00037                  *        LOAD A2 WITH 64 DEC = /40
00038                  *        LOAD A3 WITH 64 DEC = /40
00039                  *        LOAD A6 WITH  /40 ( MAX VALUE IN A6 = /80)
00040                  *                 (/40= 64 DEC IS ABOUT A DELAY OF 64 MSEC)
00041
00042                  *        LOAD START ADDRESS IN A0
00043                  *        PUSH  MC AND RUN
00044
00045                  *NOTE    WITH INST YOU CAN STOP THE PROGRAM AND IT IS
00046                  *        POSSIBLE TO CHANGE THE PARAMETERS, PUSH RUN AND
00047                  *        THE PROGRAM WILL RUN FOR THE CHANGED PARAMETERS
00048
00049                           END      START
```

```
00000                          IDENT    DISCTS                FOR P800
00001                    *PROGRAM FOR READING AND WRITING ON DISC
00002                    *PUT THE PATTERN YOU WANT READ AND WRITE IN A5, BEFORE RUNNING THE PROGRAM
00003                    *IF THE PROGRAM STOPS YOU FIND THE WRITTEN WORD IN A3 AND THE READ WORD IN A4
00004                    *IN A2 IS THE POSITION OF THE WORDS IN THE DATA BUFFERS
00005                    *AFTERWARDS YOU FIND THE STATUS IN A6.
00006                    *
00007                    *
00008                          AORG     /80
00009          0002      DA    EQU      /02                   DEVICE ADDR. DISC
00010          0004      ER1   EQU      /04                   FIRST EXTERNAL REGISTER
00011          0005      ER2   EQU      /05                   SECOND EXTERNAL REGISTER
00012                    *
00013                    *MAIN PROGRAM
00014   0080   FFFF            DATA     /FFFF
00015   0082   0000            DATA     0
00016   0084   207F     START  HLT
00017   0086   87A0            LDKL     A15,EOS               LOAD STACKPOINTER
        0088   0780
00018   008A   8120            LDKL     A1,INTROU             ADDR. INTERRUPTROUTINE
        008C   00F4
00019   008E   8141            ST       A1,/20
        0090   0020
00020   0092   0200     LOAD   LDK      A2,0
00021   0094   8549     STORE  ST       A5,DATAIN,A2          WRITE BUFFER
        0096   00FA
00022   0098   1202            ADK      A2,2
00023   009A   EA20            CWK      A2,/19A
        009C   019A
00024   009E   5C0C            RB(4)    STORE
00025   00A0   8120            LDKL     A1,/C0CD              WER CONTROL WORD 1
        00A2   C0CD
00026   00A4   7104            WER      A1,ER1
00027   00A6   8120            LDKL     A1,DATAIN             WER CONTROL WORD 2
        00A8   00FA
00028   00AA   7105            WER      A1,ER2
00029   00AC   0101            LDK      A1,1
00030   00AE   41C2            CIO      A1,1,DA               START WRITE
00031   00B0   5C04            RB(4)    *-2
00032   00B2   4F82     WAIT   TST      A7,DA
00033   00B4   EF20            CWK      A7,0
        00B6   0000
00034   00B8   5C08            RB(4)    WAIT
00035   00BA   8120            LDKL     A1,/80CD              WER CONTROL WORD 1
        00BC   80CD
00036   00BE   7104            WER      A1,ER1
00037   00C0   8120            LDKL     A1,DATAOT             WER CONTROL WORD 2
        00C2   043A
00038   00C4   7105            WER      A1,ER2
00039   00C6   0100            LDK      A1,0
00040   00C8   41C2            CIO      A1,1,DA               START READ
00041   00CA   5C04            RB(4)    *-2
00042   00CC   4F82     WAITAG TST      A7,DA
00043   00CE   EF20            CWK      A7,0
        00D0   0000
00044   00D2   5C08            RB(4)    WAITAG
00045   00D4   0200            LDK      A2,0
00046   00D6   8348     TEST   LD       A3,DATAIN,A2          COMPARE WRITE AND
        00D8   00FA
00047   00DA   8448            LD       A4,DATAOT,A2          READ BUFFER
        00DC   043A
00048   00DE   EB10            CWR      A3,A4                 OK?
00049   00E0   540C            RF(4)    HALT                  NO STOP
00050   00E2   1202            ADK      A2,2                  YES GO ON
00051   00E4   EA20            CWK      A2,/19A
        00E6   019A
00052   00E8   5C14            RB(4)    TEST
00053   00EA   8F20            ABL(7)   LOAD
        00EC   0092
00054   00EE   207F     HALT   HLT                            DATA ERROR
00055   00F0   8F20            ABL(7)   LOAD
        00F2   0092
00056                    *
00057                    *INTERRUPT ROUTINE
00058   00F4   4EC2     INTROU SST      A6,DA                 AFTERWARDS STATUS IN A6
00059   00F6   5C04            RB(4)    *-2
00060   00F8   F03E            RTN      A15
00061   00FA           DATAIN  RES      /1A0
00062   043A           DATAOT  RES      /1A0
00063   077A           STACK   RES      3
00064   0780           EOS     RES      1
00065                          END      START
```

```
          DATE  80-03-13          IDENT    DKPROG

00000                             IDENT    DKPROG
00001
00002                     *       THIS PROGRAM TESTS READING AND WRITING ON DISC IN
00003                     *       PROGRAMMED CHANNEL
00004
00005                     ****************TAKE OFF BREAKLINE*****************
00006
00007
00008                     *       LOAD WORD TO WRITE IN REGISTER A2
00009                     *       LOAD START ADDRESS (/0086) IN A0 AND PUSH RUN
00010
00011                             AORG     /80
00012
00013  0080  FFFF                 DATA     /FFFF
00014  0082  0000                 DATA     0
00015                     *       WRITE ROUTINE
00016
00017  0084  207F         START   HLT
00018  0086  20BF                 INH
00019  0088  0101                 LDK      A1,1                 WRITE COMMAND ON SECTOR ZERO
00020  008A  41C2                 CIO      A1,1,2               START CONTROLLER
00021  008C  4202                 OTR      A2,0,2               WRITE A2 CONTENTS ON DISC
00022  008E  5C04                 RB(4)    *-2
00023  0090  4182                 CIO      A1,0,2               STOP CONTROLLER
00024  0092  4CC2                 SST      A4,2                 GET STATUS
00025  0094  5C04                 RB(4)    *-2
00026  0096  207F                 HLT                           CHECK STATUS IN A4
00027                     *                                     SOMETIMES THROUGHPUT ERROR IS GIVEN
00028                     *                                     BECAUSE CIO HALT WAS JUST TO LATE
00029
00030
00031                     *       READ ROUTINE
00032  0098  20BF                 INH
00033  009A  0100                 LDK      A1,0                 READ COMMAND ON SECTOR ZERO
00034  009C  41C2                 CIO      A1,1,2               START CONTROLLER
00035  009E  4B02                 INR      A3,0,2               READ WORD
00036  00A0  5C04                 RB(4)    *-2
00037  00A2  4182                 CIO      A1,0,2               STOP CONTROLLER
00038  00A4  4CC2                 SST      A4,2                 GET STATUS
00039  00A6  5C04                 RB(4)    *-2
00040  00A8  207F                 HLT                           STATUS IN A4
00041                                                           READ WORD IN A3
00042  00AA  5F28                 RB       START
00043
00044
00045                             END      START
```

20 CARD READER/LINE PRINTER CONTROL UNIT P840-103 (CRLPZ)

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20.1 CRLPZ IDENTIFICATIONS

Typenumber : P840-103 (CRLPZ)
Testprogram : BCR1, for Card Reader P806-102
BLP1, for Line Printer P809-002 (X1415) or P809-004 (X1415)
I/O-channel : Card Reader, program channel or multiplex channel.
Break Connection : 1A05
Interrupt Connection: 1C05
: Line Printer, program channel or multiplex channel.
Break Connection : 1A04
Interrupt Connection: 1C04

Power Consumption : +5V, 1A

12NC number on the sticker on the board:

CRLPZ: 5111 199 7067X (5322 216 25318)

X = modification level

Devices : - Card Reader; Documation M300 (300 cards/min)
- Line Printer X 1415:
P809-002/31: LP-200 LPM, 5122 298 03500
Cable 5m 5111 199 70030

- Line Printer X1425:
P809-004/31: LP-400LPM 5122 298 04040
Cable 5m 5111 199 70030

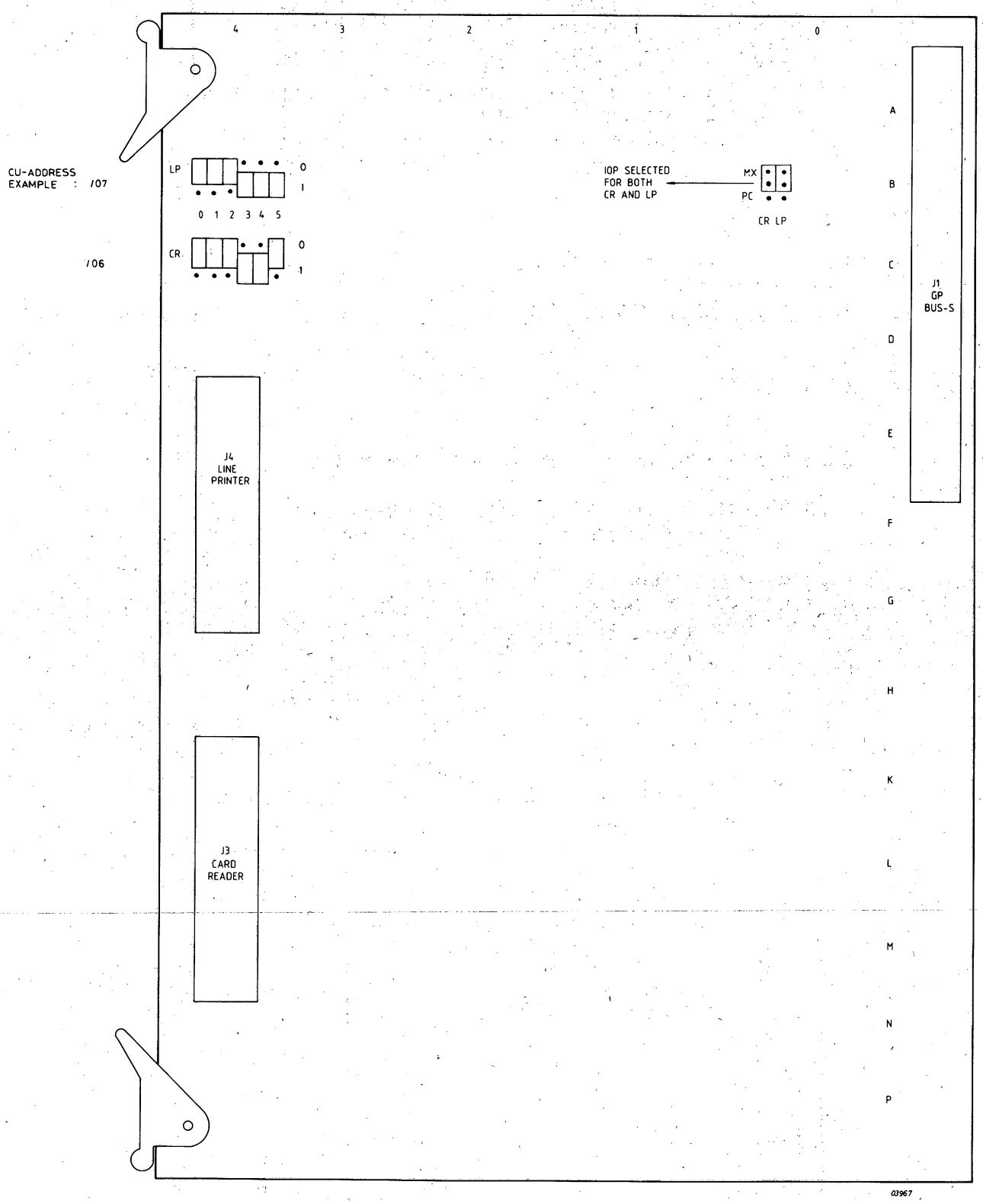


Figure 20.1 U-LINK SETTING

CU Signal	Interface Signal	CU Connector	CR Connector
FNP	IPFN	3J09	KK
FHESF	IHESFN	3J23	JJ
FCP	ICIRN	3J08	MM
FSTR	IDSN	3J06	AA
FERRN	ITRN	3J11	HH
POC	IRCN	3J13	LL
SBI007	ICL01N	3J01	D
SBI008	ICL02N	3J14	K
SBI009	ICL03N	3J02	L
SBI01Ø	ICL04N	3J15	M
SBI011	ICL05N	3J03	N
SBI012	ICL06N	3J16	U
SB1013	ICL07N	3J04	V
SBI014	ICL08N	3J17	Y
SBI015	ICL09N	3J19	Z
SBI006	ICL10N	3J20	C
SBI005	ICL11N	3J21	B
SBI004	ICL12N	3J22	A

Table 20.1 CARD READER INTERFACE (CONNECTOR J3)

Line Printer to CU Signals (all active high)

ONLINE The line printer is operable.
DEMAND The line printer requests a data word.

CU to Line Printer Signals (all active high)

DATA 1-7 7 Data bits to the device, derived from BI015-9N.
PI Paper Instruction bit: high if the Data bits are for a paper instruction; low if the Data bits are for a print character. Derived from BI08N.
STROBE Data Strobe validates the PI/DATA lines to the device.

CU Signal	Interface Signal	CU Connector	LP Connector
FONLN	ONLINE	4J03	y
FDEMN	DEMAND	4J01	E
STRLPN	STROBE	4J07	j
BI008	PI	4J22	p
BI009	DATA 7	4J10	n
BI010	DATA 6	4J23	Z
BI011	DATA 5	4J11	V
BI012	DATA 4	4J24	R
BI013	DATA 3	4J12	L
BI014	DATA 2	4J25	F
BI015	DATA 1	4J13	B

Table 20.2 LINE PRINTER INTERFACE (CONNECTOR J4)

USING DIFFERENT I.C.'s IN P450,X1150 OR P800 SYSTEM

Reader P.C. B.'s	IC location	IC used in P450, 1150	IC used in P800
clockcard (1)	C3	7416	7417
errorcard (2)	D6	7416	7417
synch. card (3)	-no-		
control card (6)	B3	7416	7417
	D4	7416	7417
	D6	7416	7417
	A4	7404 *	7417

* 7416 also possible

Interface P800 active low
Interface P450/X1150 active high

Table 20.3 DOCUMATION CARDREADER (M300) COMPATIBILITY

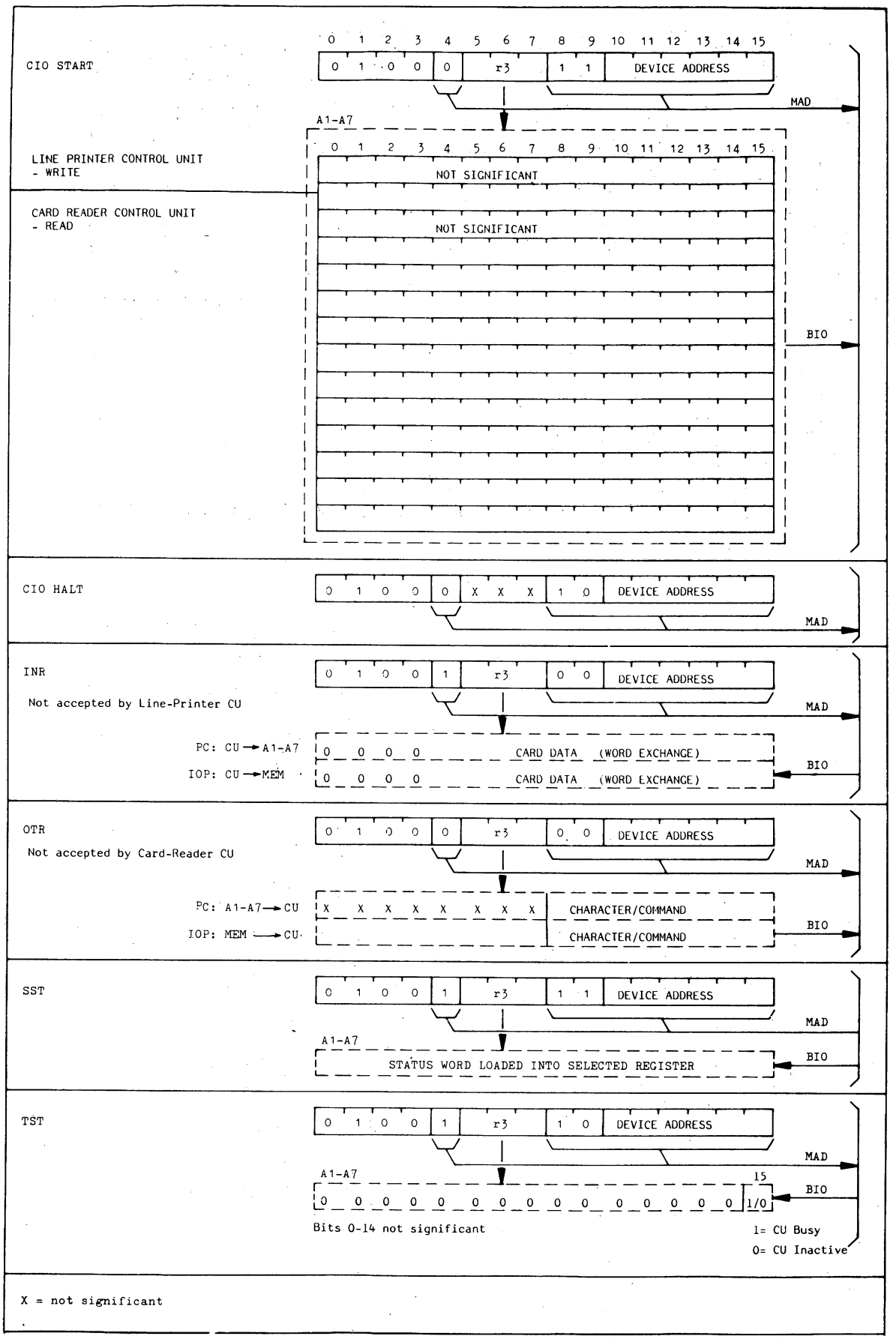


Figure 20.2 INSTRUCTION / COMMAND-WORD FORMATS

DATA and PRINT CONTROL CHARACTER CODE

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	PI	7	6	5	4	3	2	1

When the value of PI is 0 the other seven bits represent either a printable character or a format control character.

VERTICAL FORMAT CONTROL CODE

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	PI	7	6	5	4	3	2	1
Logic Value	1	1	X	0	0	Channel Number		

where --

- X is not significant.
- Channel Number indicates the channel number in the paper tape control loop.

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	PI	7	6	5	4	3	2	1
Logic Value	1	1	X	1	Number of Lines			

where --

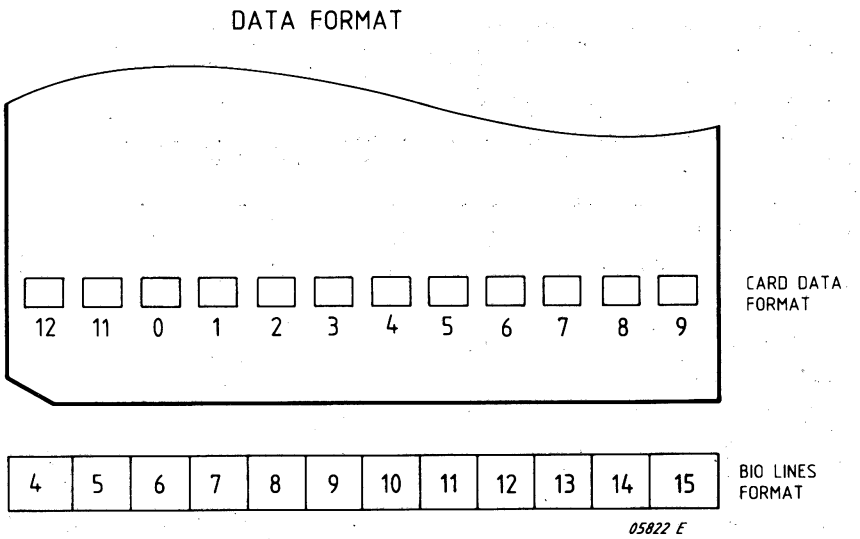
- X is not significant.
- Number of Lines indicates the number of lines to be skipped from 0 to 15.

Character Code

			b7	0	0	0	1	1
			b6	0	1	1	0	0
b4	b3	b2	b5 / b1	0	0	1	0	1
0	0	0	0		Space	Ø	@	P
0	0	0	1		!	1	A	Q
0	0	1	0		"	2	B	R
0	0	1	1		#	3	C	S
0	1	0	0		$	4	D	T
0	1	0	1		%	5	E	U
0	1	1	0		&	6	F	V
0	1	1	1		'	7	G	W
1	0	0	0		(	8	H	X
1	0	0	1		)	9	I	Y
1	0	1	0	PF	*	:	J	Z
1	0	1	1		+	;	K	[
1	1	0	0	FF	,	<	L	◇
1	1	0	1	CR	-	=	M	]
1	1	1	0		.	>	N	^
1	1	1	1		/	?	O	♡

- PF Paper Feed: advances the paper one line and prints buffer-contents
- FF Form Feed : advances the paper to the top of the next sheet of paper and prints the buffer-contents
- CR Carriage Return: prints buffer-contents

Figure 20.3 CONTROL AND CHARACTER CODES LINE PRINTER



Note: A hole is a "1".

Figure 20.4 CARD DATA FORMAT

20.4.1 STATUS WORD

LP-CU

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Not Operable

CR-CU

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0		0		0		

Not Operable
Throughput Error
Incorrect Length
Hopper Empty/ Stacker Full

NOT OPERABLE

Bit 15 is set:
- If the Line Printer is inoperable, due to Switched-off/ not On-Line or Paper-Fault.
- If Card Reader is inoperable, due to Switched-off/ not On-Line or Pick-error / Stacker Full / Hopper-Empty.

THROUGHPUT ERROR

Bit 14 is set:
- If a new character is read and the CPU/IOP did not yet answer the data-request Interrupt/Break.

INCORRECT LENGTH

Bit 12 is set:
- If the number of data exchanges by CPU or IOP differs from the number of characters on the card.

HOPPER EMPTY / STACKER FULL

Bit 10 is set:
- If either of these conditions is true.

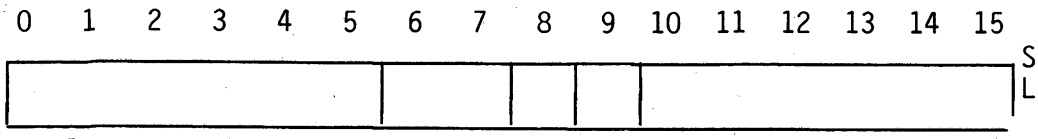
20.5 SHORT DESCRIPTION TESTPROGRAMS

TESTPROGRAM BLP1 4K

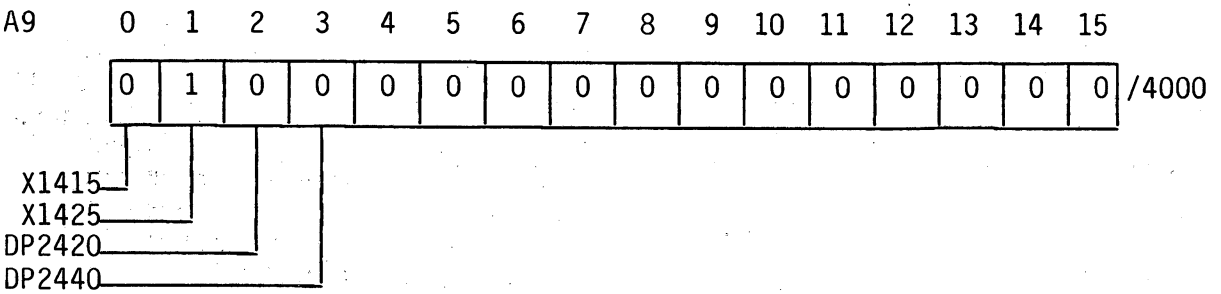
1. IPL
   Program stops at /700 (restart address and normal end).

2. Switch on RTC (PF/AR also possible) P851: after program runs.

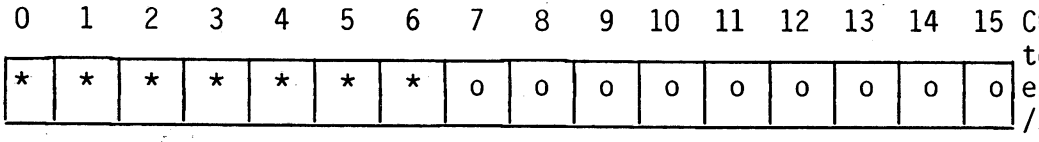
3. A8



A9



A10



* = Standard
o = Optional

Setting (X1415/25)

4. Depress MC, RUN

   Error stop at address /5F0
   Restart after power/off at /6EE
   Interrupts return to /700

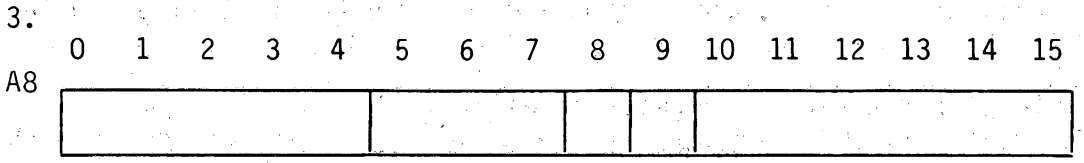
For more information see official description of testprogram.

TESTPROGRAM BCR1 4K

1. IPL
   Program stops at /700 (restart address and normal end).
   Set of special cards on the cardreader.

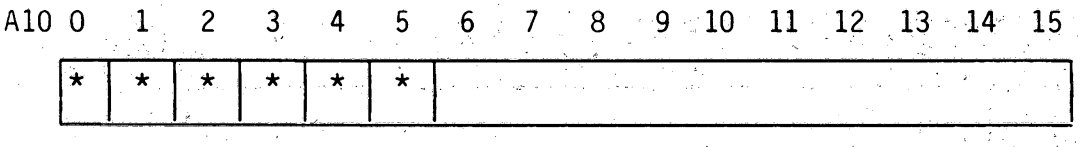
2. Switch on RTC (PF/AR also possible)

3.



Standard Levels:

/3006 /5406
Int. Levels:
/C- /15



Checks to be executed

* = Standard

4. Depress MC, RUN

   Error stop at /5F0
   Restart after power-off /6EE
   Interrupt returns to address /700

For more information see official description of testprogram.

20.6 SHORT ROUTINES

LINE PRINTER

This program is written for Programmed Channel operation so if the printer is normally used on the IOP Channel the CU must be connected to operate on the Programmed Channel. The program can be loaded either with the IPL routine or by hand using the switches on the control panel. Once loaded the following routine should be used:

- Load register A6 with the ASCII character to be printed.
- Load register A7 with number of times you want the character printed on each line.
- Load register A0 with the Start address.
- Push the RUN button.

To stop the program push the INST button.

Program LINELP

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	0200		LDK	A2,0
008A	4BC7		SST	A3,/07
008C	42C7		CIO	A2,1,/07
008E	5C04		RB(NA)	* -2
0090	050A	OUTLF	LDK	A5,/0A
0092	4507		OTR	A5,0,/07
0094	5C04		RB(NA)	* -2
0096	4607	OUTCH	OTR	A6,0,/07
0098	5C04		RB(NA)	* -2
009A	1201		ADK	A2,1
009C	EA1C		CWR	A2,A
009E	5C0A		RB(NE)	OUTCH
00A0	0200		LDK	A2,0
00A2	5F14		RB	OUTLF

```
        DATE  80-03-13          IDENT    LPIOP

00000                           IDENT    LPIOP
00001                   *
00002                   *
00003                   *       THIS PROGRAM STORES TWO SELECTED CHARACTERS INTO A BUFFER
00004                   *       THEN PRINTS THEM AND STOPS WAITING NEW CHARACTERS TO BE SELECTED
00005                   *
00006                   *
00007         0000      BEGIN   EQU      *
00008                           RORG     BEGIN+/80
00009                   *
00010                   *
00011                   *       LOAD THE TWO CHARACTERS TO BE PRINTED IN REGISTER A3
00012                   *
00013                   *       PUSH THE RUN BUTTON
00014                   *
00015   0080  FFFF              DATA     /FFFF
00016   0082  0000              DATA     0
00017   0084  207F      START   HLT
00018   0086  20BF              INH
00019   0088  850C              LDR      A5,A3                  LOAD DATA INTO A5
00020   008A  0100              LDK      A1,0                   CLEAR CHAR COUNTER
00021   008C  8545      REPT    ST       A5,LPBUF,A1            STORE THE CONTENTS OF A5 INTO LPBUF
        008E  00B8  R
00022   0090  1102              ADK      A1,2                   UPDATE LPBUF ADDRESS
00023   0092  E920              CWK      A1,78                  AND CHECK IF LINE FULL
        0094  004E
00024   0096  5C0C              RB(NE)   REPT
00025   0098  8520              LDKL     A5,/0D0A               LOAD CARRIAGE RETURN LINE FEED CHARS
        009A  0D0A
00026   009C  8545              ST       A5,LPBUF,A1            AND STORE IN LPBUF
        009E  00B8  R
00027   00A0  8120              LDKL     A1,/4050               LOAD PARAMS FOR FIRST WER
        00A2  4050
00028   00A4  710E              WER      A1,/E                  AND SEND TO IOP
00029   00A6  8120              LDKL     A1,LPBUF               LOAD FIRST ADDRESS OF LPBUF
        00A8  00B8  R
00030   00AA  710F              WER      A1,/F                  AND SEND TO IOP
00031   00AC  0600              LDK      A6,0
00032   00AE  46C7              CIO      A6,1,/7                SEND START COMMAND TO PRINTER
00033   00B0  5C04              RB(NA)   *-2                    TRY AGAIN IF NOT ACCEPTED
00034   00B2  4CC7              SST      A4,7                   GET STATUS
00035   00B4  5C04              RB(NA)   *-2
00036   00B6  5F34              RB       START                  GO AND WAIT FOR NEW DATA
00037                   *
00038   00B8            LPBUF   RES      80                     OUTPUT BUFFER
00039                           END      START
```

```
          DATE  82-05-05      IDENT    CRPROG


0000                          IDENT    CRPROG
0001                    *
0002                    *
0003                    *     THIS PROGRAM READS A CARD VIA THE PROGRAMMED CHANNEL AND STOPS SO THAT
0004                    *     CONTENTS OF THE BUFFER CAN BE CHECKED AGAINST THE PUNCHED HOLES IN THE
0005                    *     CARD
0006                    *
0007      0000          BEGIN   EQU      *
0008                          RORG     BEGIN+/80
0009                    *
0010                    *
0011                    *     LOAD THE CARD(S) TO BE READ INTO THE CARDREADER
0012                    *     AND START THE CARD READER
0013                    *
0014                    *     LOAD START ADDRESS(/0086) IN A0 AND PUSH THE RUN BUTTON
0015                    *
0016 0080 FFFF                DATA     /FFFF
0017 0082 0000                DATA     0
0018 0084 207F          START   HLT
0019 0086 20BF                INH
0020 0088 0200                LDK      A2,0                  LOAD ZERO IN A2
0021 008A 0100                LDK      A1,0                  CLEAR WORD COUNTER
0022 008C 8245 00B8 R   STORE   ST       A2,BUFF,A1            STORE ZERO INTO BUFF ADDRESS
0023 0090 1102                ADK      A1,2                  UPDATE WORD COUNT OF BUFF ADDRESS
0024 0092 E920 002A           CWK      A1,42                 CHECK IF LAST WORD IS REACHED
0025 0096 5C0C                RB(NE)   STORE                 NO? GO AND STORE THE NEXT WORD
0026 0098 0100                LDK      A1,0                  CLEAR CHARACTER COUNTER
0027 009A 0601                LDK      A6,1
0028 009C 46C6                CIO      A6,1,6                SEND CIO START COMMAND TO THE CARDREADER
0029 009E 5C04                RB(NA)   *-2
0030 00A0 4D06          READ    INR      A5,0,6                GET CHARACTER FROM CU
0031 00A2 5C04                RB(NA)   *-2
0032 00A4 8545 00B8 R         ST       A5,BUFF,A1            AND STORE IN BUFFER
0033 00A8 1102                ADK      A1,2                  UPDATE BUFFER ADDRESS
0034 00AA E920 00A0           CWK      A1,/A0                CHECK IF LAST COLUMN READ
0035 00AE 5C10                RB(NE)   READ                  NO? GO AND READ NEXT COLUMN
0036 00B0 4686                CIO      A6,0,6                SEND STOP COMMAND TO CU
0037 00B2 4CC6                SST      A4,6                  GET STATUS FROM CU
0038 00B4 5C04                RB(NA)   *-2
0039 00B6 5F34                RB       START                 GO AND WAIT FOR NEXT RUN
0040                    *
0041 00B8               BUFF    RES      42                    READ BUFFER
0042                          END      START


        SYMBOL TABLE

 BEGIN   0000  R   BUFF    00B8  R   READ    00A0  R   START   0084  R
 STORE   008C  R

        ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-10S-980MS-
```

CARD READER

This program is written to use the IOP channel. If the Card Reader normally operates on the Programmed Channel it will be necessary to connect the Break Request line on the CU. The program will read one card and stop; the data on the card can be checked by displaying the contents of the program buffer, BUFF. Once the program has been loaded either by the IPL routine or by hand using the control panel switches, it is only necessary to load the start address into register A0 and push the RUN button.

Program CRTEST

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	8120		LDKL	A1,/8050
008A	8050			
008C	710C		WER	A1,/0C
008E	8220		LDKI	A2,BUFF
0090	009E			
0092	720D		WER	A2,/0D
0094	43C6		CIO	A3,1,/06
0096	5C04		RB(NA	* -2
0098	4CC6		SST	A4,/06
009A	5C04		RB(NA)	* -2
009C	5F1A		RB	Start
009E		BUFF		

21 ASYNCHRONOUS SERIAL CONTROL UNIT FOR 4 LINES P845-145 (ASCU4Z)

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21.1 ASCU4Z INDENTIFICATIONS

Type Number	: P845-145
Function	: Control Unit for asynchronous data transfer for 4 lines and V24 or Current Loop interface.
Test program	: BASCU4
I/O Channel	: Program Channel (all lines) or Multiplex-Channel (only line 3 and 4)
Power consumption	: +5V 700mA +12V 40mA -12V 40mA
12 NC code (on sticker)	: 5111 199 6827X (5322 216 25316) X = modification level
Devices	: -MODEM: 4 lines half duplex 2 lines full duplex 2 lines full duplex + 1 line half duplex -Direct connection to VDU, V24 or Current Loop

21.2 FACILITIES

- Controls 4 lines, asynchronous characters.
- V24 or Current Loop interface.
- Data transfer: 4 Lines Half Duplex.
  2 Lines Full Duplex.
  1 Line Full Duplex + 2 Lines Half Duplex.
- Data transfer speed: 110 up to 9600 bits/sec.
- Selectable character length: 7 or 8 bits.
- Selectable parity bit (software).
- Selectable Echo Mode.
- Stop bits: 1 for reception, 2 for transmission.
- Detection of received characters, during transmission in half duplex.
- Ready for Receive (CT133) detection of peripheral.
- Break key detection on line 1, used for the Control Panel interrupt. (output on pin 1C04)
- Detection of Framing Error.
- 4 consecutive Device Addresses for each lines.

21.3 INSTALLATION DETAILS

21.3.1 STRAP SETTING

NAME STRAPS	NUMBER OF STRAPS	FUNCTIONS OF STRAPS	SETTING OF STRAPS
ADA	4	Selection Control Unit Address	See figure 21.1
RD MX/PC	3 per line 1 per line	Selection Configuration	See table 21.2 Link pos. MX (=IOP connection) may only be selected if ASCU4Z has a basic address related to the IOP nr.
RD CL 3	3 per line 1 per line	Selection V24/V28, Current Loop - Selection V24/28 - Selection Current Loop - Selection Current Loop (External Power Supply)	See figure 21.1 Links RD pos. V28 Links CL3 pos. V28 Links RD pos. CL Links CLs pos. V28 Links RD pos. CL Links CL3 pos. EX
CPTR	4 per line	Selection Data transmission / reception speed	See figure 21.1
WL	1 per line	Selection character length	See figure 21.1
BD	1 per line	Break detection option	See figure 21.1 Only for half duplex
ECHO	1 per line	Echo option	See figure 21.1 Only for half duplex
ITV	1	Factory Test Facilities	Must be in position as shown in figure 21.1
EXC1/TF TRCP	1 1 per line		
ITR	1	Factory Test Facilities	Links are hard wired must not be disconnected
ALE ROM SID	1 1 1		
CT133	1 per line	Device Ready (PER 3100)	See figure 21.1

Table 21.1 CHECK LIST STRAPS

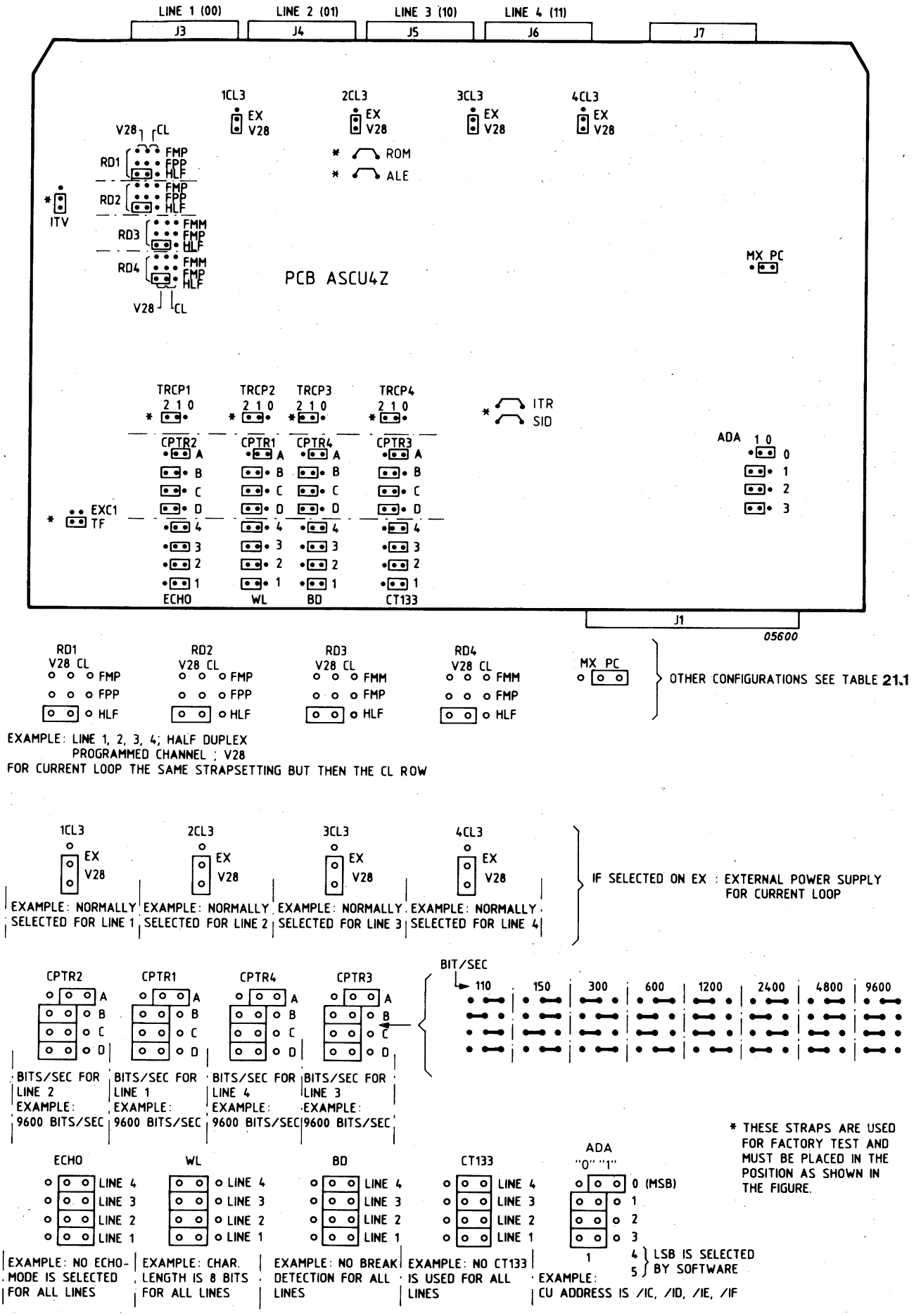


Figure 21.1 STRAP SETTING ASCU4Z

Description of the Configuration (V28)	STRAP SETTING
Line 1,2,3,4;Half duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 1,2 ;Half duplex; Programmed Channel Line 3,4 ;Half duplex; Multiplex Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 2,4 ;Full duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 3,4 ;Full duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 2 ;Full duplex; Programmed Channel Line 4 ;Full duplex; Multiplex Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 3,4 ;Full duplex; Multiplex Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 3,4 ;Half duplex; Programmed Channel Line 2 ;Full duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 1,2 ;Half duplex; Programmed Channel Line 4 ;Full duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 2,4 ;Half duplex; Programmed Channel Line 3 ;Full duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 1,3 ;Full duplex; Programmed Channel Line 4 ;Full duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .

Table 21.2 CONFIGURATION SELECTION

Line 1,2 Line 4	;Half duplex; Programmed Channel ;Full duplex; Multiplex Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 3,4 Line 2	;Half duplex; Multiplex Channel ;Full duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 2 Line 4 Line 3	;Half duplex; Programmed Channel ;Half duplex; Multiplex Channel ;Full duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .
Line 1 Line 3 Line 4	;Half duplex; Programmed Channel ;Half duplex; Multiplex Channel ;Full duplex; Programmed Channel	RD1 RD2 RD3 RD4 Mx PC . . . .

Note: - The line-address for the HSI is: Line 1 = '00'
Line 2 = '01'
Line 3 = '10'
Line 4 = '11'

- When a Full duplex configuration is selected, the output and input channels of one line have separate line - addresses: - output = line number
  - input = lowest not occupied line number

  Example: line 2 = Full duplex: - output = '01'
  (see figure 21.2) - input = '00'
- If current loop is used, all RD straps must be in the position CL (one place to the right)

Table 21.2 CONFIGURATION SELECTION (CONT'D)

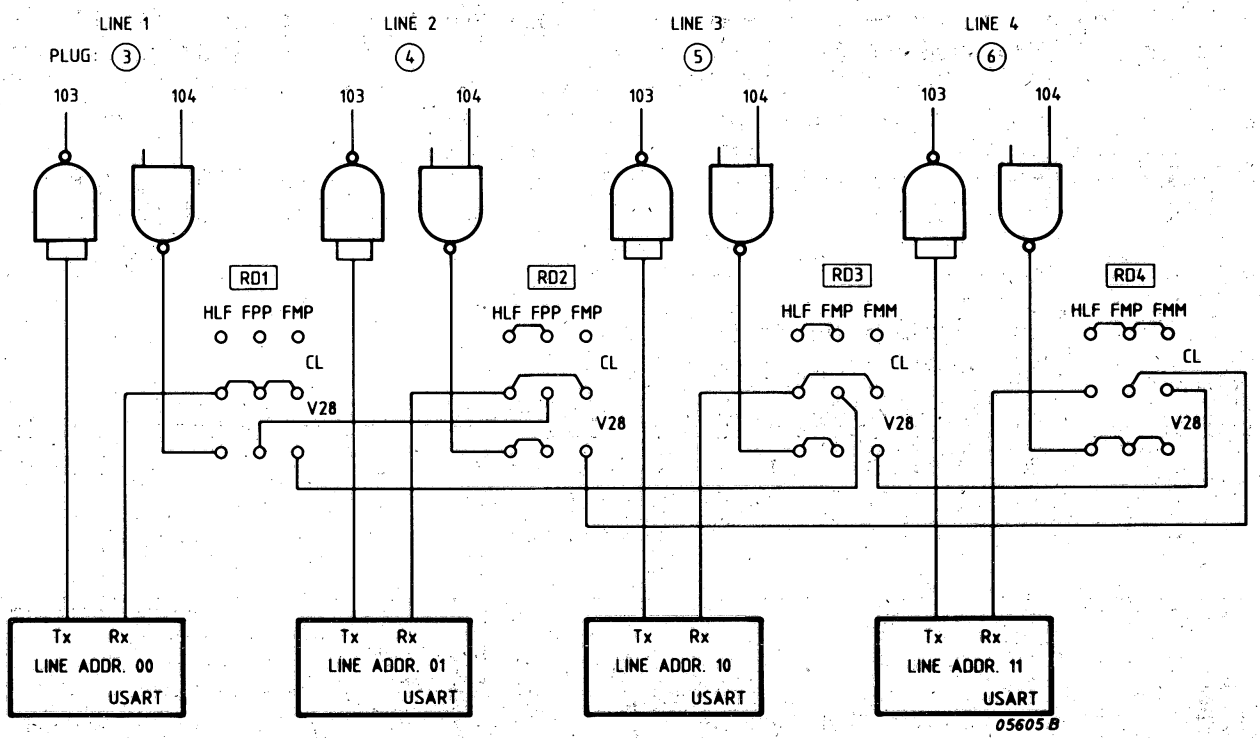


Figure 21.2 LAYOUT OF CONFIGURATION STRAPS RD

13.3.2 INTERRUPT AND BREAK WIRING

Wiring of the interrupts:

- Data and status interrupt : 1C05 to CPU
- Break Key detection interrupt (Control Panel int.) : 1C04 to CPU
- Reset Break Key Interrupt : 1C03 to CPU

Wiring of the breaks for the IOP:

- Break of line 3 (address "10") : 1A05 to IOP
- Break of line 4 (address "11") : 1A04 to IOP

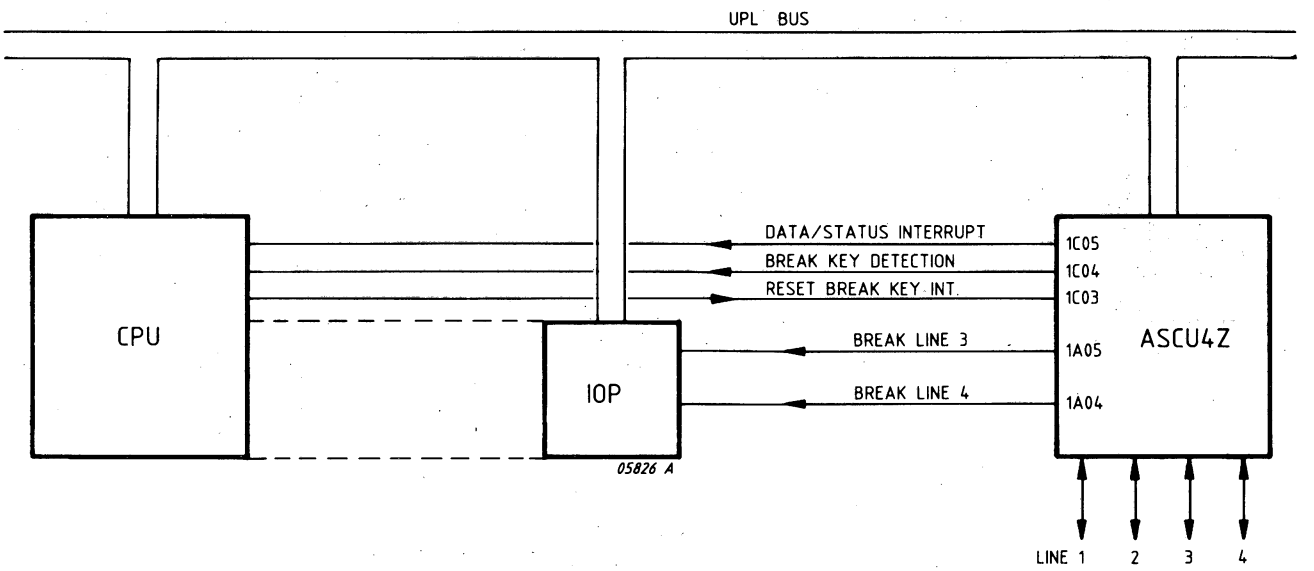


Figure 21.3 INTERRUPT AND BREAK WIRING

21.4 INTERFACE CONNECTIONS

- V24 Interconnections
- Current Loop Interconnections
- Cables (Asynchronous mode)
- Connector for an external current supply: J7

21.4.1 V24 INTERFACE:

Interconnections between ASCU4Z and the peripheral is with a V24/V28 cable

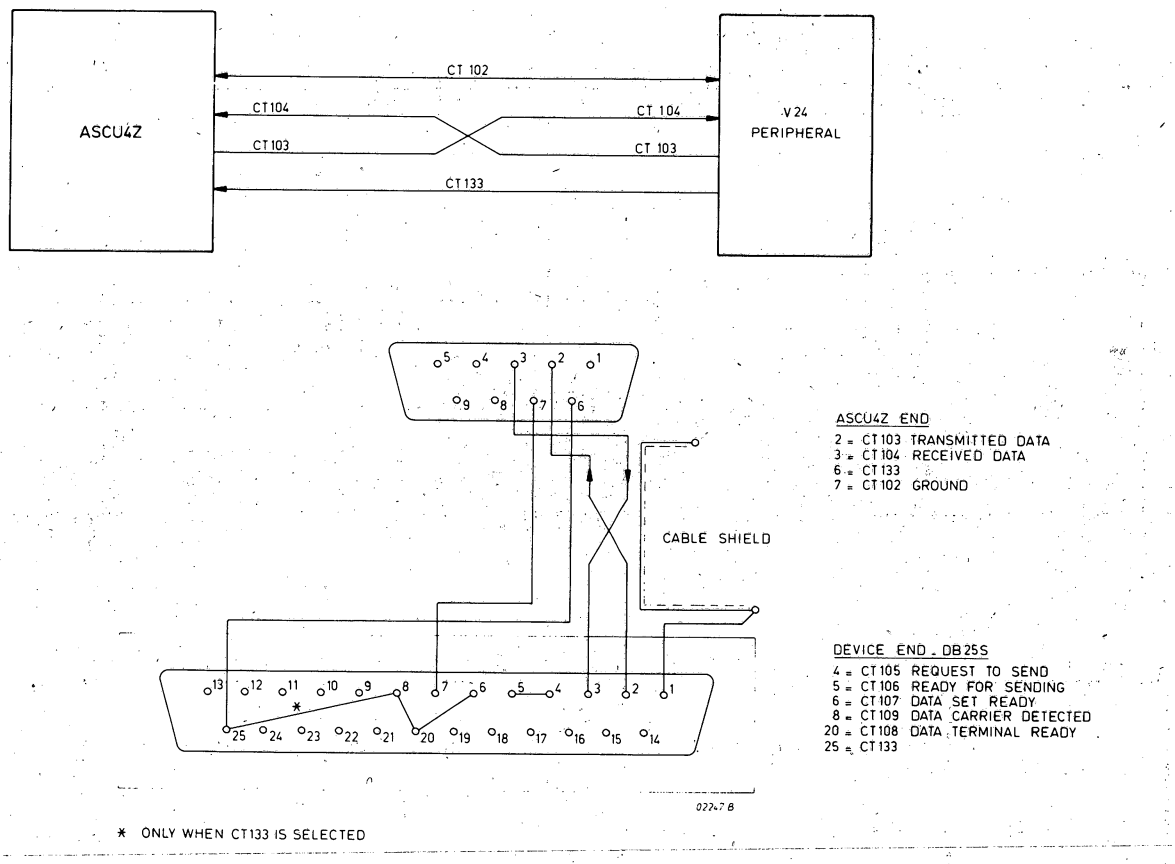
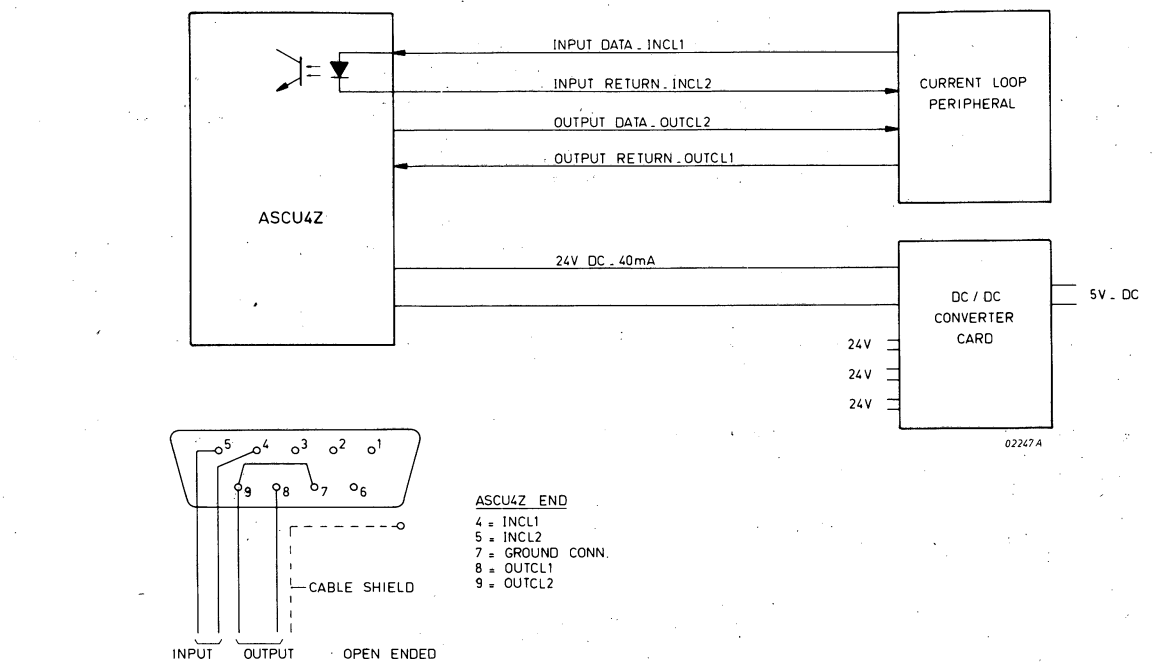


Figure 21.4 V24 INTERCONNECTIONS

21.4.2 CURRENT LOOP INTERFACE

Interconnections between ASCU4Z and the Current Loop Peripheral is with a Current Loop Cable.



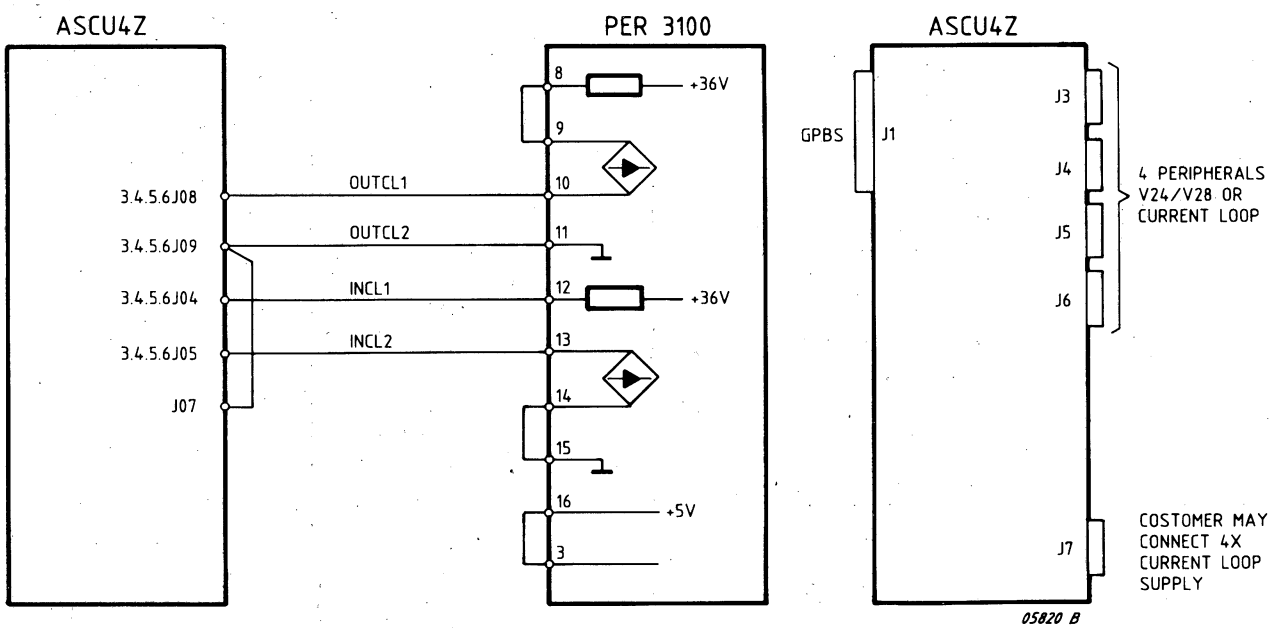


Figure 21.5 CURRENT LOOP INTERCONNECTIONS

21.4.3 CABLES

In the catalogue a maximum length of 100 m is mentioned for 9600 bps. For different transfer rates the following list may be an aid.

INTERFACE	V 28	CURRENT LOOP	
Cables	A	A	B
600 Bds	250 M	1 300 M	2 500 M
1 200 Bds	200 M	1 000 M	2 000 M
2 400 Bds	180 M	900 M	1 800 M
4 800 Bds	160 M	750 M	1 500 M
9 600 Bds	120 M	600 M	800 M

Table 21.3 CABLE LENGTHS

Cables: The following characteristics correspond to the standard cables used:
A = 243 Ohm/KM
110 pF/M between a pair
150 pF/M between a pair and ground
B = CMC04 46 Ohm/KM
20 pF/M between two conductors
130 pF/M between a conductor and ground

21.4.4 EXTERNAL CURRENT SUPPLY

For the purpose to insert a current supply into a current loop interface, it is possible to use an external power supply (24V, DC, 40m A per line).

Connector for an external current supply:

Pin Number	Inputs	Direction
7 J01	+V	Line 0
7 J02	Ground	
7 J03	+V	Line 1
7 J04	Ground	
7 J05	+V	Line 2
7 J06	Ground	
7 J07	+V	Line 3
7 J08	Ground	

Note: When an external power supply is used, the "U" links 1CL3, 2CL3, 3CL3, 4CL3 must have the position EX.

Table 21.4 CONNECTOR J7

CARD CONNECTORS				PERIPHERAL CONNECT	SIGNAL NAME	FUNCTION
3J07	4J07	5J07	6J07	07	CT 102	Command Retun (ground conn.)
3J02	4J02	5J02	6J02	02	CT 103	Transmitted Data
3J03	4J03	5J03	6J03	03	CT 104	Received Data
3J06	4J06	5J06	6J06	25	CT 133	Peripheral Ready to send or receive the next character

Table 21.5 CONNECTOR J3, 4, 5, 6 (V24 interface)

CARD CONNECTORS				PERIPHERAL CONNECT	SIGNAL NAME	FUNCTION
3J04	4J04	5J04	6J04	12	INCL1	Incoming data
3J05	4J05	5J05	6J05	13	INCL2	Incoming data
3J08	4J08	5J08	6J08	10	OUTCL1	Outgoing Data
3J09	4J09	5J09	6J09	11	OUTCL2	Outgoing Data

Table 21.6 CONNECTOR J3, 4, 5, 6 (Currentloop)

APPLICATION NOTES (Figure 21.6 and 21.7)

AFCU4Z may be used in V24 or Current Loop configurations. Two configuration examples are given in the following figures, these are:

- Current Loop, ASCU4Z/ASCU4Z Connection
- Current Loop, ASCU4Z/AMA8C Connection

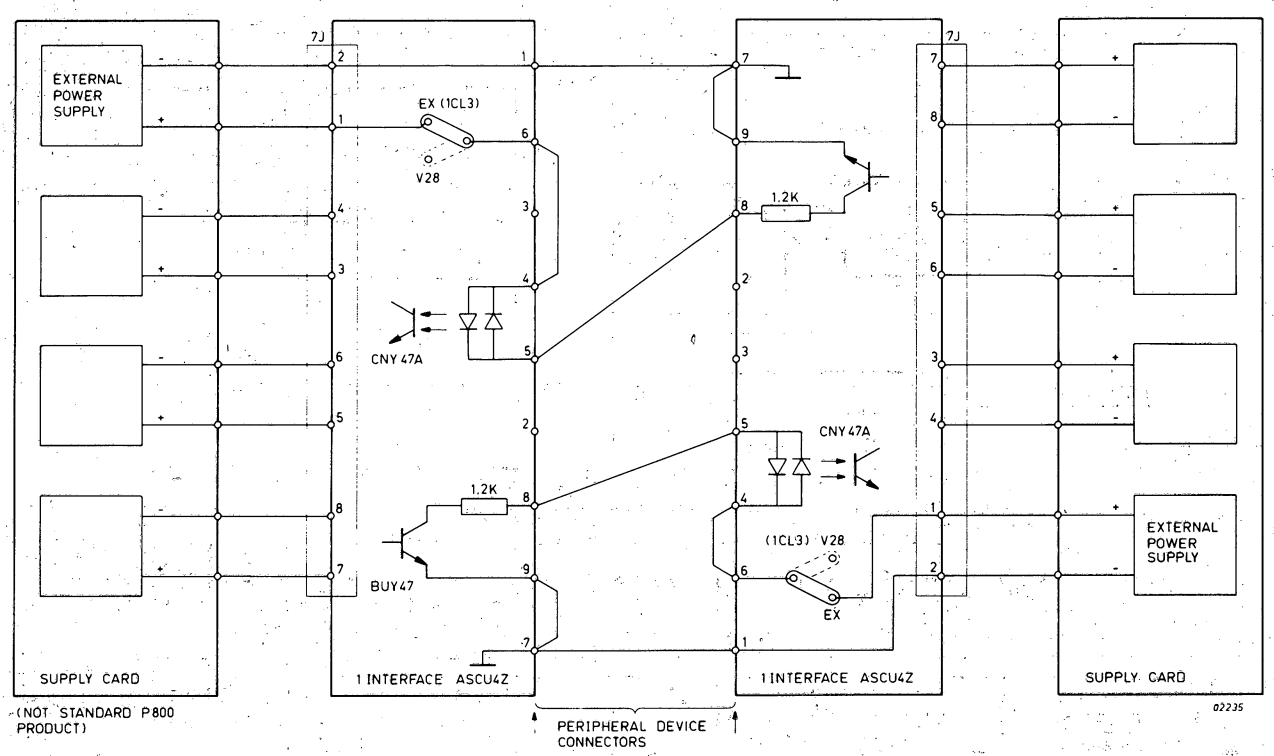


Figure 21.6 ASCU4Z/ASCU4Z, CURRENT LOOP

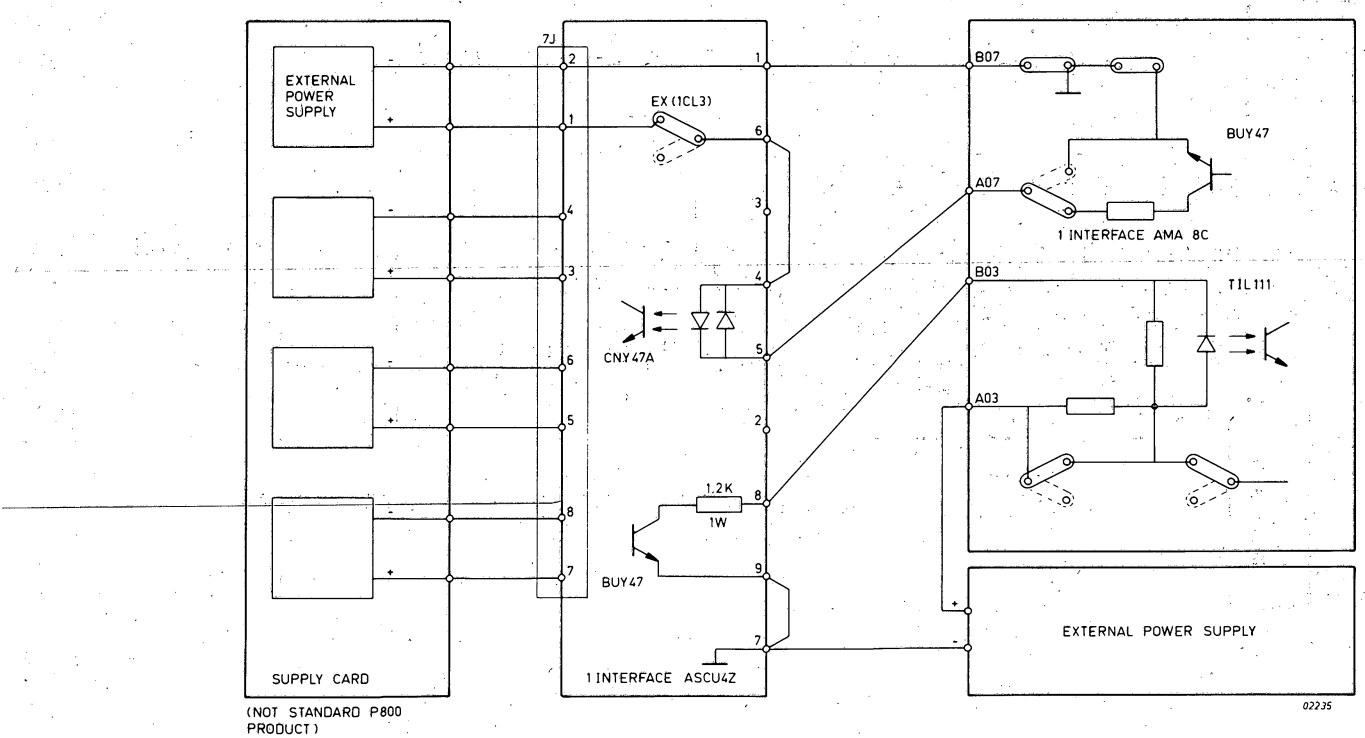


Figure 21.7 ASCU4Z/AMA8C, CURRENT LOOP

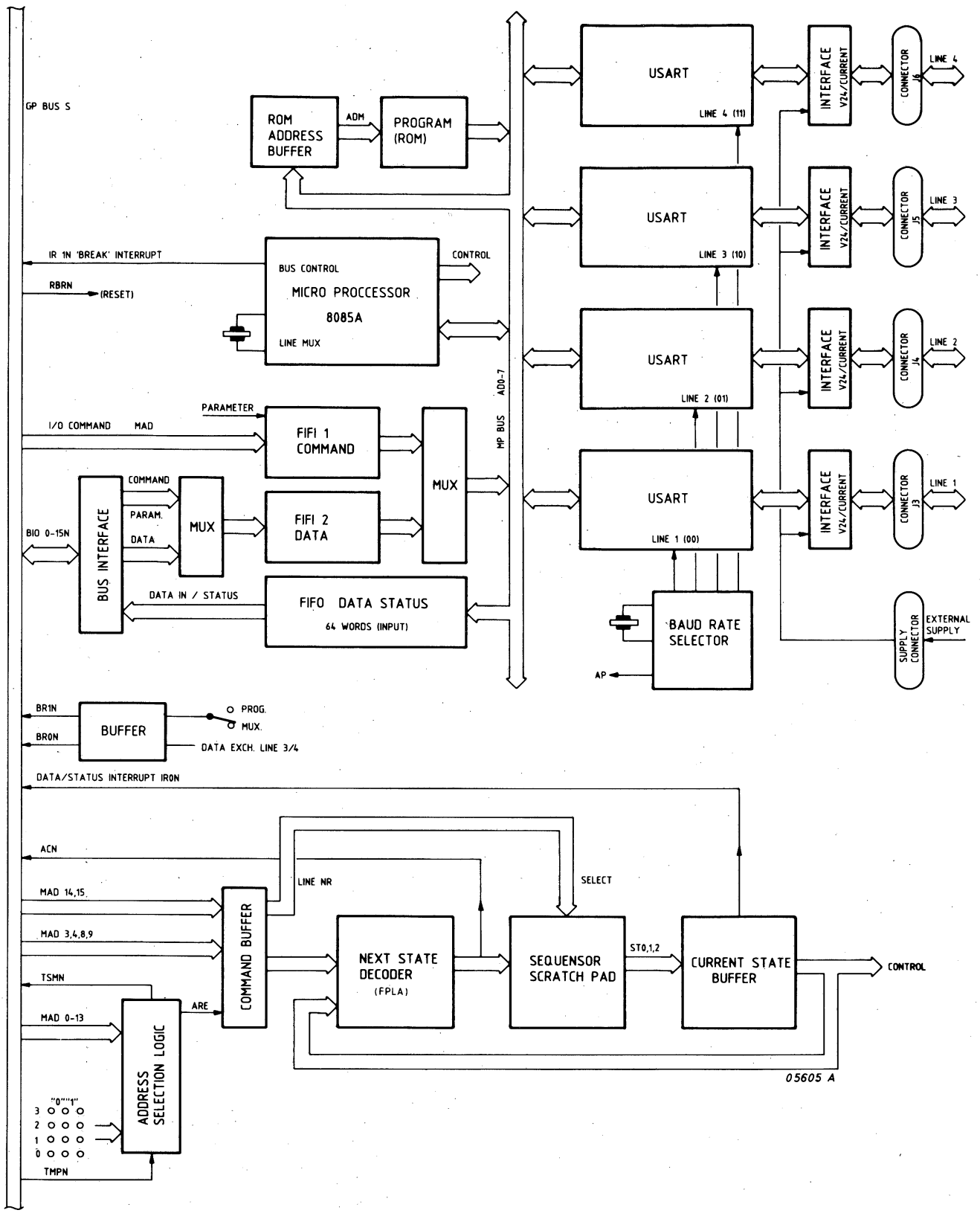


Figure 21.8 BLOCKDIAGRAM ASCU4Z

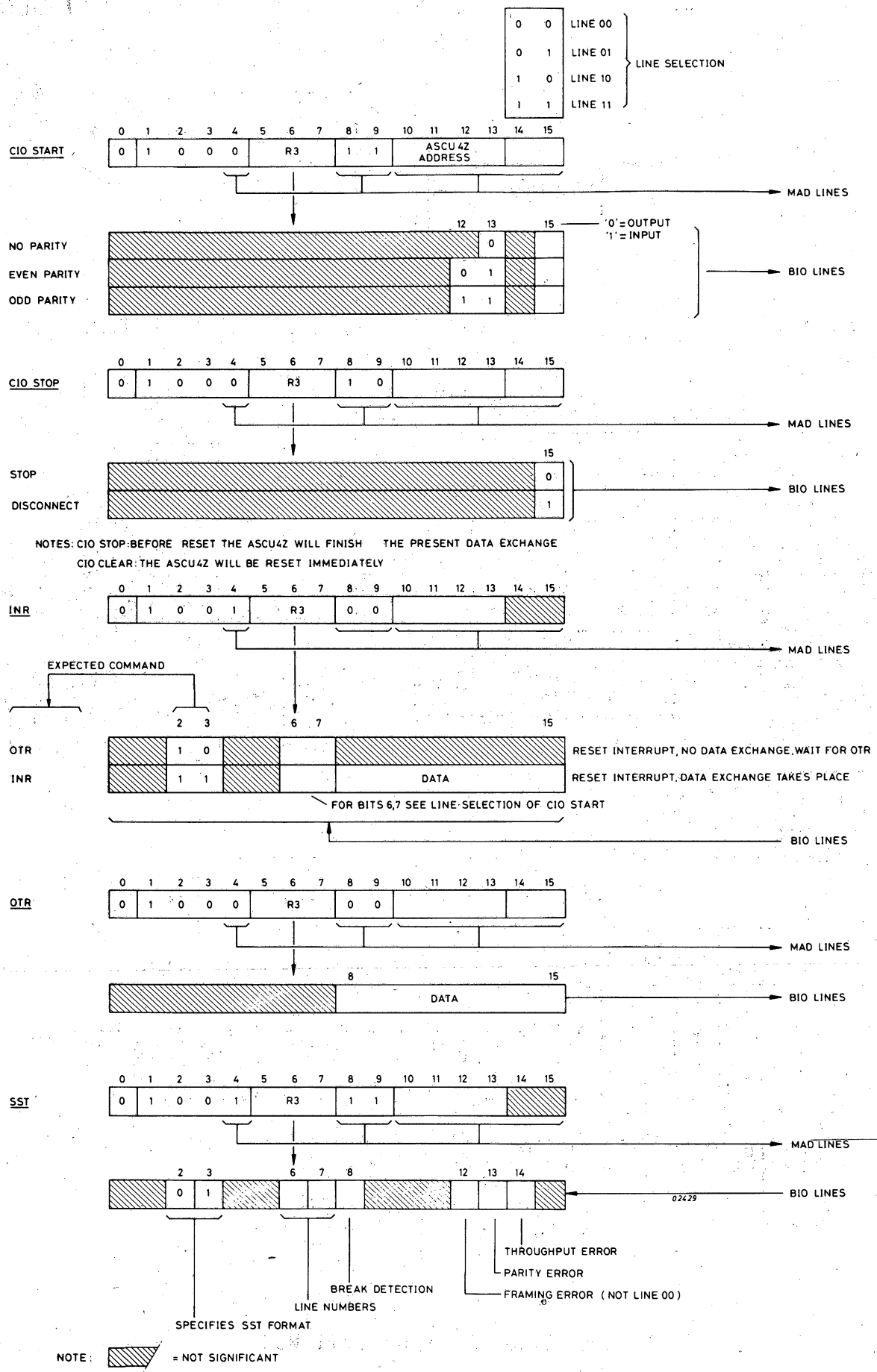
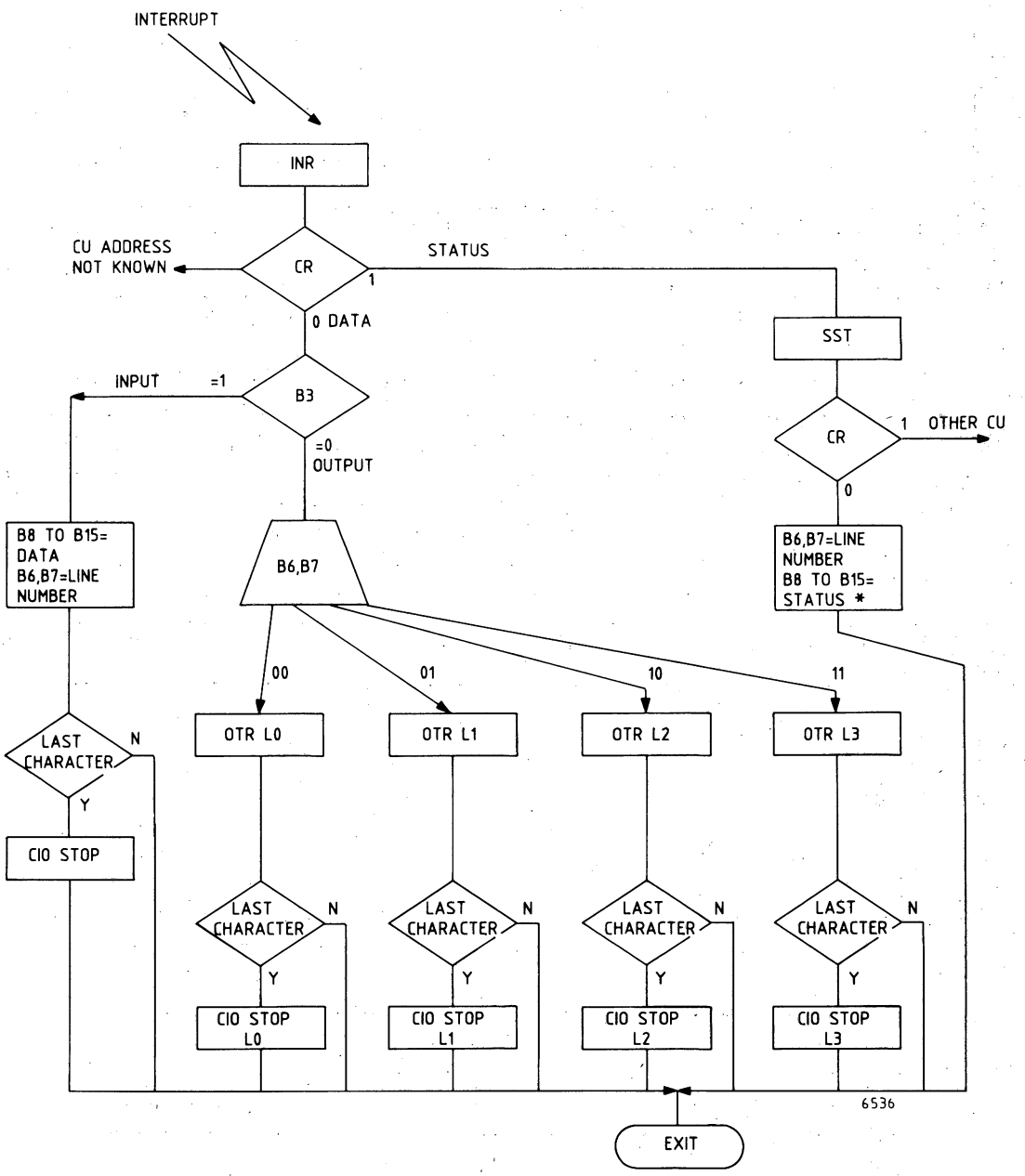


Figure 21.9 COMMANDS ASCU4Z



* STATUS , TROUGHPUT ERROR , PARITY ERROR , BREAK DETECTION , FRAMING ERROR

Figure 21.10 PROGRAMMING FLOWCHART

21.7 SHORT DESCRIPTION OF TESTPROGRAM

TESTPROGRAM BASCU4Z:

- Settings: HLF on RD 1,2,3,4 prog.channel no CT133
  non-echo no BD 8 bits data

Procedure:

- IPL
  Program displays /7ØØ
  Modify registers

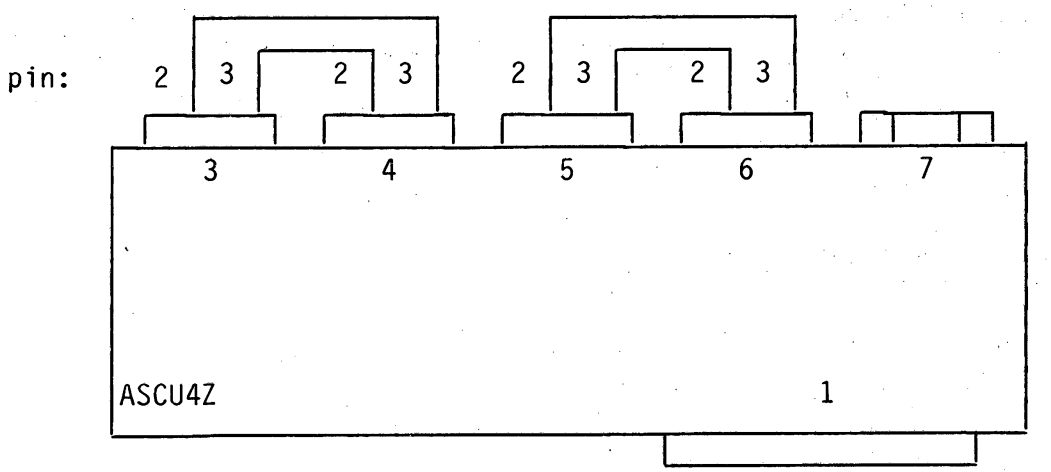
	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A8:	Ø	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	1	1	Ø	Ø	/2Ø1C
	Int. level										Dev. address						
	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A9:	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	/ØØØØ CTW
										Progr. control							/ØØ1Ø HHP
	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A10:	1	Ø	1	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	/BØØØ

1 = Tests selected

Start program

Display /5EØ = information stop
Display /5FØ = error stop
The error code is displayed. After error: reload the program, before retry.

Interconnect



Information Messages

IFØXYZ

X = check no.
Y = phase no.
Z = type of info

Hnfo Type	Meaning
Ø	Change strap position
1	-
2	-
3	Parity error
4	Framing error
5	-
6	Throughput error
7	-
8	Put ground on pin
9	Break key detected
A	Wait for 64 data input
B	Break detect
C	-
D	-
E	-
F	-

Program checks - Standard

Check ØØØ - Address recognition 4 lines
ØØ - Check data exchange PC
2ØØ - Check data exchange 4 lines simult. PC
3ØØ - Check on parity error
4ØØ - Check echo and break detection
5ØØ - Check data exchange - MX

Program checks - Special

Check 6ØØ - Check full duplex
7ØØ - Check interrupt break key line Ø and framing error lines 1,2,3
8ØØ - Check throughput error

ERØXY2

X = check nr.
Y = phase nr.
Z = error type

Error Type	Meaning
Ø	I/O instruction rejected
1	Break key not detected (line Ø)
2	Address not recognised
3	Parity error
4	Framing error
5	Incorrect length
6	Throughput error
7	Contents of SST incorrect
8	Data error
9	Hardware failure
A	Throughput error not detected
B	Break detection
C	Framing not detected

Procedure 5111 991 1ØØ91 = Procedure BASCU4 5111 991 11161
with addendum PTS8ØØØ 5111 991 11381
Listing 5111 991 11Ø81
Program 5111 199 65671

```
                        IDENT    ASCU
                      * THIS PROGRAM TRANSMITS AND RECEIVES CHAR 'U' CONTINUOUSLY
                      * LINE 1 FULL DUPLEX(LINE 00=REC. LINE 01=TRX)
                      * INT LEVEL 8 , DA /1C
                      * INTERCONNECT ON TRX-CU (LINE 01) PIN 4J02 TO REC-CU 00 PIN 4J03
                      *TEST CORRECT RUNNING: CHECK IF A3=/55
                      * (STOP PROGRAM BY CHANGING ADDR /D0 DATA (WAS:/EA0C) IN /207F (=HLT)
                      *           ---- OR -----
                      * CHECK OSCILLOSCOPE PICTURE CT103 ON PIN 4J02
                      *
                      *      +12V    I---I   I---I   I---I   I---I   I---I STOPBITS
                      *      -12V  --I   I---I   I---I   I---I   I---I   I---I---I-
                      *               ST   1   0   1   0   1   0   1   P
                      *                  I----------CHAR 'U'---------I PE
                      *
                      *  ERROR: DATA FAULT-STOP IN /DE (/E0 ON HHP)
                      *         STATUS FAULT-STOP IN /DC (/DE ON HHP)
                      *
                      *  TEST OF LINE 10/11: CHANGE DA'S IN PROGRAM, USE CONNECTOR J6
                      *
                      *
0000                            RES     /40
     001C             DA        EQU     /1C
0080 FFFF             DATA      DATA    /FFFF
0082 0000                       DATA    0
                      *
                      *  MAIN PROGRAM
0084 207F             START     HLT
0086 87A0                       LDKL    A15,/120              LOAD STACKPOINTER
0088 0120
008A 8120                       LDKL    A1,INTAD
008C 00A4  R
008E 8141                       ST      A1,/10                STORE INT ROUTINE ADDRESS
0090 0010
0092 0404                       LDK     A4,4                  EVEN PARITY,OUT
0094 0505                       LDK     A5,5                  EVEN PARITY,IN
0096 0255                       LDK     A2,/55                CHAR 'U'.
0098 2840                       ENB
009A 45DC                       CIO     A5,1,DA               START INPUT LINE 00
009C 5C04                       RB(4)   *-2
009E 44DD                       CIO     A4,1,DA+1             START OUTPUT LINE 01
00A0 5C04                       RB(4)   *-2
00A2 5F02                       RB      *
                      *
                      *  INTERRUPT ROUTINE
00A4 481C             INTAD     INR     A3,0,DA
00A6 8C20                       ABL(4)  STATUS
00A8 00D8  R
00AA 840C                       LDR     A4,A3
00AC 850C                       LDR     A5,A3
00AE A420                       ANKL    A4,/1000              CHECK: INPUT OR OUTPUT
00B0 1000
00B2 8C20                       ABL(4)  INPUT
00B4 00CC  R
                      *
00B6 A520             OUTPUT    ANKL    A5,/300               LOOK FOR LINENO.
00B8 0300
00BA 3068                       SRL     A5,8                  SHIFT RIGHT LINENO.
00BC 8420                       LDKL    A4,DA+/4200           /42DA=OTR A2,0,DA
00BE 421C
00C0 9414                       ADR     A4,A5                 ADD OTR AND LINENO.
00C2 8441                       ST      A4,OTR                STORE OTR
00C4 00C6  R
00C6 5700             OTR       RF      *+2                   REPLACED BY OTR
00C8 5C04                       RB(4)   *-2
00CA F03E                       RTN     A15
                      *
00CC A320             INPUT     ANKL    A3,/FF
00CE 00FF
00D0 EA0C                       CWR     A2,A3                 COMPARE OUTPUT AND INPUT DATA
00D2 8C20                       ABL(4)  ERR                   INPUT DIFFERENT FROM OUTPUT
00D4 00DE  R
00D6 F03E                       RTN     A15
                      *
                      *
00D8 4CDC             STATUS    SST     A4,DA
00DA 5C04                       RB(4)   *-2
00DC 207F                       HLT
00DE 207F             ERR       HLT
                                END     START
```

```
00000                          IDENT    ASCU2
00001                      *SHORT ROUTINE FOR INPUT AND OUTPUT ON ASCU4Z CARD
00002                      *
00003                      * PARAMETERS TO ENTER AFTER PROGRAM LOADING ONLY:
00004                      *
00005                      *                        INT LEVEL,PARITY,DEV.ADDR./LINE :PARITY: NO EVEN ODD
00006                      *          REG BITS:    0  TO   5, 6&7  ,   10   TO  15  BIT 6,7=00  01   11
00007                      *
00008                      *  REG  A1 (INPUT LINE) : E.G. /2004 = INT. LEV. 8, NO PARITY, DA /04
00009                      *  REG  A2 (OUTPUT LINE): E.G. /2005 = INT. LEV. 8, NO PARITY, DA /05
00010                      *
00011                      *
00012  0000                        RES      /40
00013  0080  FFFF                  DATA     /FFFF
00014  0082  0000                  DATA     0
00015  0084  87A0          START   LDKL     A15,500                STACKPOINTER
       0086  01F4
00016  0088  8120                  LDKL     A1,/2004               INT LEV 8, DA 04
       008A  2004
00017  008C  8220                  LDKL     A2,/2005               INT LEV 8, DA 1C, LINE 01
       008E  2005
00018  0090  207F                  HLT
00019                      ****PREPARE INPUT ROUTINE****
00020  0092  043F                  LDK      A4,/3F                 MASK DEV. ADDR.
00021  0094  A404                  ANR      A4,A1                  A4= DEV. ADDR.
00022  0096  AC41                  ORS      A4,CIOIS               MODIFY THE IO INSTRUCTIONS
       0098  0100  R
00023  009A  AC41                  ORS      A4,CIOIH
       009C  015C  R
00024  009E  AC41                  ORS      A4,INRI
       00A0  012C  R
00025  00A2  AC41                  ORS      A4,SSTI
       00A4  0160  R
00026  00A6  9410                  ADR      A4,A4                  SHIFT LEFT ONE BIT POS.
00027  00A8  AC41                  ORS      A4,WER1IN
       00AA  00F6  R
00028  00AC  AC41                  ORS      A4,WER2IN
       00AE  00FC  R
00029                      ****PREPARE OUTPUT ROUTINE****
00030  00B0  043F                  LDK      A4,/3F                 MASK DEV. ADDR.
00031  00B2  A408                  ANR      A4,A2                  A4= DEV ADDR. OUTPUT
00032  00B4  AC41                  ORS      A4,CIOOS               MODIFY THE IO INSTR.
       00B6  0120  R
00033  00B8  AC41                  ORS      A4,CIOOH
       00BA  0150  R
00034  00BC  AC41                  ORS      A4,INRO
       00BE  0132  R
00035  00C0  AC41                  ORS      A4,OTR
       00C2  0144  R
00036  00C4  AC41                  ORS      A4,SSTO
       00C6  0166  R
00037  00C8  9410                  ADR      A4,A4                  SHIFT LEFT ONE BIT POS.
00038  00CA  AC41                  ORS      A4,WER1OU
       00CC  0116  R
00039  00CE  AC41                  ORS      A4,WER2OU
       00D0  011C  R
00040                      ****PREPARE INT. ROUTINE ADDRESSES****
00041  00D2  8404                  LDR      A4,A1
00042  00D4  3C6A                  SRL      A4,10
00043  00D6  9410                  ADR      A4,A4                  A4 = INT ENTRY ADDR.
00044  00D8  8320                  LDKL     A3,INRI
       00DA  012C  R
00045  00DC  8331                  STR      A3,A4                  INTERRUPT ROUTINE ADDR
00046  00DE  8408                  LDR      A4,A2
00047  00E0  3C6A                  SRL      A4,10
00048  00E2  9410                  ADR      A4,A4                  A4 = INT ENTRY ADDR.
00049  00E4  8320                  LDKL     A3,INRO
       00E6  0132  R
00050  00E8  8331                  STR      A3,A4                  INTERRUPT ROUTINE ADDR.
00051  00EA  2840                  ENB
00052                      ****START INPUT LINE****
00053  00EC  8504          AGAIN   LDR      A5,A1
00054  00EE  3D66                  SRL      A5,6
00055  00F0  250C                  ANK      A5,/C                  PARITY PARAMETERS
00056  00F2  1501                  ADK      A5,1                   INPUT COMMAND
00057  00F4  0401                  LDK      A4,1                   INPUT,CHAR.MODE,BL=1
00058  00F6  7400          WER1IN  WER      A4,0
00059  00F8  8420                  LDKL     A4,BUF+1               DATA ADDRESS
       00FA  017F  R
00060  00FC  7401          WER2IN  WER      A4,1
00061  00FE  0400                  LDK      A4,0                   FLAG:SSTI ACCEPTED
00062  0100  45C0          CIOIS   CIO      A5,1,0
00063  0102  5C04                  RB(NA)   *-2
00064  0104  8410                  LDR      A4,A4                  TEST FLAG
00065  0106  5804                  RB(Z)    *-2
00066  0108  0500                  LDK      A5,0
00067                      ****START OUTPUT LINE****
00068  010A  8508                  LDR      A5,A2
00069  010C  3D66                  SRL      A5,6
00070  010E  250C                  ANK      A5,/C                  PARITY PARAMETERS, OUTPUT COMMAND
00071  0110  8420                  LDKL     A4,/4010               OUTPUT, CHAR. MODE, BL=16
       0112  4010
00072  0114  0700                  LDK      A7,0                   COUNTER PROG CHANN. OUTPUT
00073  0116  7400          WER1OU  WER      A4,0
```

```
00074  0118  8420            LDKL    A4,BUFOUT          DATA ADDRESS
       011A  0172  R
00075  011C  7401      WER2OU  WER     A4,1
00076  011E  0400            LDK     A4,0               FLAG SSTI ACCEPTED
00077  0120  45C0      CIOOS   CIO     A5,1,0
00078  0122  5C04            RB(NA)  *-2
00079  0124  8410            LDR     A4,A4              TEST FLAG
00080  0126  5804            RB(Z)   *-2
00081  0128  0500            LDK     A5,0
00082  012A  5F40            RB      AGAIN
00083                  ****INTERRUPT ROUTINE****
00084  012C  4800      INRI    INR     A3,0,0
00085  012E  5430            RF(NA)  SSTI
00086  0130  5704            RF      *+6
00087  0132  4800      INRO    INR     A3,0,0
00088  0134  5430            RF(NA)  SSTO
00089  0136  860C            LDR     A6,A3
00090  0138  A620            ANKL    A6,/1000           INPUT OR OUTPUT?
       013A  1000
00091  013C  5416            RF(NZ)  INPUT
00092  013E  E35C      OUT     LC      A3,BUFOUT,A7
       0140  0172  R
00093  0142  23FF            ANK     A3,/FF
00094  0144  4300      OTR     OTR     A3,0,0
00095  0146  1701            ADK     A7,1
00096  0148  EF20            CWK     A7,16              ALL OUTPUT CHARS DONE ?
       014A  0010
00097  014C  5404            RF(NE)  *+6
00098  014E  0500            LDK     A5,0
00099  0150  4580      CIOOH   CIO     A5,0,0
00100  0152  F03E            RTN     A15
00101  0154  23FF      INPUT   ANK     A3,/FF
00102  0156  E341            SC      A3,BUF+1
       0158  017F  R
00103  015A  0500            LDK     A5,0
00104  015C  4580      CIOIH   CIO     A5,0,0
00105  015E  F03E            RTN     A15
00106                  ****STATUS ROUTINE****
00107  0160  4CC0      SSTI    SST     A4,0
00108  0162  5C04            RB(NA)  *-2
00109  0164  F03E            RTN     A15
00110  0166  4CC0      SSTO    SST     A4,0
00111  0168  5402            RF(NA)  DELAY
00112  016A  F03E            RTN     A15
00113  016C  1401      DELAY   ADK     A4,1               WAITLOOP AFTER NOT ACC SST
00114  016E  5C04            RB(NZ)  *-2
00115  0170  5F46            RB      INRI
00116                  ***DATA BUFFER***
00117  0172  4153      BUFOUT  DATA    'ASCU4Z TEST '
       0174  4355
       0176  345A
       0178  2054
       017A  4553
       017C  5420
00118  017E  2058      BUF     DATA    ' X'
00119  0180  0A0D            DATA    /0A0D
00120                         END     START
```

22 SYNCHRONOUS/A-SYNCHRONOUS LINE CONTROL UNIT P845-160 (SALCU-Z)

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22.1 SALCUZ IDENTIFICATIONS

Typenumber	:	P845-160
Function	:	Synchronous or Asynchronous Line control unit, with V24 interface and one line.
Testprogram	:	BZSAC1
Channel	:	PC or IOP
		Interrupt Connection: Transmitter 1C04
		Receiver 1C05
		Break Connection : Transmitter 1A05
		Receiver 1A05
Devices	:	1 line, Full Duplex or Half Duplex
Power Consumption	:	+5VL, 1.5Amp
		+12VL 50mA
		-12VL 90mA

12NC code on the sticker on the board:

5111 199 5676x (5322 216 25253)

X = Modification level

22.2 FACILITIES

- Synchronous or A-synchronous (start/stop) Data Transfer.
- 1 line, Full Duplex or Half Duplex.
- Connection of modems with V24/V28 interface or local connection.
- Transfer rate selectable: A-synchronous 50 - 19,200 bps
  Synchronous 800 - 56,200 bps (internal clock)
- Word length 5 - 6 - 7 or 8 bits selectable.
- Parity (VRC) software controlled.
- Stopbits 1 - 1.5 - 2 selectable (A-synchronous)
- Echo mode selectable (SALCU Half Duplex, 4 wire connection)
- Break character detection (Half Duplex, input during output detected, A-synchronous only)
- Break generation possible ('0' = high for 220 msec., A-synchronous only)
- CT119 for connection of CT133 from PER 3100 CTW (A-synchronous only)
- Stop on Halt character code
- Connection of MODEM clock (CT114, 115) or internal clock (CT113) for local use or test. (Synchronous only)
- Transparancy mode selectable (Synchronous only)
- Use of Call Indicator (CT125) selectable
- Device address transmitter = odd receiver = even
  interrupt transmitter on pin 1C04 receiver on pin IC05
  break transmitter on pin 1A04 receiver on pin 1A05
- Programmed channel or IOP - channel selectable
  Note: -- WAIT MODE IS POSSIBLE --

Link:	A/S:	Setting:	Description:
TP		INT: 1 / 0 / 2 — EXT: 1 / 0 / 2	Selection of the transmit baud rate freq. (internal or modem)
RP		INT: 1 / 0 / 2 — EXT: 1 / 0 / 2	Selection of the receive baud rate freq. (internal modem)
192	A	no / yes	CT119 option operational
C1, C2, C3			Select Halt Character

C1 C2 C3	ASCII	EBCDIC
1 / 0 / 2	=	NACK
1 / 0 / 2	7	EOT
1 / 0 / 2	.	ACK
1 / 0 / 2	NACK	NL
1 / 0 / 2	CR	CR
1 / 0 / 2	EOT	PF
1 / 0 / 2	ACK	LC
1 / 0 / 2	ETX	ETX

25		yes / no	Calling indicator (CT125) option operational

Figure 22.1 STRAP SETTING SALCUZ

RD,RC,RB,RA,RT

Position					local	
o o o RD	o o o RC	o o o RB	o o o RA	o o o RT	1 2 Linking A	S
2	2	2	2	1	50	(800)*
2	2	2	1	1	75	(1200)*
2	2	1	2	1	110	(1760)*
2	2	1	1	1	134.5	(2152)*
2	1	2	2	1	150	(2400)*
X	X	X	X	2	200	(3200)*
2	1	2	1	1	300	(4800)*
2	1	1	2	1	600	(9600)*
2	1	1	1	1	1200	(19200)*
1	2	2	2	1	1800	(28800)*
1	2	2	1	1	2000	(32081)*
1	2	1	2	1	2400	(38400)*
1	2	1	1	1	3600	(57600)*
1	1	2	2	1	4800	
1	1	2	1	1	7200	
1	1	1	2	1	9600	
1	1	1	1	1	19200	

* If internal clock is used.

Note: A = Asynchronous Mode Only S = Synchronous Mode Only (local clock)
Only transfer rates indicated in section 1.3 Technical Data are qualified.

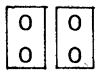
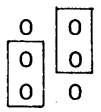
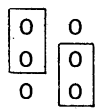
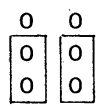
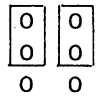
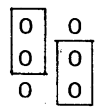
Link: W2 W1	A/S:	Setting:	Description: Number of data bits per character
		W2 W1 	8 bits
			6 bits
			7 bits
			5 bits
S1,S2	A	S1 S2 	2 stopbits
			1 stopbits

Figure 22.1 STRAP SETTING SALCUZ - CONTINUED

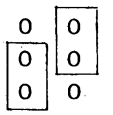
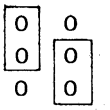
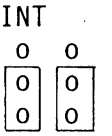
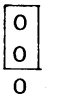
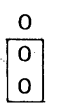
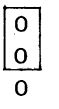
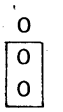
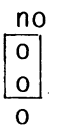
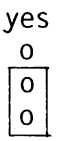
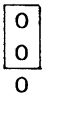
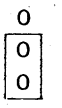
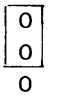
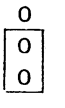
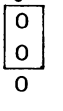
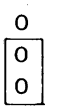
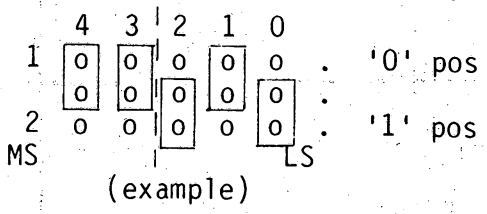
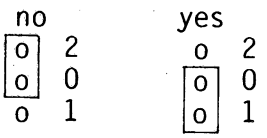
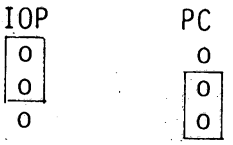
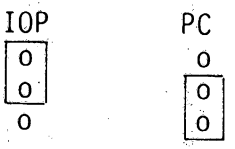
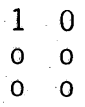
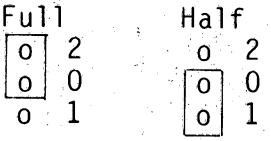
Link:	A/S:	Setting:	Description:
			1.5 stopbits
S1,S2	S	EXT 	Transparency Mode
		INT 	Internal Synchronization on SYN
MD		ASYN  SYN 	A-synchronous or Synchronous Mode
191	A	+12V  -12V 	Selection of the active level for CT119
COM		no  yes 	Comparator Operational for blocking leading SYN and HALT Char. detection
SYN	S	EXT 	Transparency Mode
		INT 	Internal Synchronization on SYN
134	S	CT114 	(Input) CT114 Modem
		CT113 	(Output) CT113 Local
BD		yes  no 	Break detection operational

Figure 22.1 STRAP SETTING SALCUZ - CONTINUED

Link:	A/S:	Setting:	Description:
AD		 (example)	SALCU Address (Input) (shown /0A)
HC			Halt on preselected character
MO/PO			Channel in Output Mode
MI/PI			Channel in Input Mode
GEX			Internal clock pulse (shown: position for normal operation)
FH			Full or Half duplex mode

Note: A = Asynchronous Mode Only; S = Synchronous Mode Only

Figure 22.1 STRAP SETTING SALCUZ - CONTINUED

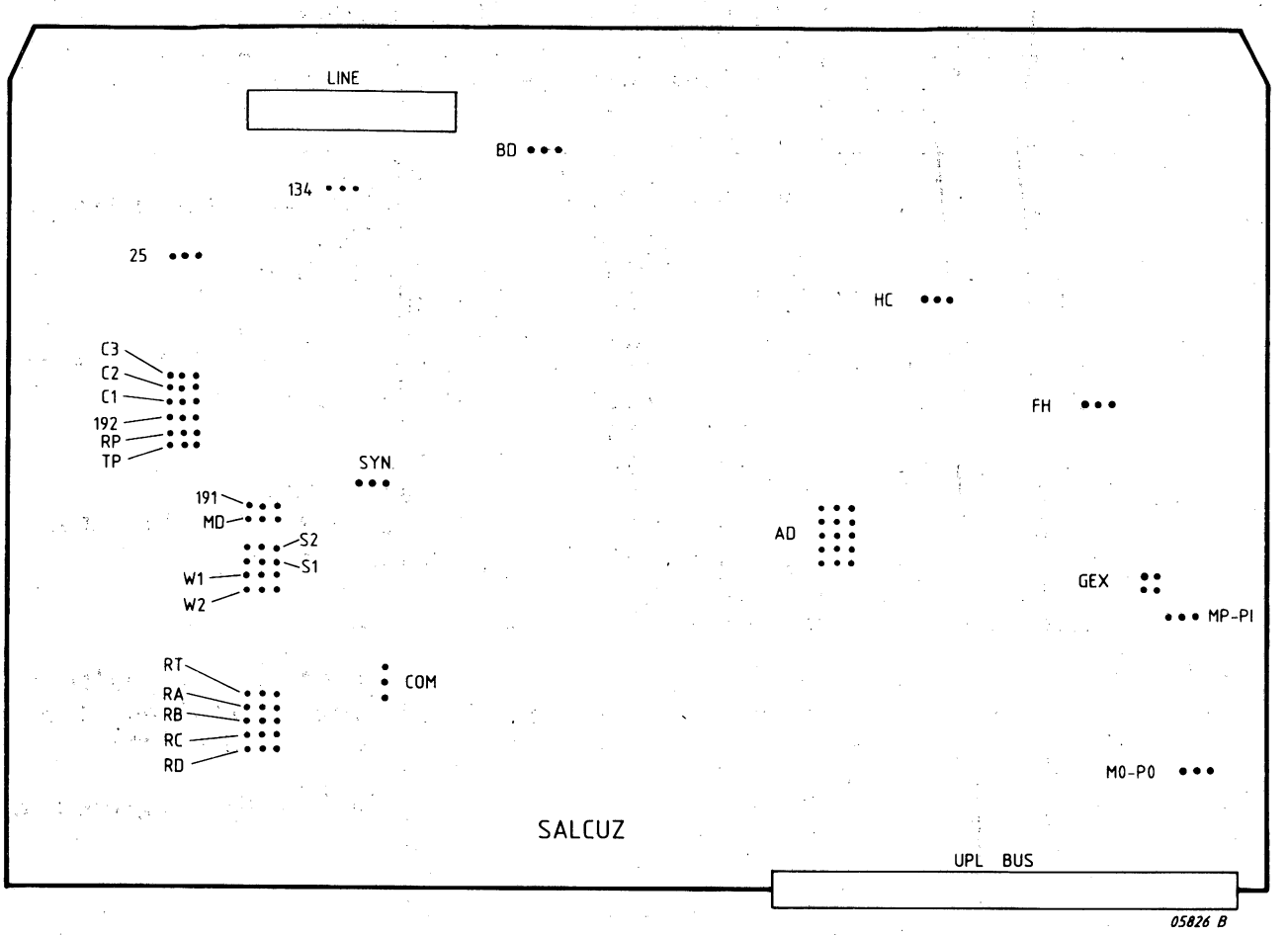


Figure 22.1 STRAP SETTING SALCUZ - CONTINUED

22.4 INTERFACE CONNECTIONS

Available signals according V24 on SALCU-Z

Card (female)	Modem (male)	Signal Name	Signal Direction
1	1	CT101 mech. gnd	Bi-directional
7 - 25	7 - 25	CT102 logic gnd	Bi-directional
2	2	CT103 trx. data	Output to the DCTE
3	3	CT104 rec. data	Input to SALCUZ
4	4	CT105 req. to send	Output to the DCTE
5	5	CT106 ready f.s.	Input to SALCUZ
6	6	CT107 modem r.	Input to SALCUZ
20	20	CT108 connect m.	Output to the DCTE
8	8	CT109 carrier	Input to SALCUZ
15	15	CT113 m. clock	Output to the DCTE
15	15	CT114 trx. clock	Input to SALCUZ
17	17	CT115 rec. clock	Input to SALCUZ
16	16	CT119 backw. ch.	Input to SALCUZ
22	22	CT125 ring ind.	Input to SALCUZ

Table 22.1 SALCUZ SOCKET 3 CONNECTIONS TO DCE

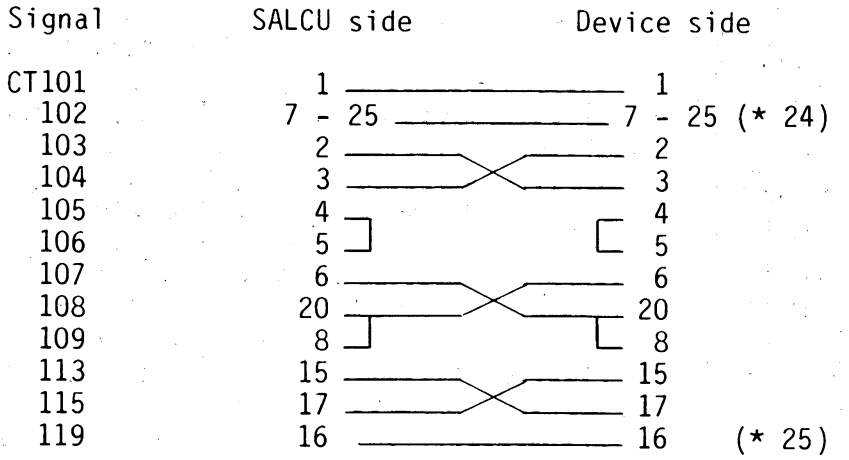
For SALCU-Z a standard cable is used.

Signal	Connector Panel Female	Modem Male
CT101	1	1
102	7 - 25	7 - 25
103	2	2
104	3	3
105	4	4
106	5	5
107	6	6
108	20	20
109	8	8
111	23	23
114	15	15
115	17	17
119	16	16
125	22	22

Note: CT111 is not controlled by SALCU.
Max. cable length is 15m.

Table 22.2 STANDARD CABLE SALCUZ

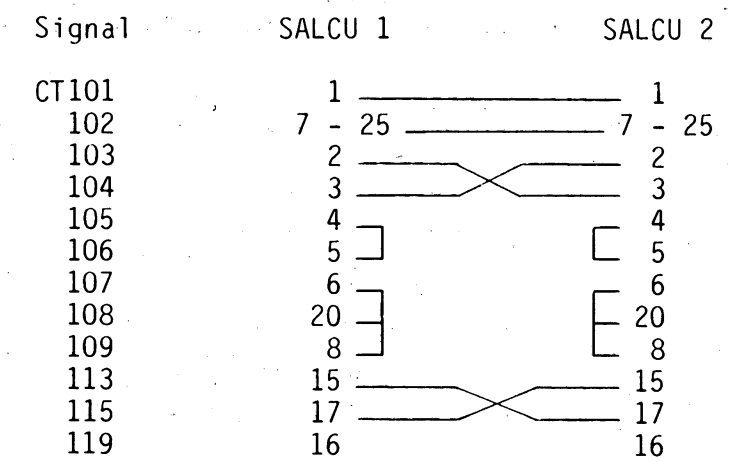
For a local connection, between CU and terminal, wiring could be made according:



(* = if RFR used on PER3100 typewriter)

Figure 22.2 INTERFACE WIRING CU-TERMINAL (LOCAL)

For local connection of two systems, wiring could be made according:

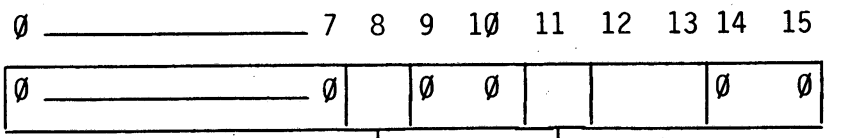


Note: U-link setting in this case RP ext
TP int
134 in 113 position

Figure 22.3 INTERFACE WIRING CU-CU (LOCAL)

Device address in = DA (rec)
Device address out = DA +1 (trx)

CIO start (in/out) BIO

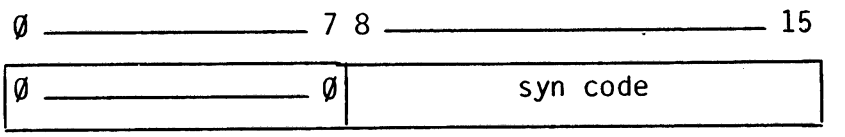


HD only (generate break (220ms)
(echo input)

X Ø = no parity
Ø 1 = even parity
1 1 = odd parity

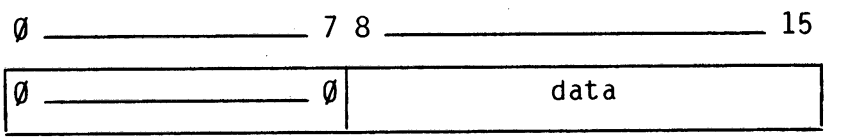
Notes: - CIO start-in must precede start out.
- generate break: only in idle or HD input.

OTR syn F = 1 (in/out) BIO

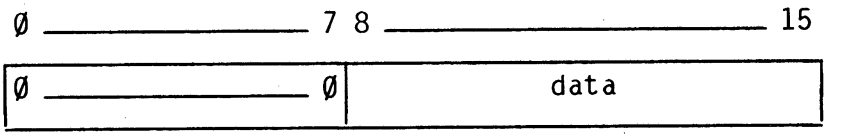


Synchronous mode only, immediately after 1st CIO start.

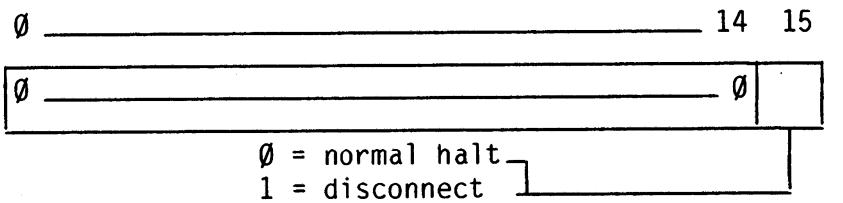
OTR data F = 0 (out) BIO



INR data F = 0 (in) BIO

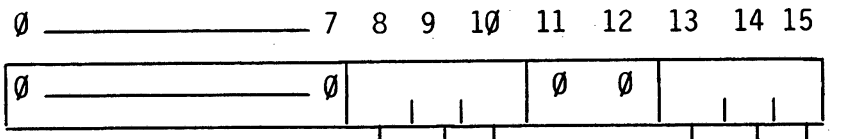


CIO halt (in/out) BIO



Notes: Normal halt at FD: CIO halt must be given for both input and output, before the next CIO start.
Disconnect : The specified device address must be 'input address'. The SALCU is reset immediately.

SST (in/out)



HD OUT: char. received (=break)
IN : ring indicator CT125
IN : carrier drops CT109
IN : parity error
IN : character loss (throughput)
modem not operable CT107

22.6 SHORT DESCRIPTION OF TESTPROGRAM

TESTPROGRAM BZSAC1

Transfer rate synchr. mode max. 4800 bps
a-synchr. mode max. 9600 bps

PROCEDURE:

- IPL
  Note: Connect loop plug! = CT 103-104 pin 2-3
  (Select local clock) CT 105-106- 4-5
  CT 108-107-109 20-6-8
- Switch on RTC, Lock (within 3 sec.)

Typewriter prints: Type in: example = standard configuration.

```
Initialization   etc.
Standard checks  etc.
Extra checks     etc.
Standard checks?              Y
Address input?                0A
Nb of data bits?              07
Int input?                    04
Int output                    05
Channel?                      P
Mode?                         A
Error exit?                   Y
Break detection?              N
Halt detection?               N
Reloop check?                 N
```

- End of program, stop at address/0D00 = restart address

BZSAC1 tested:

```
IF 0000  (B)  Check 00 (standard)     Test I/O instruction
IF 0001  (B)  Check 01     ,,         Test sequensor
IF 0002  (B)  Check 02     ,,         Test interrupt in output mode
IF 0003  (B)  Check 03     ,,         Test input/output (1st part)
IF 0004  (B)  Check 04     ,,         Test input/output (2nd part)
IF 0005  (B)  Check 05     ,,         Test ODD/EVEN parity
IF 0006  (A)  Check 06     ,,         Test break emission
IF 0007  (A)  Check 07     ,,         Test throughput error
IF 0008  (A)  Check 08     ,,         Test break detection
IF 0009  (B)  Check 09     ,,         Test halt character
IF 000A  (A)  Check 10 (not standard) Test CT119
IF 000B  (A)  Check 11     ,,         Test parity error detection and echo
                                      mode/visualisation
IF 000C  (B)  Check 12     ,,         Test CT105
IF 000D  (S)  Check 13     ,,         Test comparator inhibition
IF 000E  (S)  Check 14     ,,         Test transparency mode
IF 000F  (B)  Check 15 (standard)     Test multiplex
```

A = Asynchronous mode only
B = Both modes
S = Synchronous mode only

```
  Procedure  5111 991 10071 =     Procedure BZSAC1   5111 991 09304
                                with addendum PTS8000  5111 991 11381
  Listing    5111 991 10081
  Program    5111 199 65671
```

```
                                IDENT    SALCUT
                        *
                        * SALCU PROGRAM, TRX ONLY, A-SYNCHRONOUS
                        * CONNECT LOOPPLUG: CT108-107-109 (PIN 20-6-8) AND CT105-106 (PIN 4-5)
                        *
                        * LINE CHECKED WITH OSCILLOSCOPE:
                        *
                        *    '0'=+12V    I---I   I---I   I---I   I---I   I---I   I---I STOPBITS
                        *    '1'=-12V ---I   I---I   I---I   I---I   I---I   I---I
                        *                          1   0   1   0   1   0   1   0
                        *          =A2 BITN   15  14  13  12  11  10   9   8      /55='U'
                        *
                        *
                        * OR:  CONNECT CTW, 1 LINE OF CHARS 'U' IS PRINTED (USE CT108/7/5/6)
                        *
                        * INTERRUPT LEVEL 11 = /B
     0018               DA       EQU      /1B
0000                             RES      /40
0080  FFFF              DATA     DATA     /FFFF
0082  0000                       DATA     0
0084  207F              START    HLT
0086  2840                       ENB
0088  87A0              BEG      LDKL     A15,/120              STACKPOINTER
008A  0120
008C  8120                       LDKL     A1,INTAD
008E  009A  R
0090  8141                       ST       A1,/16                START ADDR INT ROUTINE
0092  0016
0094  0104                       LDK      A1,4
0096  41DB                       CIO      A1,1,DA
0098  5F02                       RB       *                     WAITING FOR DATA INTERRUPT
                        *
                        *   INTERRUPT ROUTINE
                        *
009A  0255              INTAD    LDK      A2,/55                CHAR 'U'
009C  421B                       OTR      A2,0,DA
009E  F03E                       RTN      A15



                                IDENT    SALCLA
                        *
                        * LOOP, FULL DUPLEX, A-SYNCHRONOUS
                        * CONNECT LOOPPLUG: CT103-104  PIN 2-3, 105-106 PIN 4-5,
                        *                   CT108-107-109=PIN 20-6-8
                        * 7-BITS, EVEN PARITY
                        *
                        *  CHECK:1) STOP AFTER INR.(REPLACE '/5408' BY '/207F')
                        *           CHECK IF REC CHARACTER='U': A3 MUST CONTAIN /55.
                        *        2) CHECK OSCILLOSCOPE PICTURE.(SEE PROGRAM SALCUT)
                        *
                        *        DATA FAULT: STOP AT /0AE (HHP /00B0)
                        *        STATUS FAULT: STOP AT /B2 OR /B8 (HHP /B4,/BA)
     001A               DAREC    EQU      /1A
     001B               DATRX    EQU      /1B
     000A               INTREC   EQU      10
     000B               INTTRX   EQU      11
0000                             RES      /40
0080  FFFF              DATA     DATA     /FFFF
0082  0000                       DATA     0
                        * -- MAIN PROGRAM --
0084  207F              START    HLT
0086  2840                       ENB
0088  0255              BEG      LDK      A2,/55                CHAR 'U'
008A  87A0                       LDKL     A15,/120              STACKPOINTER
008C  0120
008E  8120                       LDKL     A1,STAR               START ADDR INT ROUTINE REC
0090  00A6  R
0092  8141                       ST       A1,/14
0094  0014
0096  8120                       LDKL     A1,STAT               START ADDR INT ROUTINE TRX
0098  00B4  R
009A  8141                       ST       A1,/16
009C  0016
009E  0104                       LDK      A1,4
00A0  41DA                       CIO      A1,1,DAREC
00A2  41DB                       CIO      A1,1,DATRX            START I/O
00A4  5F02                       RB       *                     WAIT FOR INTERRUPT
                        * -- INTERRUPT ROUTINE REC --

00A6  481A              STAR     INR      A3,0,DAREC
00A8  5408                       RF(4)    *+/A
00AA  E808                       CWR      A3,A2
00AC  5002                       RF(0)    ERR                   DATA FAULT
00AE  207F                       HLT
00B0  F03E              ERR      RTN      A15                   EQUALITY RIGHT,RETURN
00B2  207F                       HLT



                        *  INTERRUPT ROUTINE TRX --
00B4  421B              STAT     OTR      A2,0,DATRX
00B6  5002                       RF(0)    *+4
00B8  207F                       HLT
00BA  F03E                       RTN      A15                   IF NO STATUS ERROR
```

```
                        IDENT    SALCLS
                      * LOOP ON SALCU, FULL DUPLEX, SYNCHRONOUS MODE
                      *CONNECT LOOPPLUG:CT103-104 (PIN 2-3),105-106 (4-5),108-107-109(20-6-8)
                      *        DATA: SYN - SYN - CHAR 'U'
                      *
                      * CHECK: STOP PROGRAM AFTER INR.(REPLACE /EC18 BY /207F)
                      *              CHECK IF REC CHAR ='U'.(REG A6 MUST CONTAIN /55)
                      *      -OR- CHECK WITH OSCILLOSCOPE
                      *
                      *     DATA FAULT: STOPS AT /B2 (B4 AT HHP)
                      *     STATUS FAULT KEEPS PROGRAM IN RUN.BUT DATA TRANSFER STOPS
                      *
                      *
                      * OSCILLOSCOPE PICTURE:

                      *  0  0 000 0  0 000 . 0 0 0 0
                      *   11 1     11 1    1 1 1 1
                      *   SYN      SYN      'U'CHAR
      001A      DAREC    EQU      /1A
      001B      DATRX    EQU      /1B
      000A      INTREC   EQU      10
      000B      INTTRX   EQU      11
0000                     RES      /40
0080  FFFF      DATA     DATA     /FFFF
0082  0000               DATA     0
                      *
                      * -- MAIN PROGRAM --
0084  207F      START    HLT
0086  2840               ENB
0088  87A0      BEG      LDKL     A15,/120              STACKPOINTER
008A  0120
008C  8120               LDKL     A1,STAR               START ADDR INT ROUTINE REC
008E  00AC  R
0090  8141               ST       A1,/14
0092  0014
0094  8120               LDKL     A1,STAT               START ADDR INT ROUTINE TRX
0096  00C6  R
0098  8141               ST       A1,/16
009A  0016
009C  0416               LDK      A4,/16                SYN CHAR CODE
009E  8220               LDKL     A2,/FFFD              CONTROL COUNTER
00A0  FFFD
00A2  030C               LDK      A3,/C
00A4  430A               CIO      A3,1,DAREC            START REC
00A6  445A               OTR      A4,1,DAREC            SYN
00A8  430B               CIO      A3,1,DATRX            START TRX
00AA  5F02               RB       *                     WAIT FOR INTERRUPT


                      *
                      * -- INTERRUPT ROUTINE REC --
00AC  4E1A      STAR     INR      A6,0,DAREC
00AE  EC18               CWR      A4,A6
00B0  5002               RF(0)    ON                    HLT IF DATA FAULT
00B2  207F               HLT
00B4  439A      ON       CIO      A3,0,DAREC
00B6  8140               LD       A1,/120
00B8  0120
00BA  190E               SUK      A1,/E
00BC  8141               ST       A1,/120               CHANGE RETURN ADDRESS
00BE  0120
00C0  4DDA               SST      A5,DAREC
00C2  5C04               RB(4)    *-2                   STATUS
00C4  F03E               RTN      A15
                      *
                      * -- INTERRUPT ROUTINE TRX --
00C6  4FDB      STAT     SST      A7,DATRX              STATUS
00C8  500C               RF(0)    RET2
00CA  1201               ADK      A2,1
00CC  5004               RF(0)    DAT
00CE  5204               RF(2)    SYN
00D0  439B               CIO      A3,0,DATRX
00D2  0455      DAT      LDK      A4,/55
00D4  4418      SYN      OTR      A4,0,DATRX
00D6  F03E      RET2     RTN      A15
```

23 HIGH LEVEL DATA LINK CONTROL UNIT P845-110 (HLVCUZ)

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23.1 HLVCUZ IDENTIFICATIONS

Typenumber : P845-110

Function : Datacom Control Unit for High Level Data Link transfer (synchronous, HDLC frames), with V24 interface.

Testprogram : BHLCU1

I/O Channel : Program or Multiplex channel

Power consumption : +5V 2.5 A
+12V 50mA
-12V 50mA

12NC code (on the sticker) : 5111 199 6010X
X = modification level

Devices : - MODEM (in point to point or multidrop connection)
- Direct connection to a VDU (null modem)

23.2 FACILITIES

- Half or Full Duplex
- HDLC frame format (synchronous data transfer).
- V24/V28 interface.
- Bit oriënted protocol for transmit and receive.
- Transfer speed : up to 115 kb/sec.
- Leased or Switched Line.
- Idle and Abort detection.
- Secondary Station Adress detection.
- Remote IPL.
- Internal clock selection (CT113), for local or modem connection.
- Selectable connection timer (for CT107 time out).
- Test loop facilities (V54)
- Selection for Binary Coded (BCI) or Direct interrupt.
- Selection of pin ouput of the BCI interrupt (1C03 for CIP or 1C04 for DIP).

23.3 INSTALLATION DETAILS

23.3.1 STRAP SETTING (Figure 23.1)

The meaning of the STRAPS:

- Control Unit Adress (S22 - S26) : Selects the 5 msb of the control unit address.

- Interrupt level (S28-S38) : Selects the Binary Coded Interrupt level for transmitter and receiver.

- Interrupt Destination (S02) : Selects the destination of the interrupt, pin 1C03 for CIP, pin 1C04 for DIP. (see figure 23.2)

- Kind of interrupt (S27) : Selects Binary Coded or Direct interrupt. (see figure 23.2)

- Local or Modem (S01 and S41) : Selects a Modem or Local connection for the V24 interface (for Local connection the internal clock CT113 of the CU is used.

- Speed internal clock (S11 - S13) : Selects the speed in bits/seconde of the internal clock, used if the Local Connection is selected. (7.1, 56.8 and 113.6 Kbit/sec)

- CT107 timer (S08-S10) : Selects the time out for the signal CT107 of the modem. (72msec, 4.6sec or infinity)

- Receiver timer out (S42) : Selects the time out of 18.4 second, when after the the start for receiving command, no data is received.

- CT108 selection (S39) : Selects the CT108 signal for being active or inactive after power on.

- Oscillator (S40) : Selects the internal oscillator of the CU, or an external oscillator connected to J4.

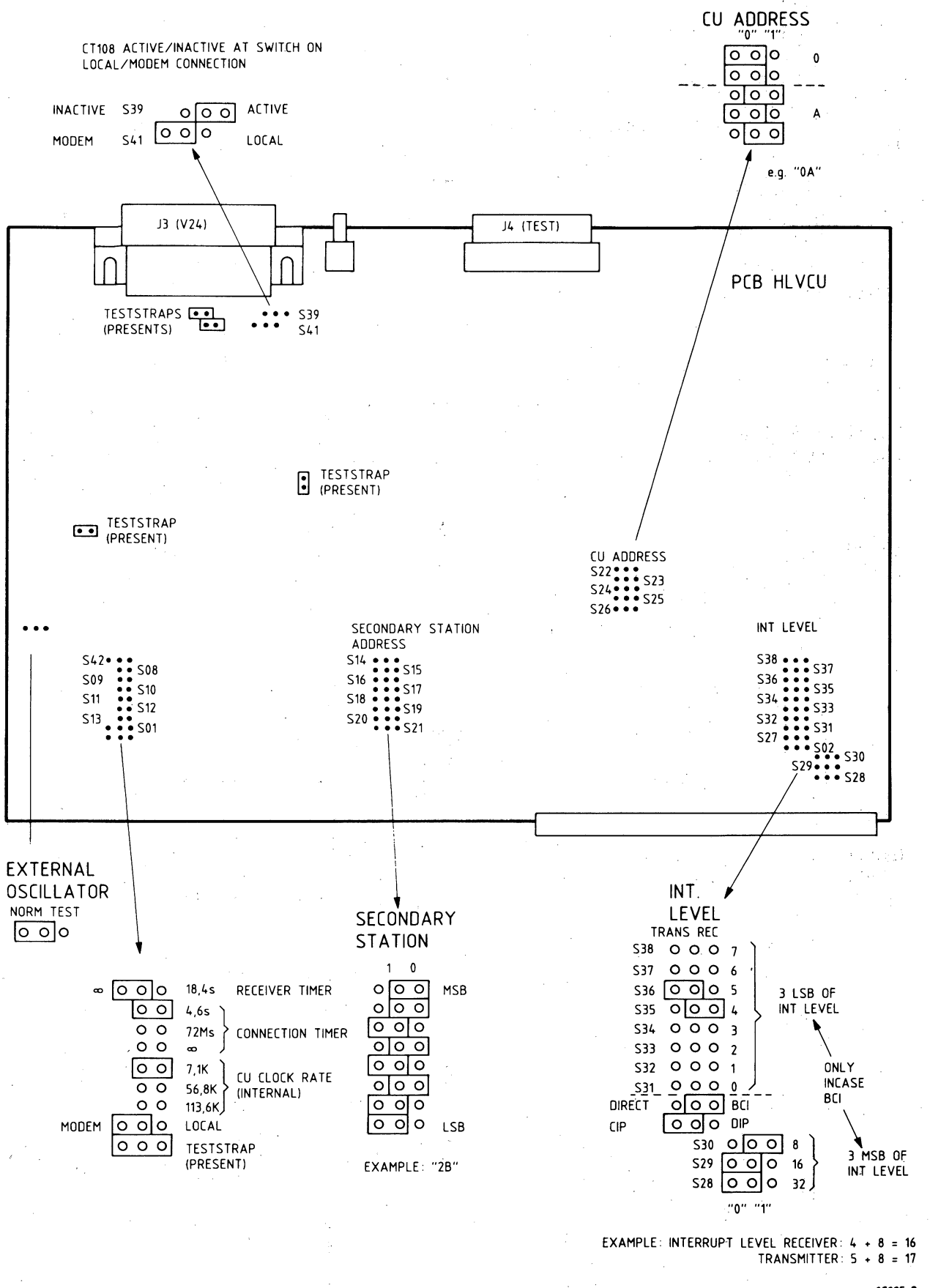


Figure 23.1 STRAP SETTING HLVCUZ

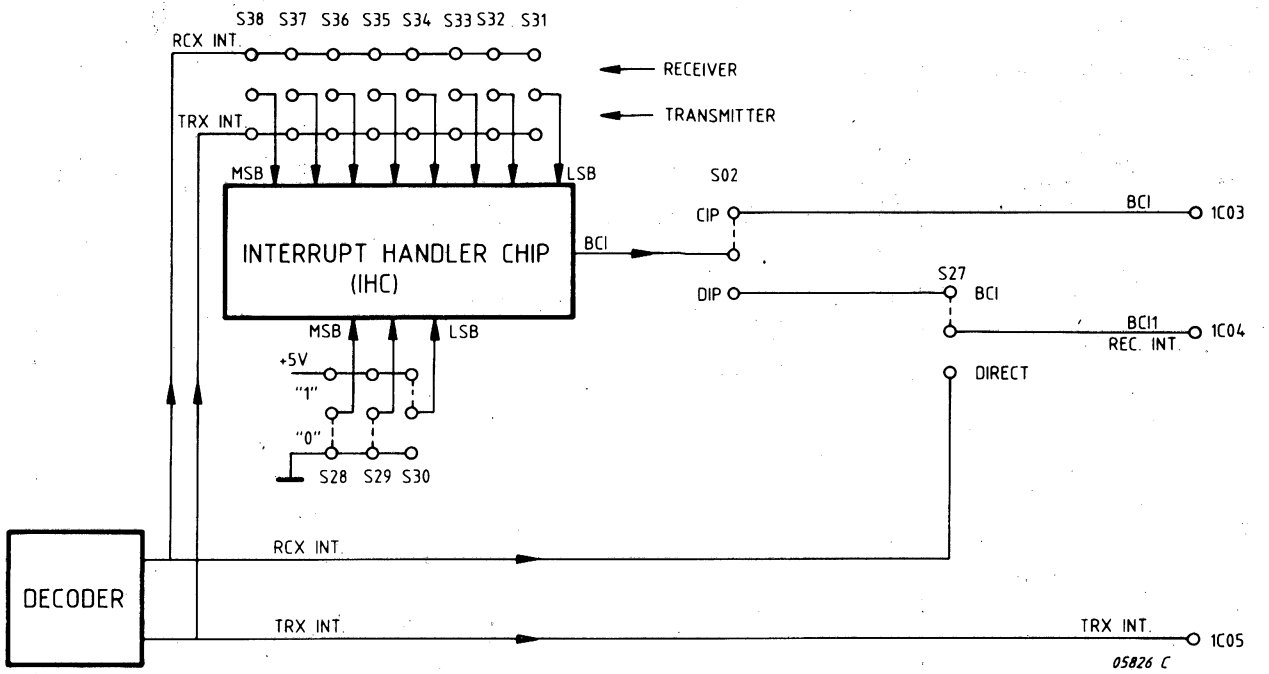


Figure 23.2 INTERRUPT STRAPS

23.3.2 INTERRUPT AND BREAK WIRING

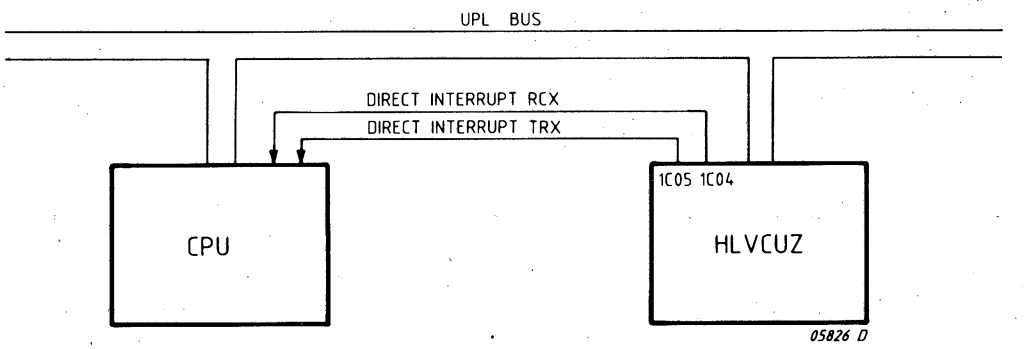


Figure 23.3a DIRECT INTERRUPT WIRING

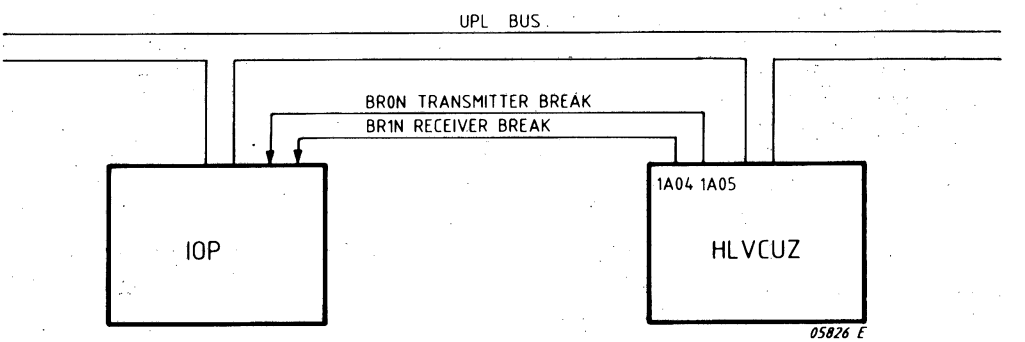


Figure 23.3b BREAK WIRING

23.4 INTERFACE CONNECTIONS

23.4.1 MODEM CONNECTION

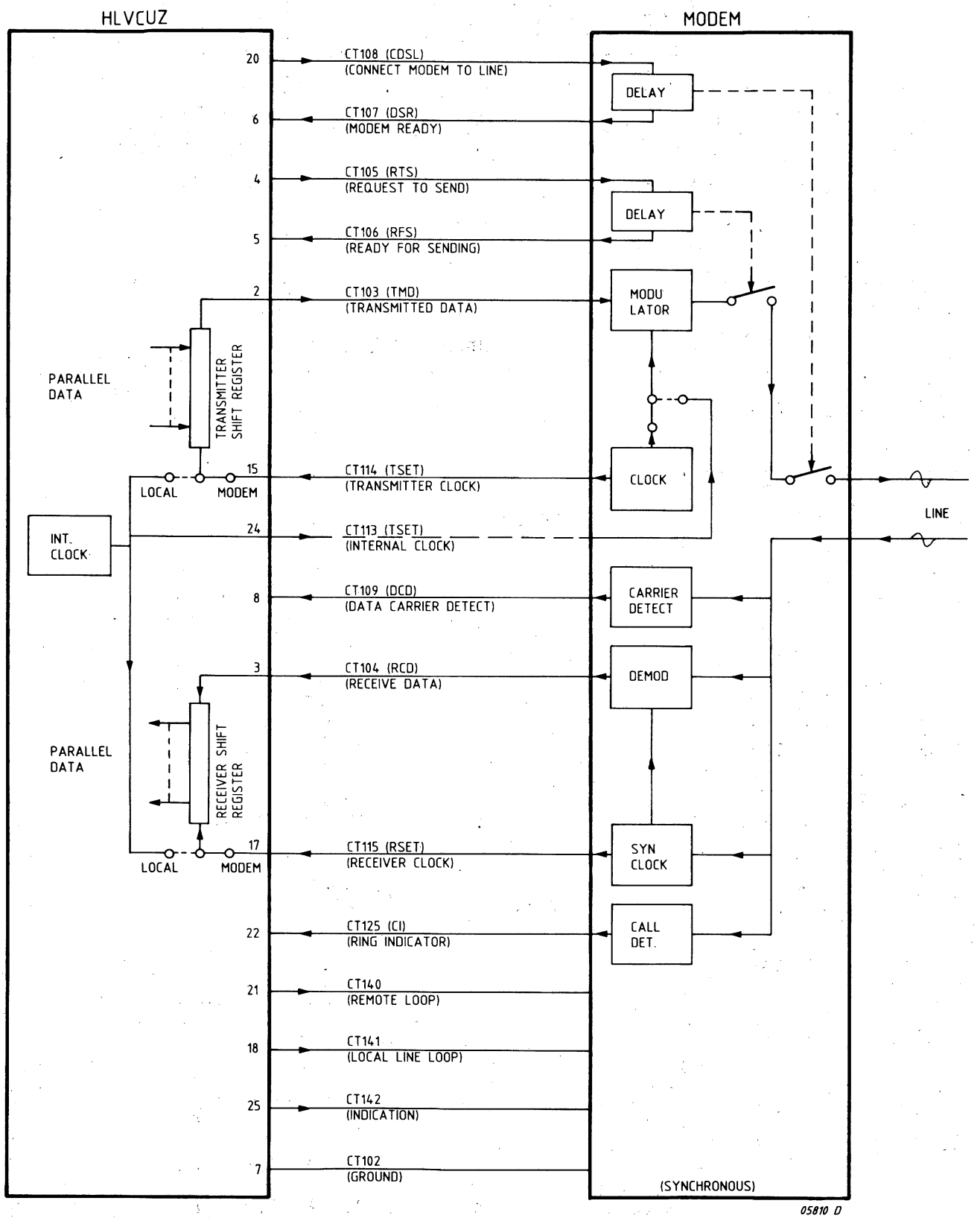


Figure 23.4 MODEM CONNECTION

23.4.2. LOCAL CONNECTION

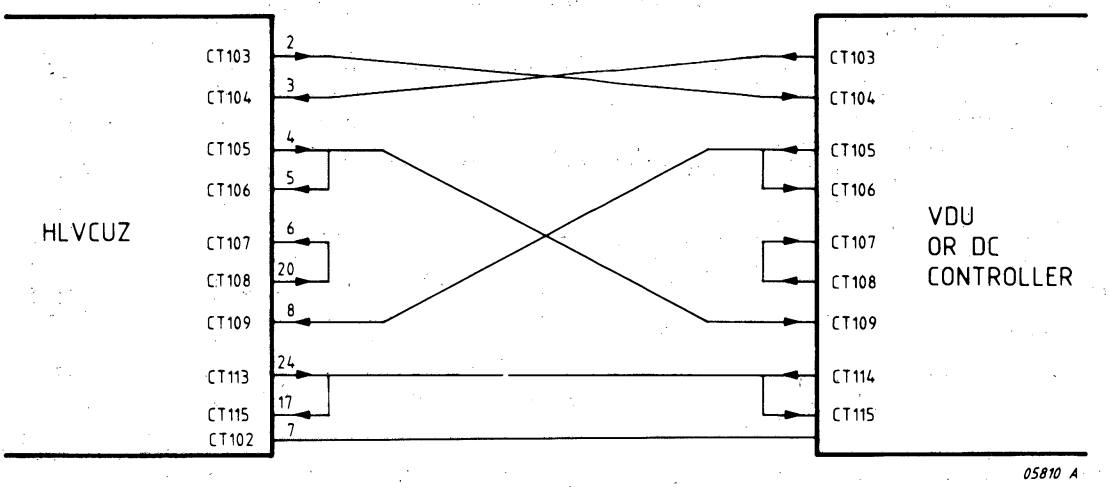


Figure 23.5 LOCAL CONNECTION

23.4.3 CONNECTORS

PIN NO.	SIGNAL MNEMONIC
---	CT101
3J01	---
3J02	CT103
3J03	CT104
3J04	CT105
3J05	CT106
3J06	CT107
3J07	CT102
3J08	CT109
3J09-14	---
3J15	CT1314
3J16	---
3J17	CT115
3J18	CT141
3J19	---
3J20	CT108/1 CT108/2
3J21	CT140
3J22	CT125
3J23	CT111
3J24	CT113
3J25	CT142

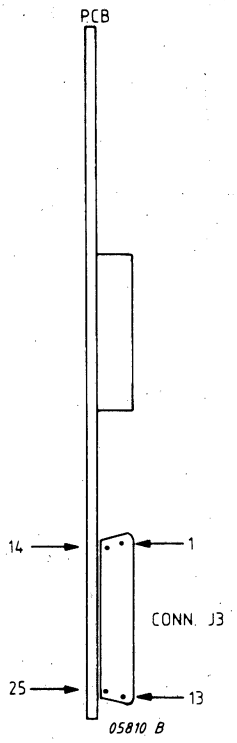


Table 23.1 CONNECTOR J3 (V24 INTERFACE)

PIN NO.	SIGNAL MNEMONIC	SIGNAL FUNCTION
4A01	IVB3N	]
4A02	IVB4N	]
4A03	IVB5N	] Cu Internal Bus Lines
4A04	IVB6N	]
4A05	IVB7N	]
4A06,8	0V	Logical Ground
4A07	OSCTEST	External Test Oscillator Input
4A9,10	+5V1	Power Supply
4A11	M10	]
4A12	M11	]
4A13	---	]
4B01	M0	]
4B02	M1	]
4B03	M2	]
4B04	M3	] PROM Address Lines
4B05	M4	]
4B06	M5	]
4B07	M6	]
4B08	M7	]
4B09	M8	]
4B10	M9	
4B11	IVB0N	]
4B12	IVB1N	] Internal Bus Lines
4B13	IVB2N	]

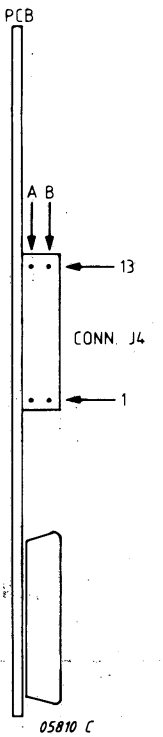


Table 23.2 CONNECTOR J4 (TEST)

23.4.4 CABLES (figure 23.6)

The 12 NC code of the Modem-cable is: 5111 199 53770

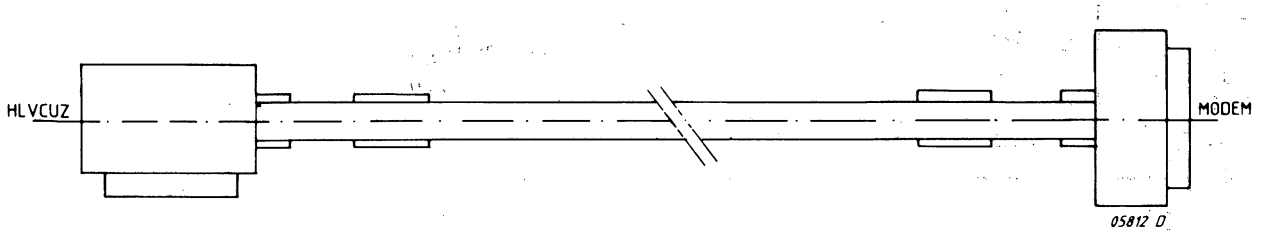


Figure 23.6 CABLE

23.5 BLOCK DIAGRAM HLVCUZ

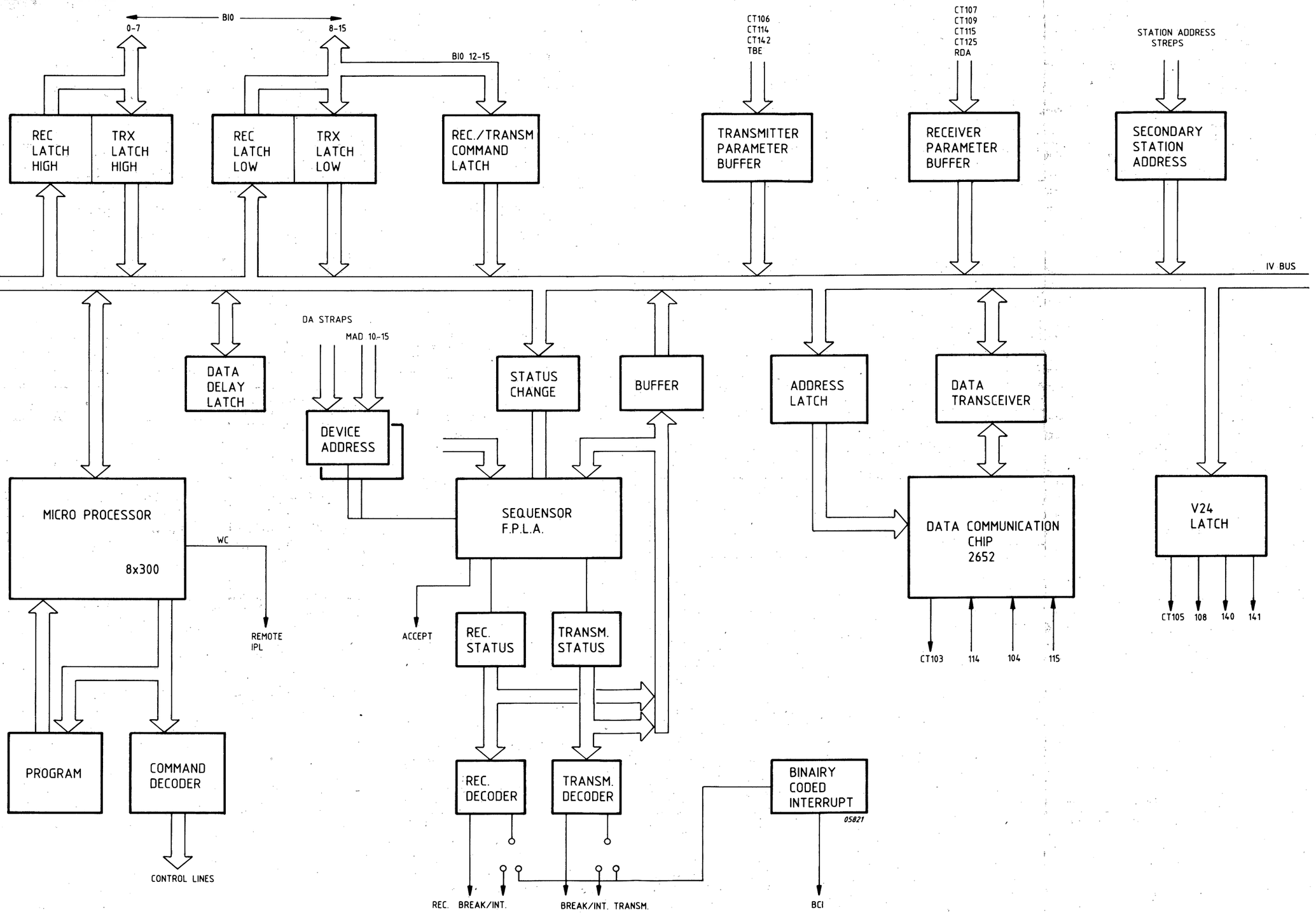
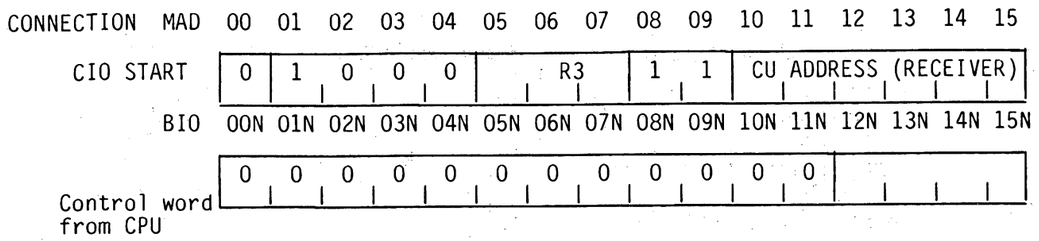
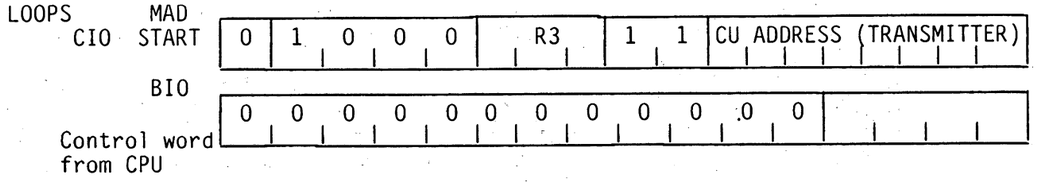


Figure 23.7 BLOCK DIAGRAM HLVCUZ

GENERAL COMMANDS



Must use receiver address	Disconnect DCE	0 0 0 1
	Connect 1 (no secondary address checking)	0 0 1 0
	Connect 2 (with secondary address checking)	0 1 1 0
	Wait for Call	0 0 1 1



Must use transmitter address	Set CT141 Loop	X 1 1 0
	Stop CT141 Loop	0 1 0 1
	Set CT140 Loop, Program Channel	0 1 1 1
	Stop CT140 Loop, Program Channel	0 0 0 0
	Set CT140 Loop, IOP Channel	1 1 1 1
	Stop CT140 Loop, IOP Channel	1 0 0 0

MISCELLANEOUS

Must use transmitter address	Request to Send OFF	X 0 0 1
	Transmit Idle Sequence	X 1 0 0
	Get V24 Line Status	1 1 0 1

Figure 23.8 GENERAL AND RECEIVER COMMANDS

RECEIVER COMMANDS

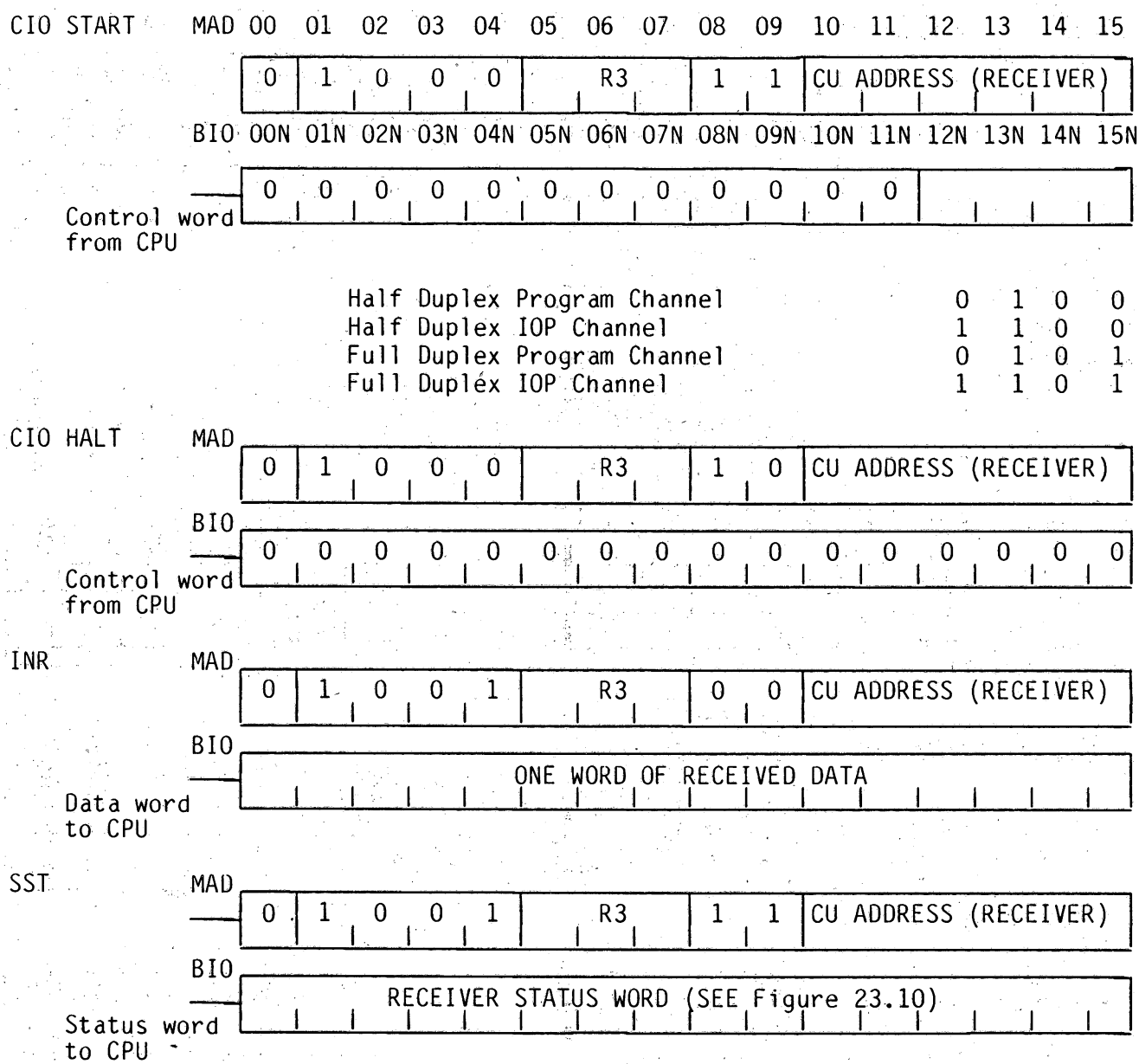


Figure 23.8 GENERAL AND RECEIVER COMMANDS (CONT.)

TRANSMITTER COMMANDS

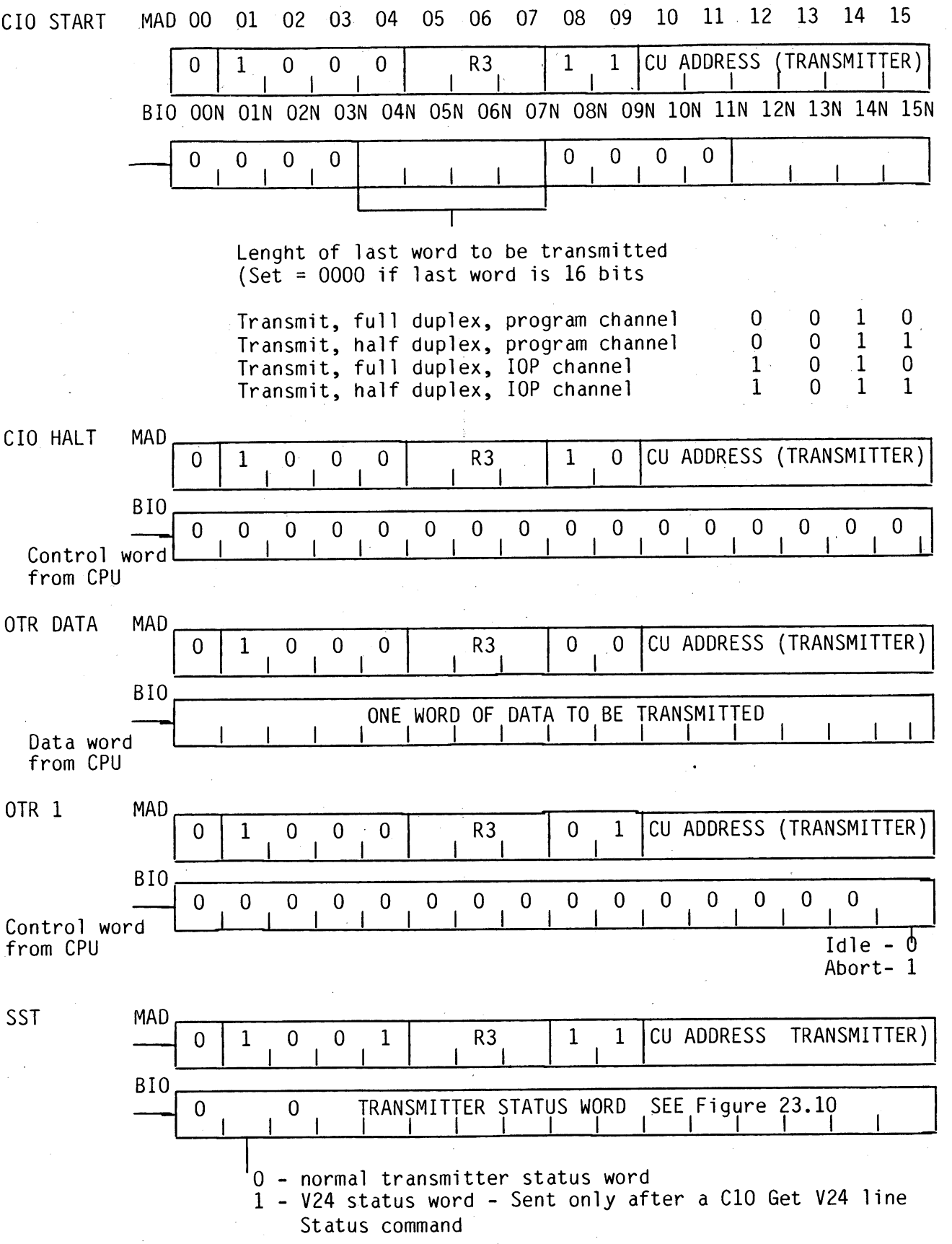


Figure 23.9 TRANSMITTER COMMANDS.

RECEIVER STATUS WORD

00	01	02	03	04 05 06 07	08	09	10	11	12	13	14	15
0	0	ABRT IDLE	0	No. of true data bit in last word	Prog. Error	CT 125	CT 109 N	0	Inc. Lnth	FCS Err	Thr. put	Not op.

TRANSMITTER STATUS WORD

Normal Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	Time Out	0	Thr. Put	Not op.

V24 Status Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	0	CT 141	CT 140	CT 105	CT 106	CT 107	CT 108	CT 109	0	0	CT 125	CT 142	CT 114/ 113	CT 115

Figure 23.10 STATUS WORD

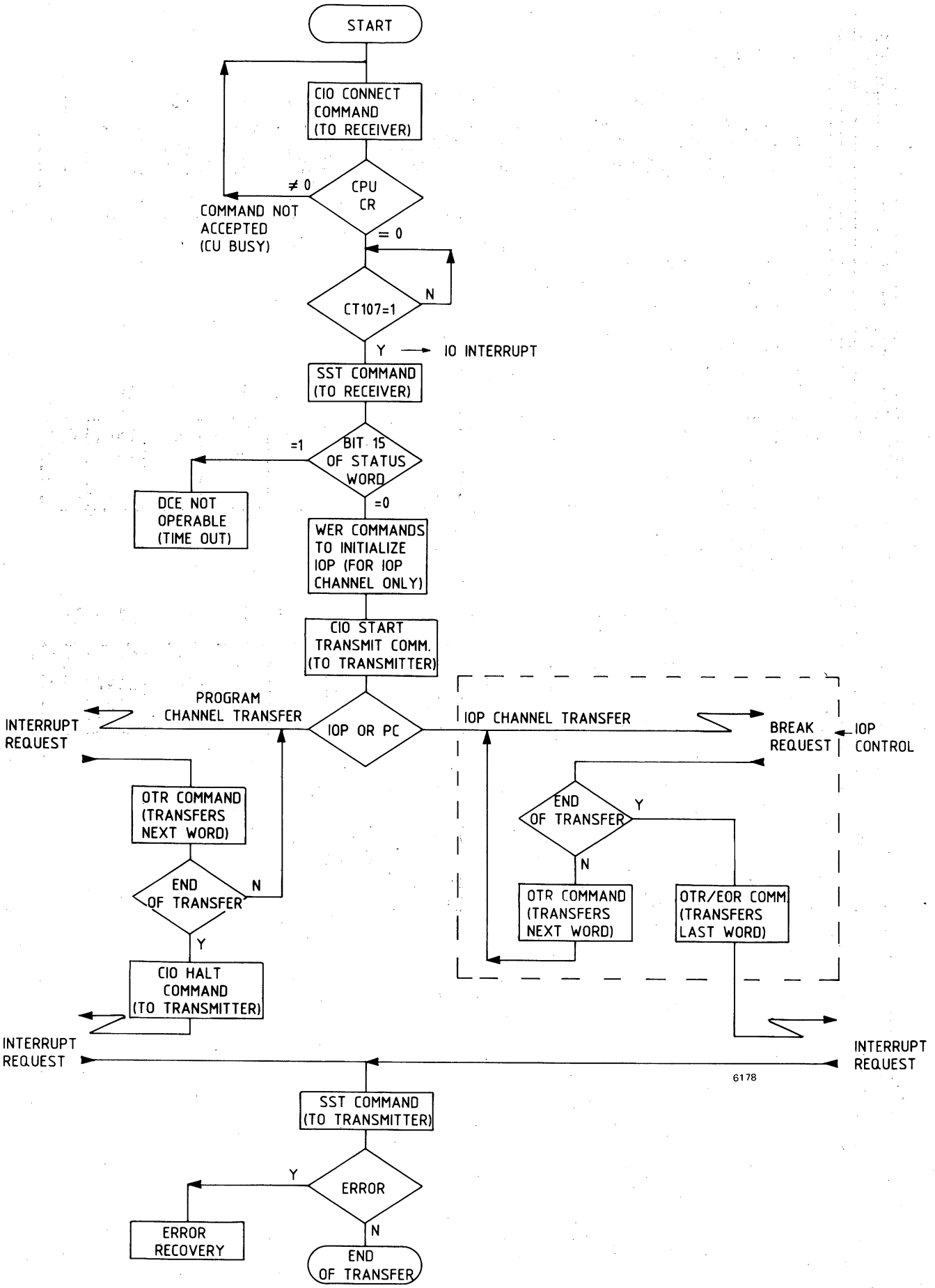


Figure 23.11 COMMAND FLOWCHART

23.7 SHORT DESCRIPTION OF TESTPROGRAM

TESTPROGRAM BHDLC

12K
Program runs under monitor BOS
- Connect loop-plug to HLVCUZ, set Local Clock

Procedure:

- IPL
  RTC on

Terminal output:	Type in on keybord:
PARMON	
Standard or change FC	C "CR"
Full/half duplex	F "
Input device address	ØA "
interrupt level	Ø4 "
Output device address	ØB "
interrupt level	Ø5 "
PC or IOP	P "
Leased or switched line	L "
End of PARMON	
Print 1 for HLCU1	
Print 0 for HLVCUZ	Ø "
Filecode	5 "
*	"CR"

- The program starts after 'CR' is depressed.
- Check on running testprogram: take off the loop plug from HLVCUZ
  An error message will be displayed on the terminal.
- Stop program: press Control Panel Interrupt button.
  type 'SP' on keyboard (= Stop Program)

Loop-plug wiring HLVCUZ	pin	2 - 3 CT	1Ø3 - 1Ø4
		4 - 5	1Ø5 - 1Ø6
		20-6-8	1Ø8-1Ø7-1Ø9
		15 - 17	113 - 115

Note: Max speed 7.1 kbits/sec.

Error Messages

Errors in the commands message

ERR 0 : - A wrong order has been printed
        - More than one order has been printed

ERR 1 : - Too much characters have been printed
          . More than 4 in the word length or in the pattern
          . More than 2 in the bit length or bit length greater than 15

ERR 2 : - Decimal number greater than 9 or hexadecimal number greater than /F

ERR 13: - The required check does not correspond to the file code definition

Errors printed during running of a check:

ERR 3 : Status error after a C10 connect

ERR 4: Hardware status error after a Transmission

ERR 5: Software status error after a Transmission

ERR 6: Hardware status error after a Reception

ERR 7: Software status error after a Reception

ERR 8: Error in the residual bit count after a Reception

ERR 9: Error in the effective length after a Reception

ERR 10: The last received word is not OK (error at bit level)

ERR 11: Status error after a C10 disconnect

Err 12: Error in the received data

Remark:

- Errors from 4 to 9 and error 11 are followed by a dump of the concerned ECB.
- Errors 10 ans 12 are followed by a dump of the receiver data buffer with the indication of the first wrong data and the indication of the expected data.

ECB Description

The Event Control Block is provided to the monitor with the request; it is a seven word long table whose content is as follows:

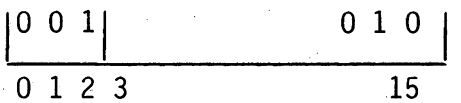
WORD 0	E	File code
WORD 1	Buffer address	
WORD 2	Nb of bits	Requested length
WORD 3	Nb of bits	Effective length
WORD 4	Status	
WORD 5	Reserved	
WORD 6	Control Word	

WORD 0 Bit 0 = Event bit
- Is managed by the monitor
- Reset at request time
- Set when the request is ended.

File Code
To be provided by the user.
The file code is defined at system generation time or by an assign request.

WORD 1 Buffer Address
To be provided by the user.
It is the first address of the user data buffer.

WORD 2 Requested Length
To be provided by the user.
It indicates in characters and bits the desired length of the frame.
Example: Requested length 17 bits.



= 2 characters and 1 bit

WORD 3 Effective Length
Is provided by the monitor on request completion and provides the user the effective length of the transmitted frame.
The effective length has the same format (character and bits) as the requested length.

WORD 4 Status
This information is given by the monitor.
It is meaningful only when the Event bit is set.

WORD 5 Reserved

WORD 6 Control word
That word contains the timer value in multiple of 100ms.
Control word equal to zero implies no time out supervision.

Status Description

The status returned in the ECB contains the result of the transmission:

Bit 0 = 0 Software status
Bit 0 = 1 Hardware status

Software Status

Bit 0 = 0
    1 = Not significant
    2 = Non connected line
    3 = Illegal Request - Line already connected
                        - Invalid order
                        - Disconnect requested on an active line
                        - Abort/Idle requested on an Input file code
4 to 7 = Irrelevant
    8 = Transmission stopped
    9 = Time out request may not be served
   10 = Time over
   11 = Abort requested with a non active line
   12 = File code table overflow
   13 = NS
   14 = NS
   15 = Line busy

Hardware Status

Bit 0 = 1
    1 = NS
    2 = Abort detected
    3 = Idle detected
4 to 7 = Number of true data bits in the last word (if 0, the length is 16 bits)
    8 = NS
    9 = Ring indicator
   10 = End of carrier detection
   11 = Command refused
   12 = Incorrect length
   13 = FCS error
   14 = Throughput error
   15 = Modem not operable

On each request a timer is set its value is:

- 100 ms For a stop request
- 200 ms For a connect or a disconnect request
- 3,5 s   For a read or write request.

Procedure	5111 991 11491	Procedure BHDLC	5111 991 Ø8885
		with addendum PTS8ØØØ	5111 991 11381
Listing	5111 991 08895		
Program	5111 199 69585		

```
                    IDENT    HLCUT

                  * TRX CONTINUOUSLY DATA /FC
                  *
                  * CONNECT LOOPPLUG: CT105-106 (PIN 4-5), 108-107 (20-6) AT LEAST.
                  * LOCAL CLOCK 57 (OR 7 KBITS/SEC), NRZI NOT SELECTED
                  *
                  * CHECK WITH OSCILLOSCOPE:           10 USEC/DIV,10 V/CM
                  * CT103 PIN 2
                  *      PROGRAM RUNS:
                  *      +12V='0' --I   I---I---I                    I---I   I-
                  *      -12V='1'   I---I       I---I---I---I---I---I   I---I
                  *                   0   0   1   1   1   1   1   0   1
                  *                 I----------DATA /FC-----------------I
                  *
                  *      EXECUTE PROGRAM INST-BY-INST UNTIL CIO START:
                  *
                  *       +12V='0'      I---I---I                       I---I---I
                  *       -12V='1'    --I       I---I---I---I---I---I---I       I--
                  *                     0   0   1   1   1   1   1   1   0   0
                  *                       I-----------FLAG--------------I
                  *                       LS                           MS
                  *
     000A         DAREC    EQU      /0A
     000B         DATRX    EQU      /0B
0000              DATA     RES      /40
0080  FFFF                DATA     /FFFF
0082  0000                DATA     0
0084  207F         START    HLT
0086  20BF                INH
0088  0102         BEG      LDK      A1,2
008A  41CA                 CIO      A1,1,DAREC          CONNECT
008C  4BCA                 SST      A3,DAREC
008E  5C04                 RB(4)    *-2
0090  41CB                 CIO      A1,1,DATRX          START DATA OUT
0092  8220                 LDKL     A2,/FCFC
0094  FCFC
0096  420B                 OTR      A2,0,DATRX
0098  4CCB                 SST      A4,DATRX            STATUS
009A  5C06                 RB(4)    *-4                 OTR IF STATUS OK
009C  207F                 HLT
                           END      START
```

```
                        IDENT    HLCUL
                       *
                       * HLCU LOOPS FRAME: FLAG - DATA /FC, /FC - FCS (=CRC) -FLAG
                       *
                       * CONNECT LOOPPLUG: CT103-104 (PIN 2-3), 105-106 (4-5), 113-115 (15-17)
                       *                   CT108-107-109 (20-6-8)
                       * CHECK CORRECT RUNNING:
                       *          1) STOP AFTER INR.(REPLACE /EC08 BY /207F)
                       *             REG A4 MUST CONTAIN /FCFC.
                       *          2) CHECK OSCILLOSCOPE PICTURE:(USE MAGNIFIER)          50 USEC/DIV
                       *             PROGRAM RUNNING:
                       *
                       *    +12V 0       00       000      0 00      0 00  0000   00   0       00
                       *    -12V  111111  111111   11111 1  11111 1  11    111  111 111111  1111
                       *         I-FLAG-II-FLAG-II-DATA--II-DATA--II----FCS-------II-FLAG-II-FLA
                       *
                       *
                       *             PROGRAM NOT RUNNING / INST BUTTON PRESSED:
                       *
                       *    +12V     00       00       00       00
                       *    -12V   1  111111  111111  111111  111111
                       *             I-FLAG-II-FLAG-II-FLAG-I
                       *
                       *
                       * ERROR: DATA FAULT STOPS AT /BA (/BC AT HHP)
                       *        STATUS FAULT KEEPS PROGRAM IN RUN
                       * LOCAL CLOCK 57 (OR 7) KBITS/SEC, NRZI NOT SELECTED
            000A       DAREC    EQU      /0A
            000B       DATRX    EQU      /0B
            0004       INTREC   EQU      4
            0005       INTTRX   EQU      5
0000                   RES      /40
0080  FFFF   DATA     DATA     /FFFF
0082  0000             DATA     0
0084  207F   START    HLT
                       *
                       * MAIN PROGRAM:
0086  87A0   BEG      LDKL     A15,/120
0088  0120
008A  8120             LDKL     A1,STAR
008C  0080  R
008E  8141             ST       A1,8
0090  0008
0092  8120             LDKL     A1,STAT
0094  00C4  R
0096  8141             ST       A1,/A
0098  000A
009A  0102             LDK      A1,2
009C  20BF             INH
009E  41CA             CIO      A1,1,DAREC          CONNECT MODEM
00A0  4CCA             SST      A4,DAREC            STATUS
00A2  5C04             RB(4)    *-2
00A4  2840             ENB
00A6  0105             LDK      A1,5
00A8  41CA             CIO      A1,1,DAREC          START REC
00AA  0302             LDK      A3,2
00AC  43CB             CIO      A3,1,DATRX          START TRX
00AE  5F02             RB       *                   WAIT FOR INTERRUPT
                       *
                       * REC INT ROUTINE
00B0  4DCA   STAR     SST      A5,DAREC
00B2  500C             RF(0)    *+/E
00B4  4C0A             INR      A4,0,DAREC          DATA TO A4
00B6  EC08             CWR      A4,A2
00B8  5002             RF(0)    *+4                 HLT IF DATA FAULT
00BA  207F             HLT
00BC  418A             CIO      A1,0,DAREC          STOP REC
00BE  F03E             RTN      A15
00C0  41CA             CIO      A1,1,DAREC
00C2  F03E             RTN      A15
                       *
                       * TRX INT ROUTINE
00C4  4ECB   STAT     SST      A6,DATRX
00C6  500A             RF(0)    *+/C
00C8  8220             LDKL     A2,/FCFC            DATA /FCFC
00CA  FCFC
00CC  420B             OTR      A2,0,DATRX
00CE  418B             CIO      A1,0,DATRX          STOP OUTPUT
00D0  F03E             RTN      A15
00D2  43CB             CIO      A3,1,DATRX
00D4  F03E             RTN      A15
```

24 SYNCHRONOUS LINE CONTROL UNIT P845-160 (SLCUZ)

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24.1 SLCUZ IDENTIFICATIONS

Type number : P845-170

Function : Datacom control Unit for synchronous data transfer with BSC procedures and a V24 interface. (1 line)

Test program : BSLCUZ

1/O channel : IOP or Program channel

Power consumption : +5V, 2,2A
+12V, 100mA
-12V, 45mA

12NC code (on sticker) : 5111 199 6140x
x = modification number

Devices : MODEM (synchronous, V28).
Direct connection to VDU (with BSC procedure).
Direct connection with SLCUZ of other system.

24.2 FACILITIES

- CCITT V24/28 interface
- Half or full duplex connection
- Synchronous character oriented procedures (BSC)
- comprises separte transmit and receive circuits each of which has its own CU address and interrupt and break priority levels
- optional binary coded interrupt system (for use with UPL Bus only)
- Connection types : Point to point, multi-point or local connection)
- Terminal type : Synchronous (block transfer)
- Bit transport type : Synchronous (uses DCE clock for connections via a DCE, or internal CU clock for local connection

- Transmission Rates :
  Connections via a DCE : - up to 9600 bits/second on half duplex
  - up to 4800 bits/second on full duplex
  Local connection : - 600,1200,2400,4800,9600 bits/sec on half duplex
  - 600,1200,2400,4800, bits/second on full duplex
- Transmission Codes : USASCII,EBCIDIC
- Error Checking:
  - with ASCII code : VRC,LRC, CRC
  - with EBCDIC code : CRC only

24.3 INSTALLATIONS DETAILS

24.3.1 STRAPSETTING (Figure 24.1)

Description of the straps:

ADDL = Remote IPL address

FREQ = Line speed of receiver and transmitter.

ADR = Control Unit address.

BIEC = Binary Coded Interrupt level.

1314 = Local or Modem connection (internal or external clock).

108 = CT108 signal switched or constant active.

107 = Time out selection for CT107.

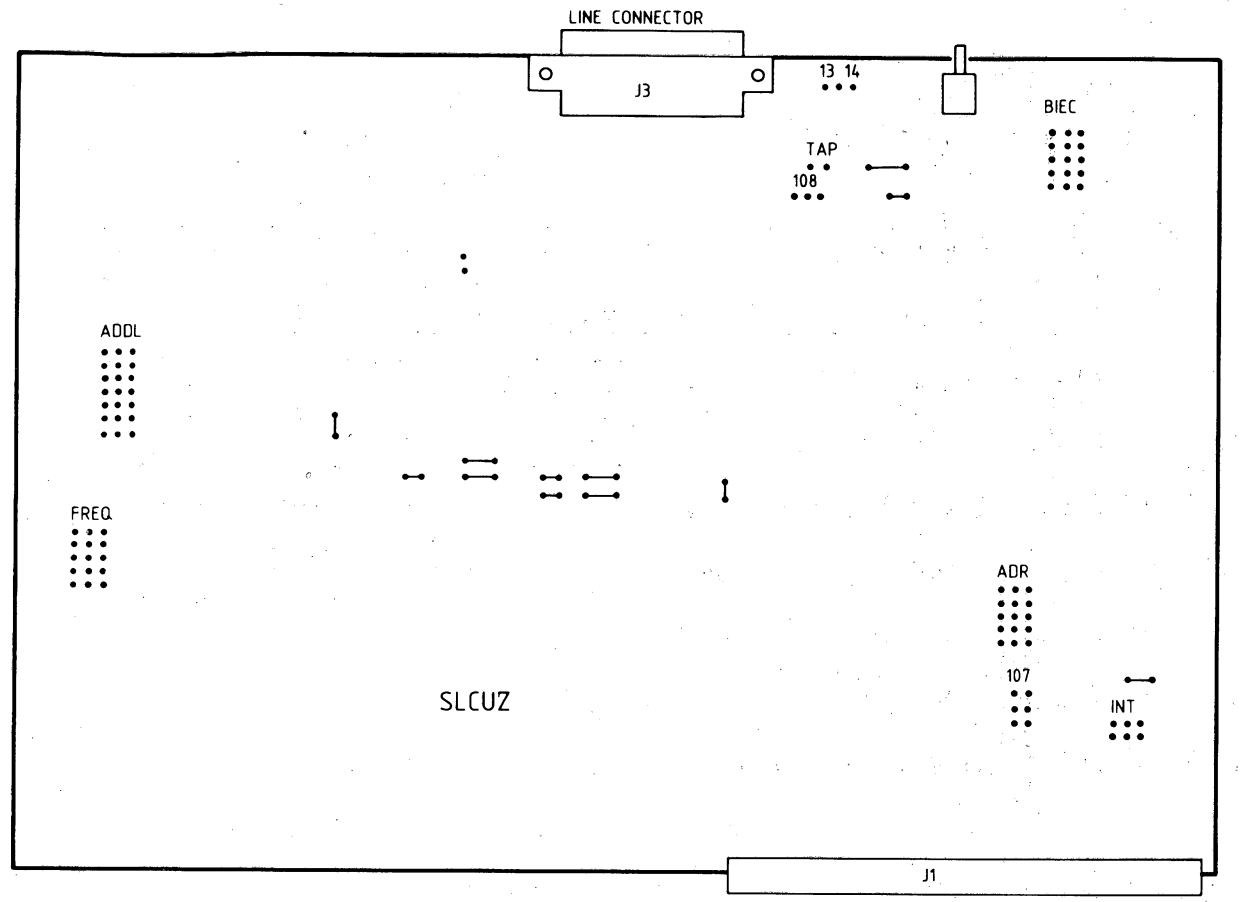
INT = BCI or Direct interrupt, and interrupt destination.

24.3.2. INTERRUPT AND BREAK WIRING (Figure 24.2)

Back panel wiring:

Interrupts: - Receiver interrupt : 1CO5 to CPU
- Transmitter interrupt : 1CO4 to CPU

Breaks : - Receiver break : 1AO5 to IOP
- Transmitter break : 1AO4 to IOP



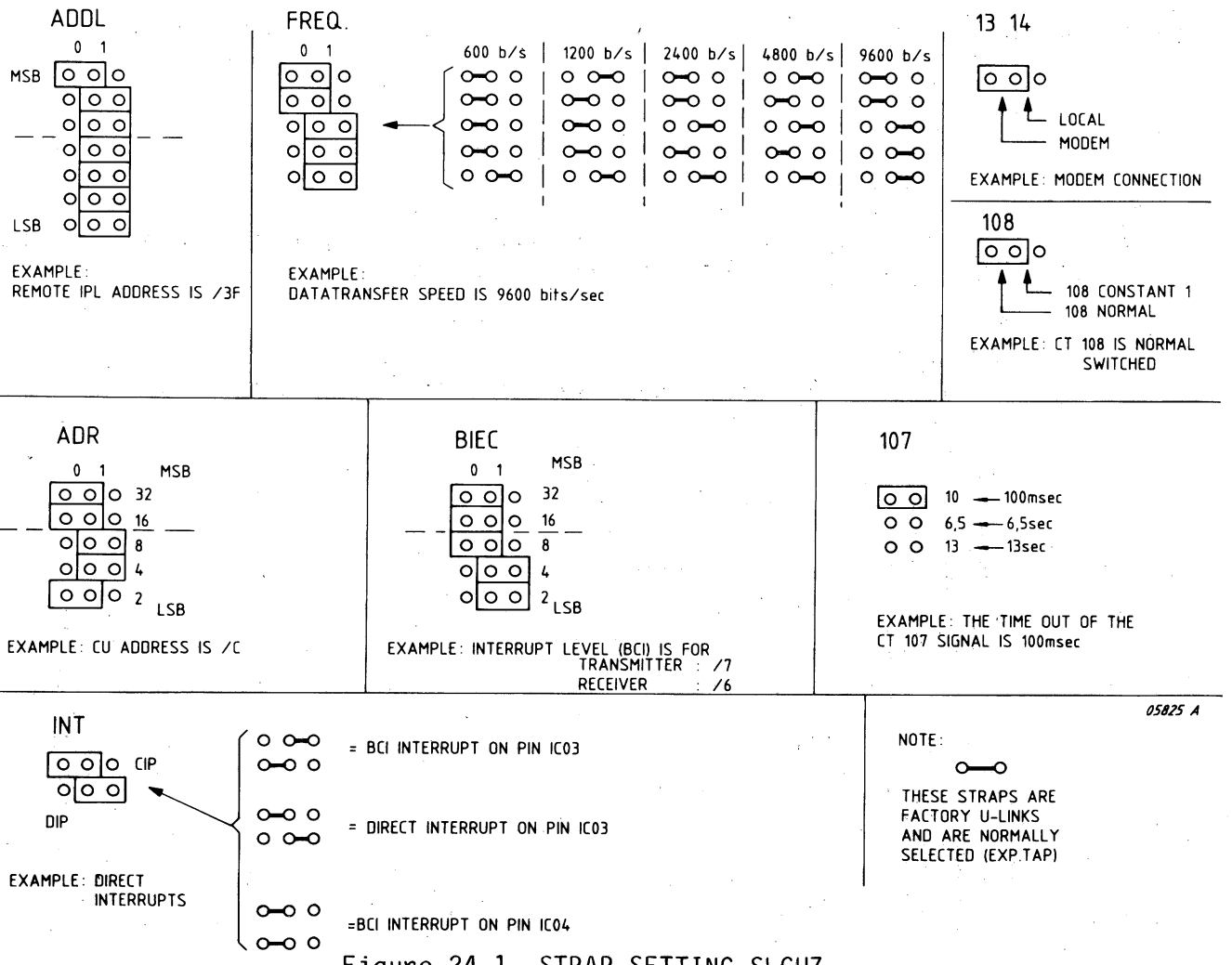
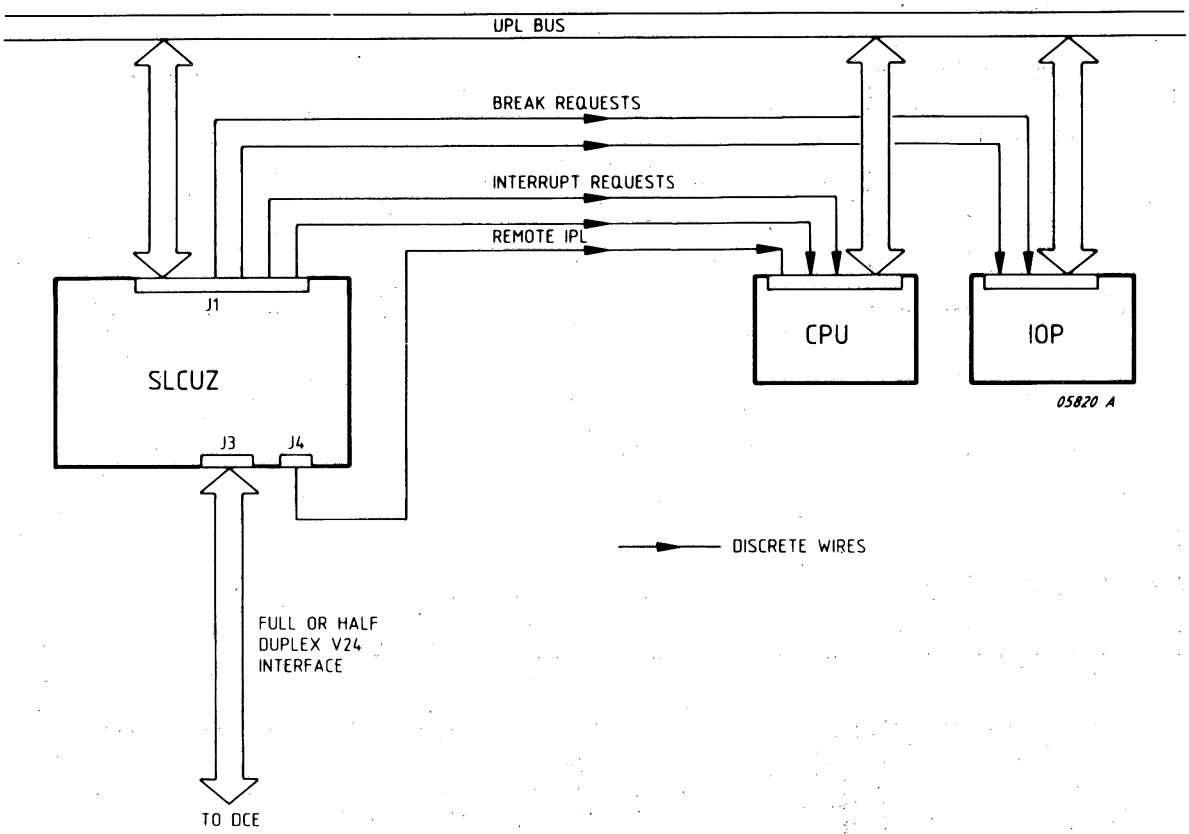


Figure 24.1 STRAP SETTING SLCUZ



Note: If this card is used with a UPL Bus and Binary Coded Interrupts, the discrete Interrupt Requests are not connected.

Figure 24.2 : INTERRUPT AND BREAK WIRING

24.4 INTERFACE CONNECTIONS

24.4.1 MODEM CONNECTION (Figure 24.3)

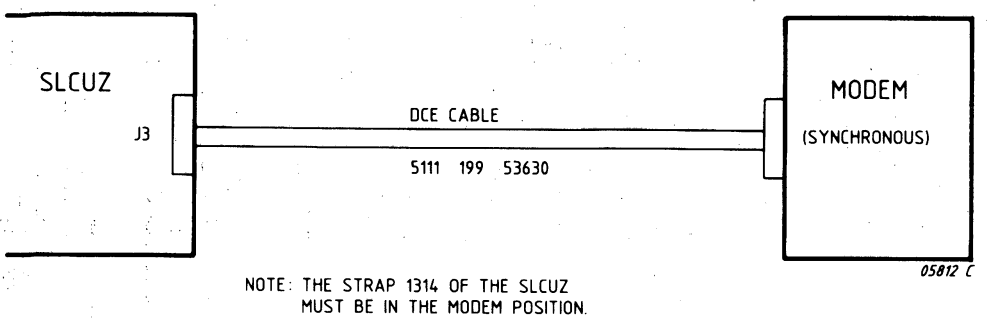


Figure 24.3 MODEM CONNECTION

2.4.4.2 LOCAL CONNECTION (FIGURE 24.4)

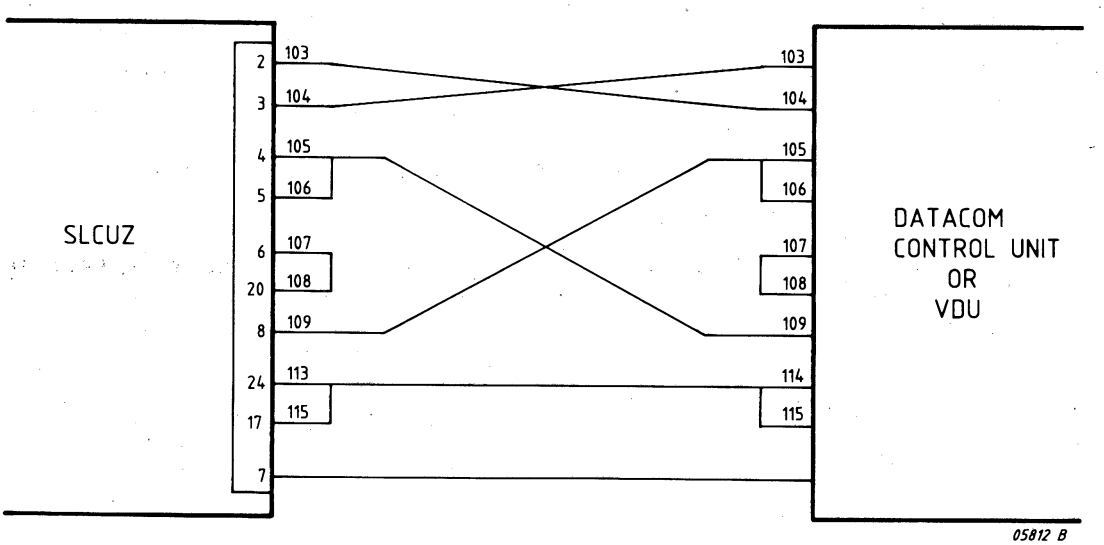


Figure 24.4 LOCAL CONNECTION

PIN No.	Signal Mnemonic	Signal Function
3J01	CT101	Protective ground
3J02	CT103	Transmitted data
3J03	CT104	Received data
3J04	CT105	Request to send
3J05	CT106	Ready for sending (clear to send)
3J06	CT107	Data set ready
3J07	CT102	Logical ground
3J08	CT109	Data carrier detect
3J09-14	---	not used
3J15	CT1314	Transmitter signal element timing (CT114 for connection via a DCE, CT113 for local connec.)
3J16	---	not used
3J17	CT115	Receiver signal element timing
3J18	CT141	Local loopback
3J19	---	not used
3J20	CT108/1	Connect data set to line
	CT108/2	Data terminal ready
3J21	CT140	Remote loopback
3J22	CT125	Calling indicator
3J23	CT111	Data signalling rate selector
3J24	CT113	Transmitter signal element timing (from CU)
3J25	CT142	Test loop indicator

All signals comply with CCITT V24 specifications

Table 24.1: V24 INTERFACE (CONNECTOR J3)

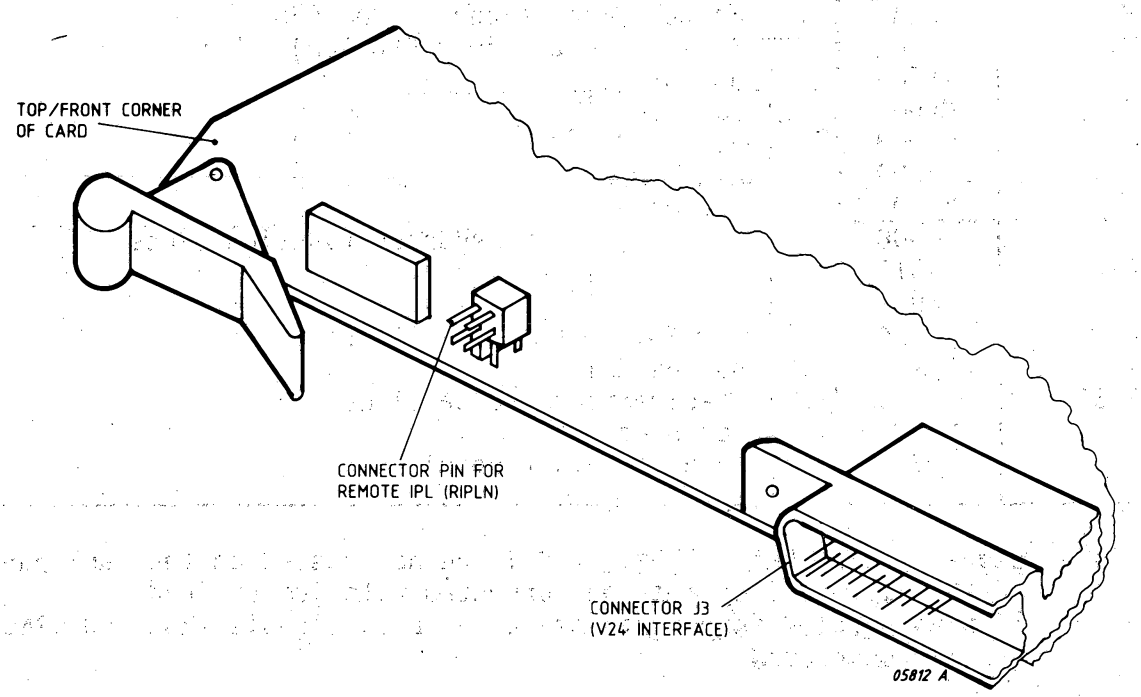


Figure 24.5: CONNECTOR PIN FOR REMOTE IPL

Pin No.	Signal Mnemonic	Signal Function
1A01	-12VL	Power Supply (V24 Interface Drivers)
1A02	+5VM	not used
1A03	INCL	Clock input for Binary Coded Interrupt (from CPU)
1A04	BRIN	Break request - Transmitter (to IOP)
1A05	BRON	Break request - Receiver (to IOP)
1A06,9,12 22	0V	Logical Ground
1A07	RSLN	Reset Signal (from power supply unit)
1A08	ACN	Accept command (to CPU)
1A10	TSMN	Timing signal (to CPU/IOP)
1A11	TMRN	not used
1A13	MAD01	not used
1A14	MAD03	
1A15	MAD05	not used
1A16	MAD07	not used — Address/function lines
1A17	MAD09	
1A18	MAD11	
1A19	MAD13	
1A20	MAD15	
1A21	WRITE	not used
1A23-30	BI000N-07N	Bi-directional data lines
1A31	+12VM	not used
1A32	+5VL	Power supply (logic)
1C01	+12VL	Power supply (V24 Interface Drivers)
1C02	+5VM	not used
1C03	BCI	Binary coded interrupt (to CIP)
1C04	IRNBCI	Discrete Int. -TRX (to CPU) or B.C.Int. (to DIP)
1C05	IRON	Discrete interrupt request - receiver (to CPU)
1C06,9,12 22	0V	Logical Ground
1C07	PWFN	Power failure signal (from power supply unit)
1C08	CLEARN	Master clear signal (from CPU)
1C10	TMPN	Timing signal (from CPU/IOP)
1C11	TMEN	not used
1C13	MAD00	not used
1C14	MAD02	not used
1C15	MAD04	
1C16	MAD06	not used
1C17	MAD08	Address/function lines
1C18	MAD10	
1C19	MAD12	
1C20	MAD14	
1C21	CHA	not used
1C23-30	BI008N-15N	Bi-directional data lines
1C31	+12VM	not used
1C32	+5VL	Power supply (logic)

Note: signals BRON, BR1N, IRON, IRNBCI are not bussed on the back panel of the system. They must be connected with jumper leads.
If binary coded interrupts are used (BCI) signals IRON and IRNBCI are not connected.

Table 24.2: BUS CONNECTIONS (CONNECTOR J1)

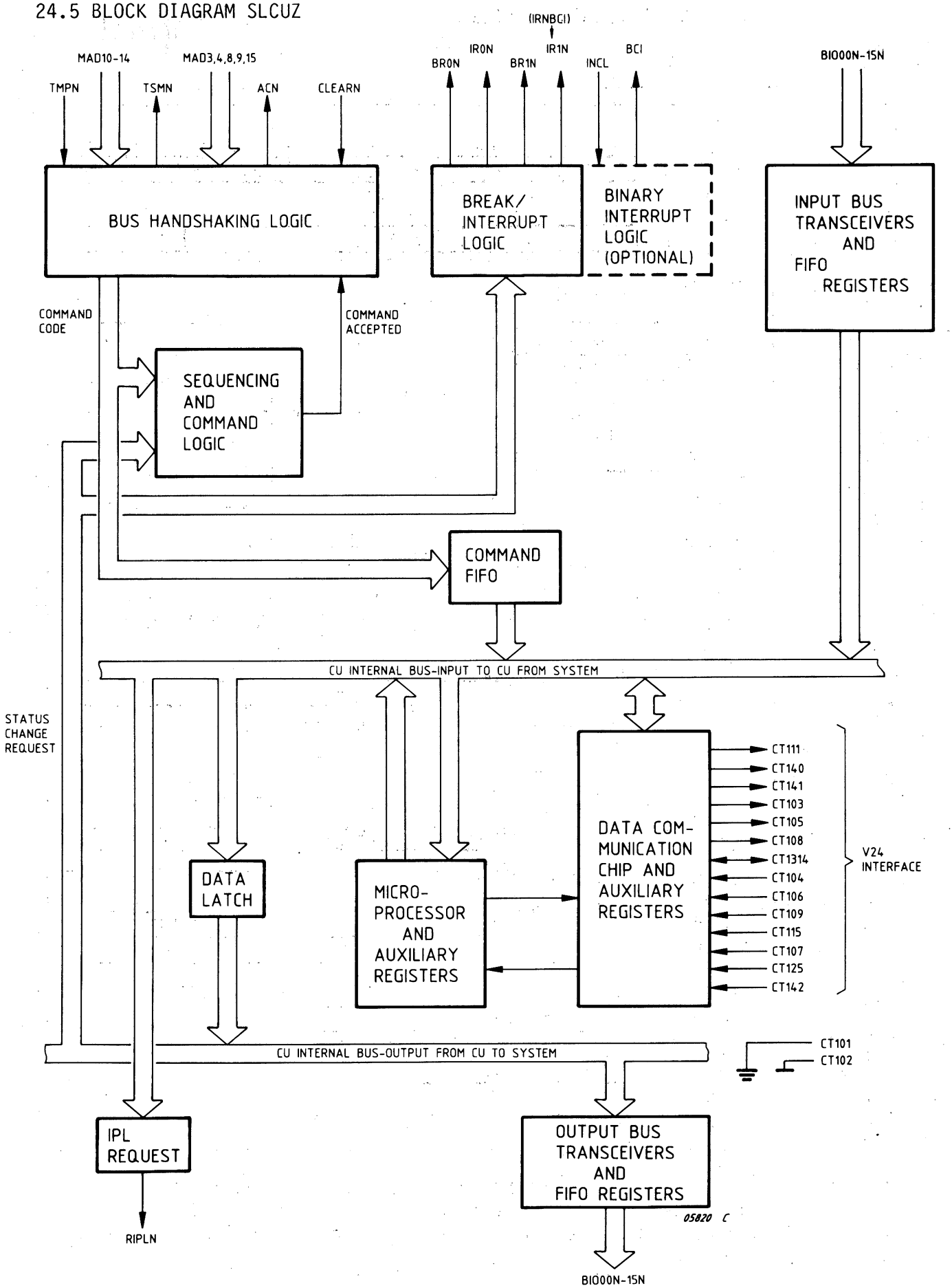
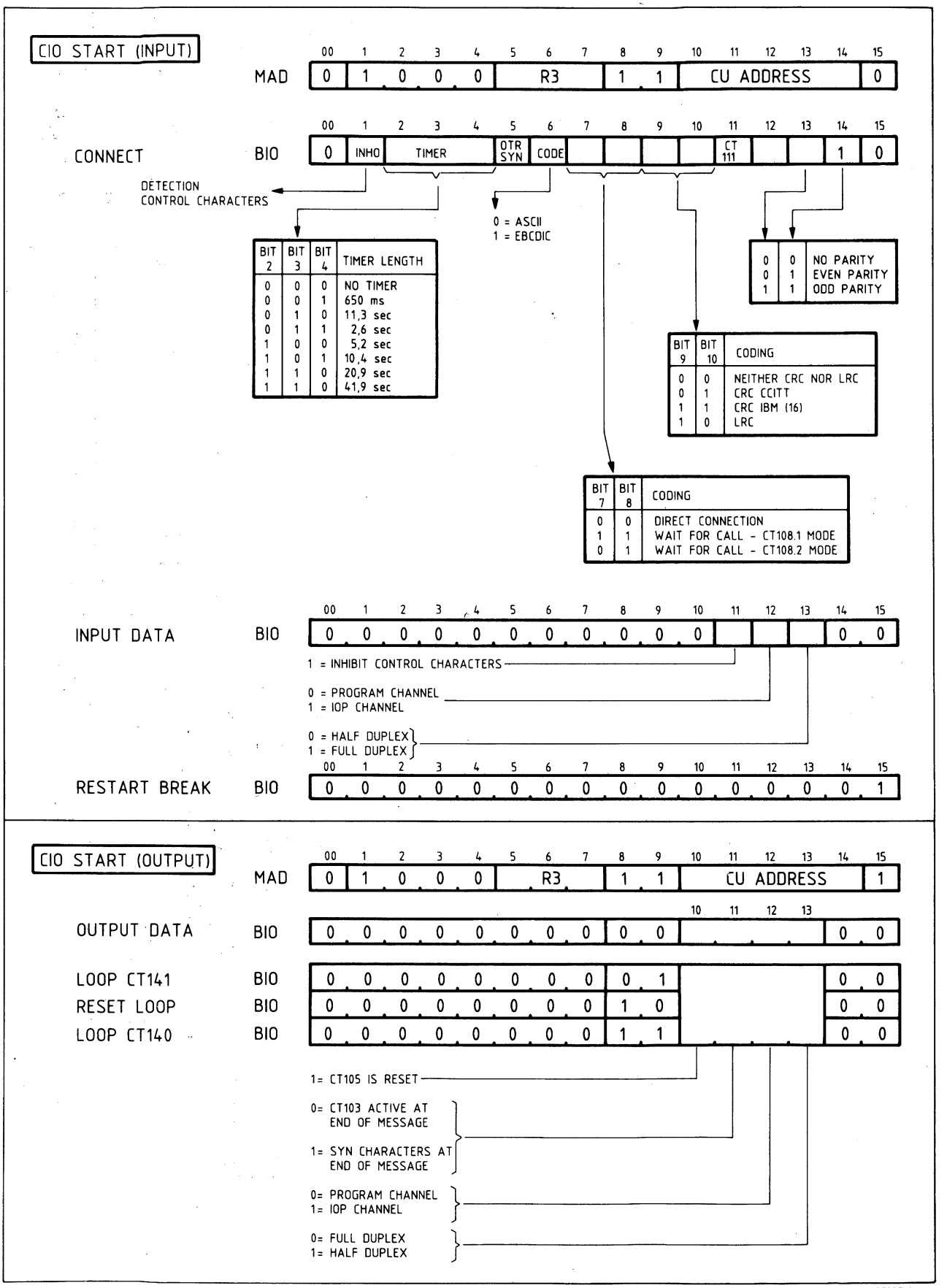
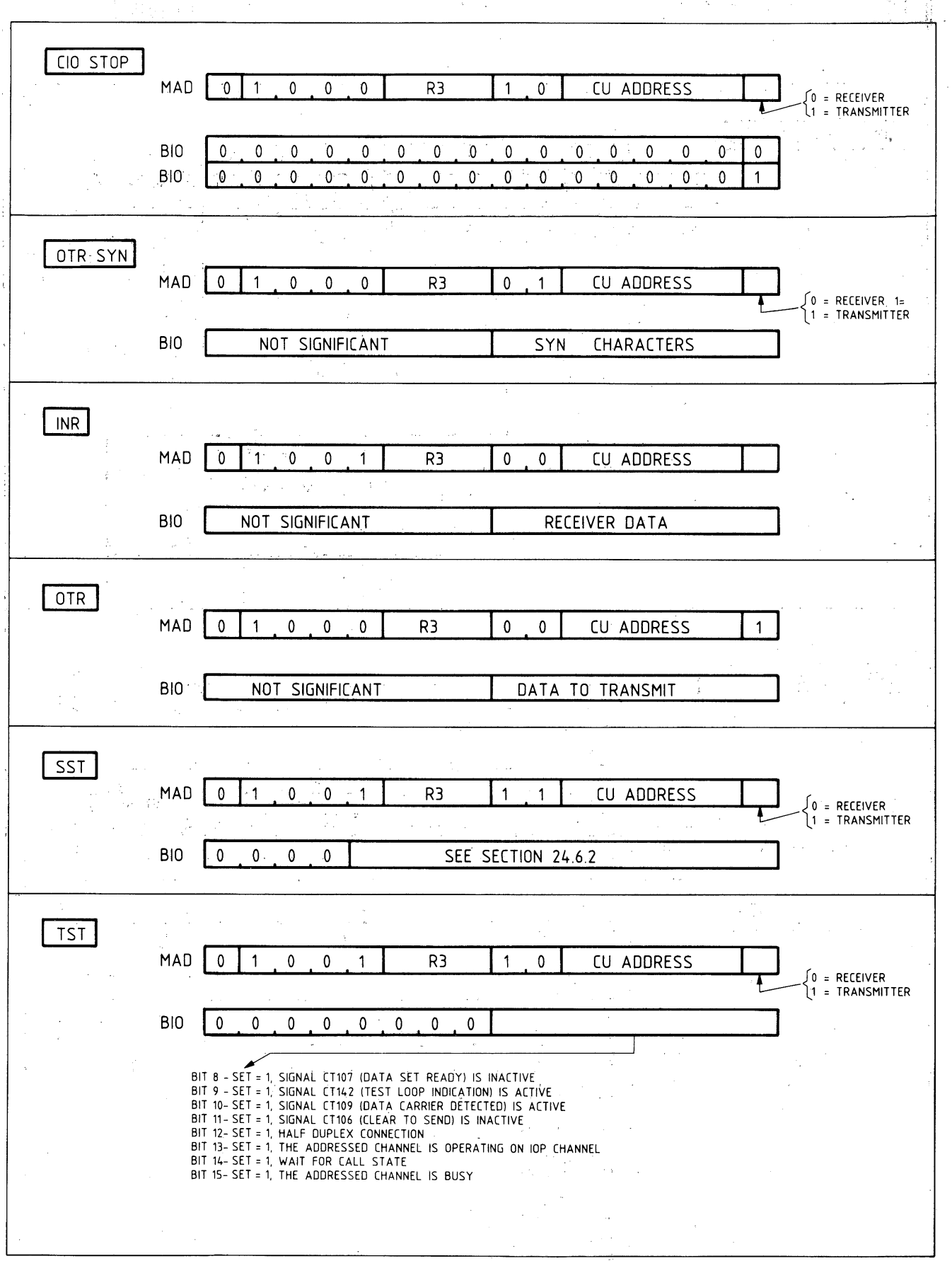


Figure 24.6 BLOCK DIAGRAM SLCUZ

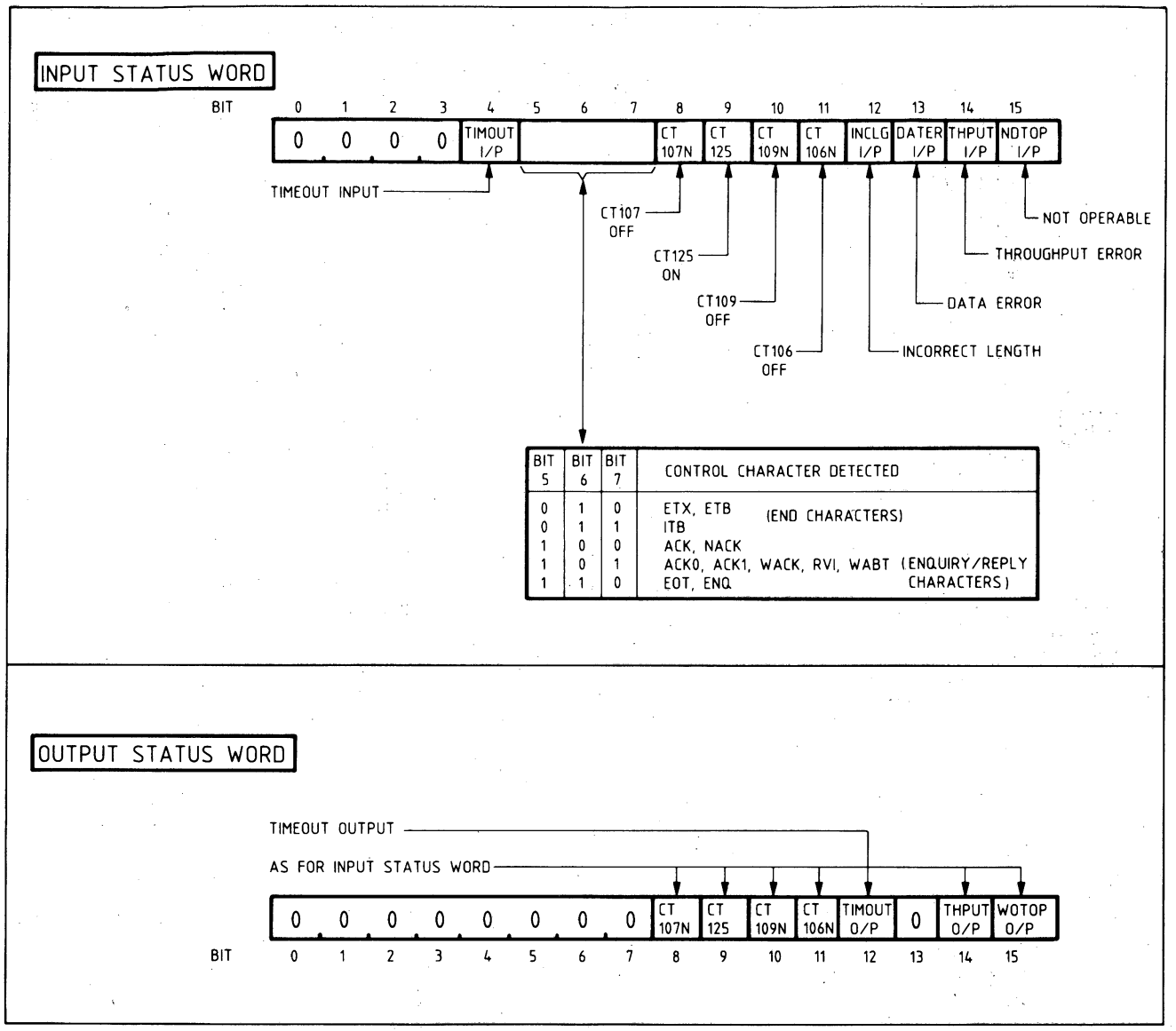
24.6 HARDWARE SOFTWARE INTERFACE DETAILS

24.6.1 COMMANDS




CIO STOP
MAD
0 1 0 0 0 R3 1 0 CU ADDRESS
0 = RECEIVER
1 = TRANSMITTER
BIO
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
BIO
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
OTR SYN
MAD
0 1 0 0 0 R3 0 1 CU ADDRESS
0 = RECEIVER 1=
1 = TRANSMITTER
BIO
NOT SIGNIFICANT
SYN CHARACTERS
INR
MAD
0 1 0 0 1 R3 0 0 CU ADDRESS
BIO
NOT SIGNIFICANT
RECEIVER DATA
OTR
MAD
0 1 0 0 0 R3 0 0 CU ADDRESS 1
BIO
NOT SIGNIFICANT
DATA TO TRANSMIT
SST
MAD
0 1 0 0 1 R3 1 1 CU ADDRESS
0 = RECEIVER
1 = TRANSMITTER
BIO
0 0 0 0
SEE SECTION 24.6.2
TST
MAD
0 1 0 0 1 R3 1 0 CU ADDRESS
0 = RECEIVER
1 = TRANSMITTER
BIO
0 0 0 0 0 0 0 0
BIT 8 - SET = 1, SIGNAL CT107 (DATA SET READY) IS INACTIVE
BIT 9 - SET = 1, SIGNAL CT142 (TEST LOOP INDICATION) IS ACTIVE
BIT 10- SET = 1, SIGNAL CT109 (DATA CARRIER DETECTED) IS ACTIVE
BIT 11- SET = 1, SIGNAL CT106 (CLEAR TO SEND) IS INACTIVE
BIT 12- SET = 1, HALF DUPLEX CONNECTION
BIT 13- SET = 1, THE ADDRESSED CHANNEL IS OPERATING ON IOP CHANNEL
BIT 14- SET = 1, WAIT FOR CALL STATE
BIT 15- SET = 1, THE ADDRESSED CHANNEL IS BUSY
05937 B

24.6.2 STATUS DESCRIPTION



05939

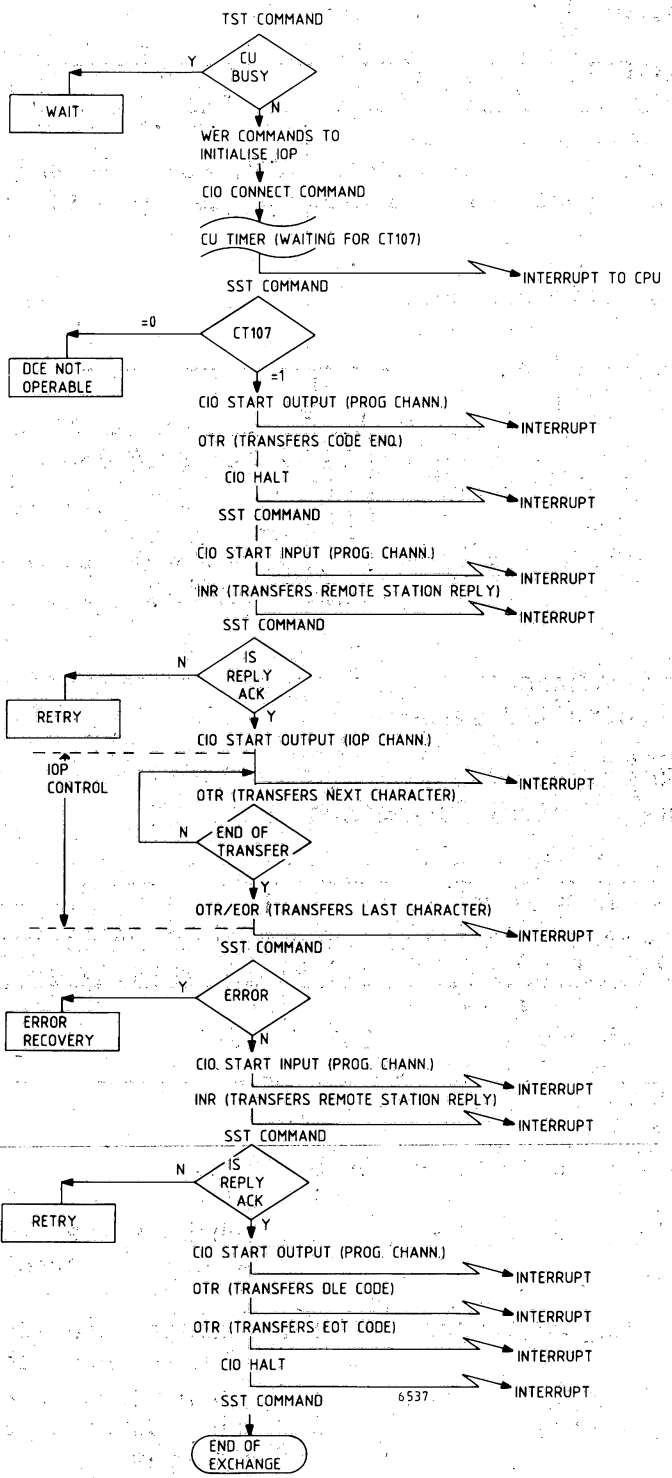


Figure 24.7 PROGRAMMING FLOWCHART

24.7 SHORT DESCRIPTION TESTPROGRAM

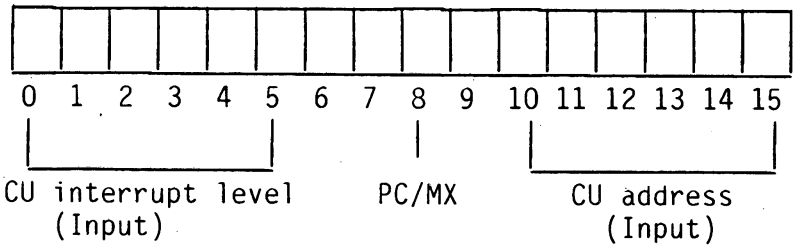
BSLCUZ

RUNNING THE TEST PROGRAM

PROGRAM INITIALIZATION

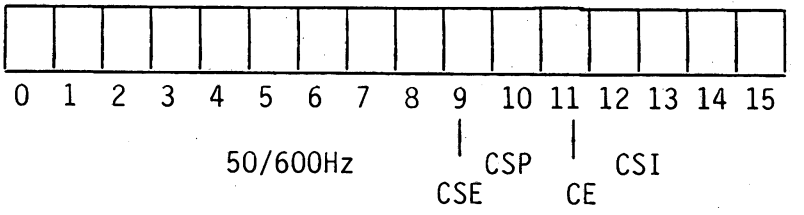
When the program has stopped at address/700, A8-, A9- and A10-registers must be initialized with the appropriate parameters, as follows:

A8-register: Control Unit Parameters



Bit 8: 0 : IOP channel
1 : Programmed channel

A9-register : Program Control Parameters



Bit 7 : Mains frequency selection 0 : 50Hz
1 : 60Hz
Bit 9 : Clear stop on error 1 : Inhibits the stop at /5F0 in case of error.

Bit 10 : Clear stop on program 1 : Inhibits the stop at /700 after running the program (loop on tests again)
Bit 11 : Clear editing 1 : Inhibits error and information messages.
Bit 12 : Clear stop on information 1 : Inhibits information messages and stops at /5E0

A10-register : Checks to be run

Set the bits corresponding to the required check number to 1.
(i.e, bit0 = check0, bit 1 = check1)

PROGRAM EXECUTION

The program execution is started by:

- Push the MC button
- Push the RUN button

A message is produced on the operator's panel, as follows :

```
FIXED CONFIGURATION: A,B,C,D,E, OR F
```

The response may be A,B,C,D,E,OR F. If the response is none of them, according to the set of checks selected by A10-register, a list of questions is produced on the operator's console, as follows:

```
LOW SPEED: (Y OR NO) N
DIRECT CONNECTION: (Y OR N) Y
STANDARD SYN. PATTERN: (Y OR N) Y
AUTO.SYN.GENERATION: (Y OR N) Y
FULL DUPLEX: (Y OR N) Y
ALARM RECEIVE MODE: (0 1 OR 2)
HARD TIMER VALUE: (0 1 OR 2)
FOR 0.1, 6.5 OR 13 SEC. 0
TEST LOOP: (Y OR N) N
```

The answer may be YES or NO (only the first character is tested)
0,1 or 2 (only the first figure is tested)
one or two hexadecimal digits (strictly)
followed by carriage return.
The Rubout character /5F deletes the previous entered character.

After the initialization dialoque via the operator's console, the program links automatically the checks in accordance with the initialization of A10-register, and will stop at address /700 after one cycle.

The operator can stop the program and return to address /700 at any time by pushing the INT button, if the program permits the interrupts.

PARASITIC INTERRUPTS

Any interrupt from a level different from that loaded in A8-register is considered as a parasitic interrupt and the program stops and returns to address /700.

DESCRIPTION OF THE CHECKS

IF0000 : Recognition of I/O commands

IF0001 : Evolution of the sequensor

IF0002 : Elementary transmission

IF0003 : Detection of special characters

IF0004 : Parity and BCC generation

IF0005 : Parity and BCC errors detection

IF0006 : Throughput error detection

IF0007 : Incorrect length detection

IF0008 : IPL frame recognition

24.8 SHORT ROUTINE

```
                        IDENT    SLCUZT
                        *
                        * THIS PROGRAM TRX: SYN-SYN-'U'-PAD-PAD WITH SLCUZ
                        *
                        *
                        *
      000A      DAREC   EQU      /0A
      000B      DATRX   EQU      /0B
0000                    RES      /40
0080  FFFF              DATA     /FFFF,0
0082  0000
0084  010A      START   LDK      A1,/A              CONNECT,SYN=/16
0086  0255              LDK      A2,/55             DATA 'U'
0088  207F      HLT     HLT
008A  20BF              INH
008C  41CA      CIO     CIO      A1,1,DAREC         CONNECT
008E  5C04              RB(4)    *-2
0090  4BCA              SST      A3,DAREC           CHECK ON CONNECT
0092  5C04              RB(4)    *-2
0094  0400              LDK      A4,0
0096  44CB              CIO      A4,1,DATRX
0098  5C04              RB(4)    *-2                START DATA TRANSFER
009A  420B              OTR      A2,0,DATRX
009C  5C04              RB(4)    *-2                'U' TRX
009E  448B              CIO      A4,0,DATRX         STOP TRX
00A0  4BCB              SST      A3,DATRX           STATUS?
00A2  5C04              RB(4)    *-2
00A4  5F14              RB       *-/12
                        END      START
```

25 ASYNCHRONOUS MEDIUM SPEED LINE MULTIPLEXOR P845-180 (AMA4Z)

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	25.5	CONNECTOR 8J (TEST)	25-8
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25.1 AMA4Z IDENTIFICATIONS

Type number	:	P845-180
Function	:	Datacom Control Unit for asynchronous data transfer; can control 4 lines with V24 interface.
Test program	:	?
I/O channel	:	DMA channel
Power consumption	:	+5V (Typ) 2.8A +12V " 150mA -12V " 125mA
12NC code (on sticker)	:	5111 199 5374X X = modification level
Devices	:	- MODEM (asynchronous) - Direct connection to a VDU

25.2 FACILITIES

The features of the AMA4Z:
-direct memory access (DMA)
-asynchronous data transfer
-4 lines can be connected in full duplex data transfer
-the interface to the modem is V24/V28
-one line can be selected for V24/V28 or V24/V11
-the line parameters are selectable by software
-BREAK detection
-remote IPL (only for one line)
-special character detection
-test loop facillity (V54)

Specifications:

-data transfer	:	half or full duplex, 4 lines
-bit transport type	:	asynchronous.
-transmission speed	:	75 up to 19200 bit/sec.
-parity bit	:	Even, Odd, Forced to 0, Forced to 1, or No parity.
-stopbit	:	1, 1.5, or 2 bit.
-character length	:	5, 6, 7, or 8 bit.
-interface	:	V24/V28, or for line 1 V24/V11.
-remote IPL CODE	:	EOT, R,J. (04,52,4A)

25.3 INSTALLATIONS DETAILS

25.3.1 STRAP SETTING

The meaning of the straps in figure 25.1 is as follows:

ADA = 6 straps for selecting the control unit address.
V11/V28 = selects the interface of line 1, V11 (double current) or V28.
IPL = enable or inhibits the remote IPL detection for line 1. (output on connector 7J)

The selection of the datacom parameters is done by the software.

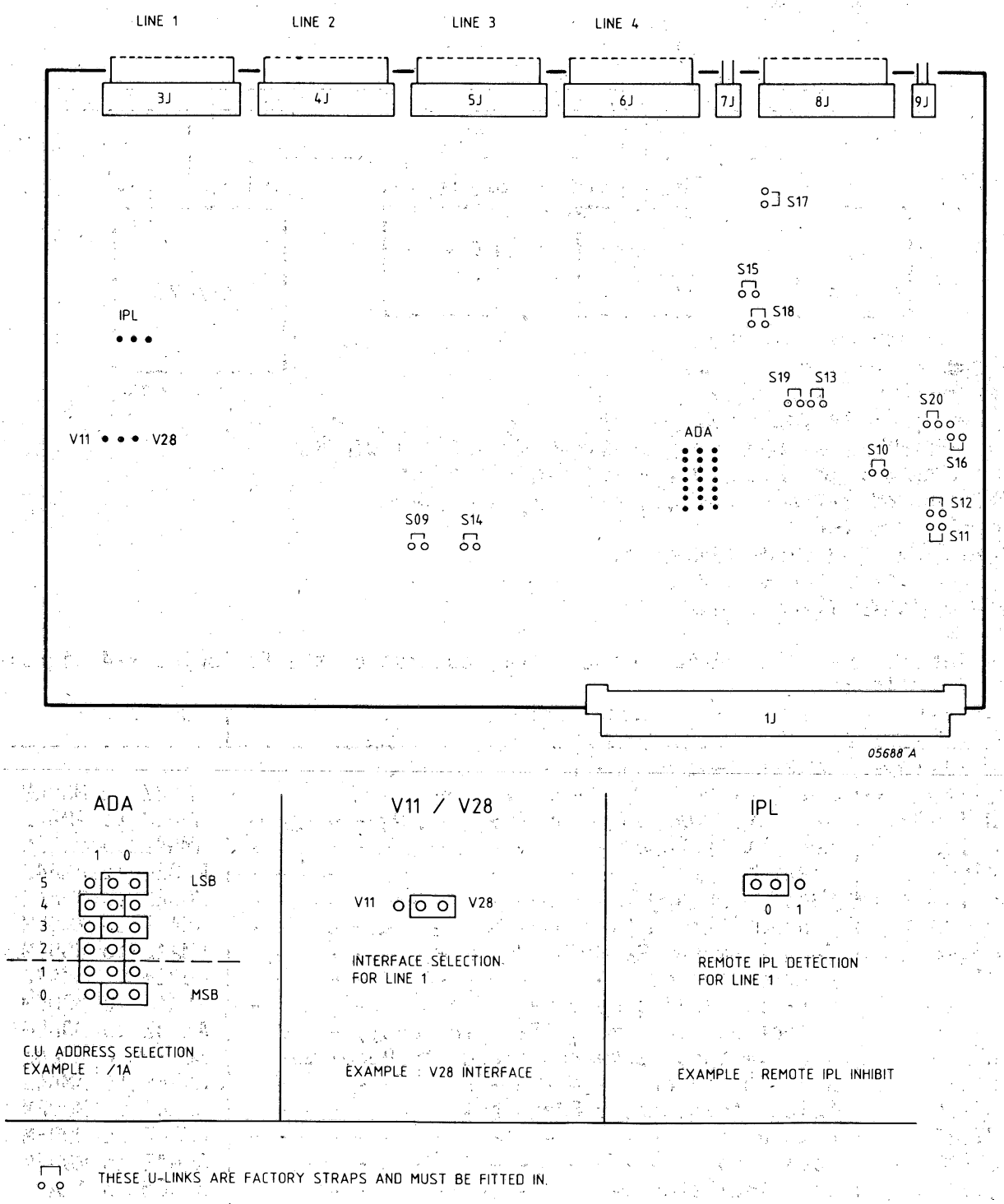


Figure 25.1 STRAP SETTING

25.3.2 OKO/OKI-WIRING

For mounting the AMA4Z in the system-rack, it is important that the signal OKO/OKI is connected to the AMA4Z. (figure 25.2).
Therefor a wire must be made from the last DMA control unit to the AMA4Z at the back-side of the system rack.

If the AMA4Z is mounted beside controle-units, which are chaining the OKO/OKI signals internally, it is not necessary to make a wire at the back-side of the system rack.

pinning: OKI = 1B07
OKO = 1B08

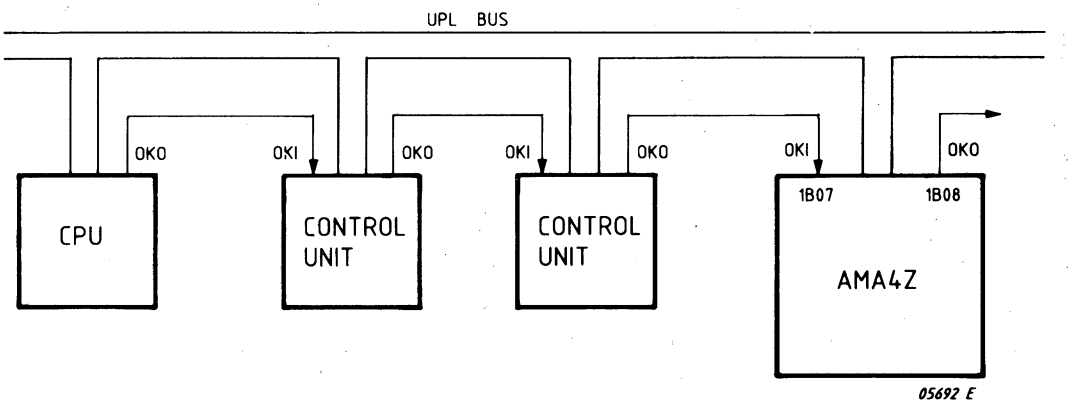


Figure 25.2 OKO/OKI WIRING

25.4 INTERFACE CONNECTIONS

25.4.1 MODEM CONNECTION

The interface of the AMA4Z to the modem, consist of the following V24 signals:

signal	description	direction
CT102	Common Return	
CT103	Transmit Data	AMA4Z to MODEM
CT104	Receive Data	MODEM to AMA4Z
CT105	Request to Send	AMA4Z to MODEM
CT106	Clear to Send	MODEM to AMA4Z
CT107	Data Set Ready	MODEM to AMA4Z
CT108-1	Connect Set to Line	AMA4Z to MODEM
CT108-2	Data Terminal Ready	AMA4Z to MODEM
CT109	Carrier Detect	MODEM to AMA4Z
CT111	Data Signalling Rate Detector	AMA4Z to MODEM
CT116	Select DCE Equipment (Set Line Busy)	AMA4Z to MODEM
CT119	Receive Data Backwards (ready to Receive)	MODEM to AMA4Z
CT125	Ring Indicator	MODEM to AMA4Z
CT126	Select Transmitter Frequency	AMA4Z to MODEM
CT140	Remote Loop	AMA4Z to MODEM
CT141	Local Loop	AMA4Z to MODEM
CT142	Test Indicator	MODEM to AMA4Z

25.4.2 LOCAL CONNECTION

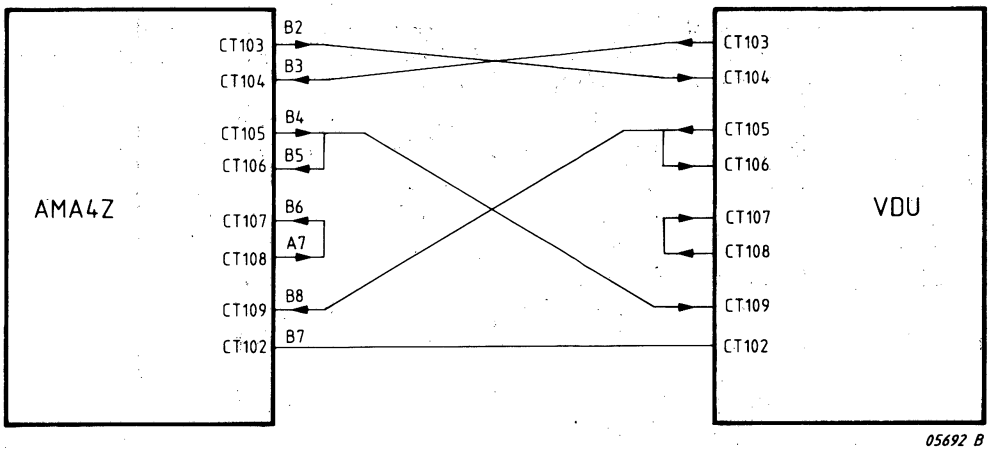


Figure 25.3 LOCAL CONNECTION

25.4.3 CONNECTORS

- connector 1J: UPL bus
- connector 3J: Line 1 (V24 interface)
- connector 4J: Line 2 (V24 interface)
- connector 5J: Line 3 (V24 interface)
- connector 6J: Line 4 (V24 interface)
- connector 7J: Remote IPL
- connector 8J: Test tool (for stepping through micro program)
- connector 9J: Test (EMADAN)

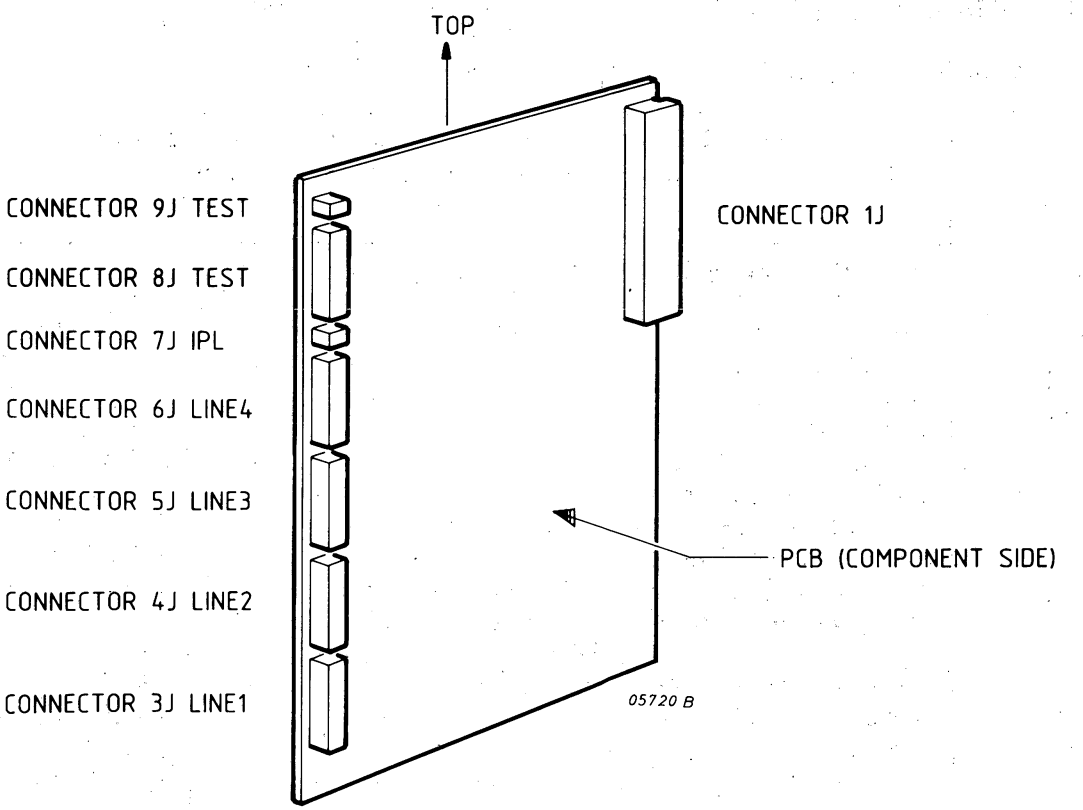
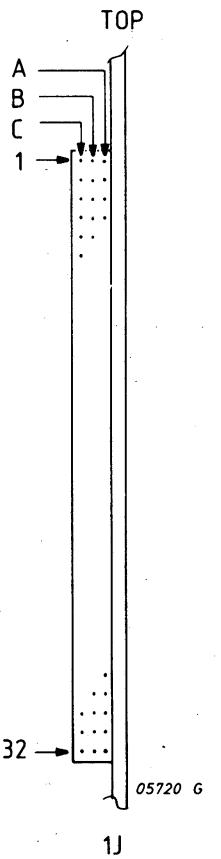


Figure 25.4 CONNECTORS

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01	+12VL	1B01	ERON	1A01	-12VL
1C02		1B02	BUSRN	1A02	
1C03	BCI	1B03	MSN	1A03	INCL
1C04	*	1B04	OV	1A04	*
1C05	*	1B05	BSYN	1A05	*
1C06	OV	1B06	OKO	1A06	OV
1C07	PWFN	1B07	OKI	1A07	RSLN
1C08	CLEARN	1B08	RTCN	1A08	ACN
1C09	OV	1B09	BAWOFN*	1A09	OV
1C10	TMPN	1B10	STOPN	1A10	TSMN
1C11	TMEN	1B11	OV	1A11	TMRN
1C12	OV	1B12	MADE0	1A12	OV
1C13	MAD00	1B13	MADE1	1A13	MAD01
1C14	MAD02	1B14	OV	1A14	MAD03
1C15	MAD04	1B15	MADE2	1A15	MAD05
1C16	MAD06	1B16	MADE3	1A16	MAD07
1C17	MAD08	1B17	MADE4	1A17	MAD09
1C18	MAD10	1B18	MADE5	1A18	MAD11
1C19	MAD12	1B19	MADE6	1A19	MAD13
1C20	MAD14	1B20	MADE7	1A20	MAD15
1C21	CHA	1B21	OV	1A21	WRITE
1C22	OV	1B22	*	1A22	OV
1C23	BIO08N	1B23	*	1A23	BIO00N
1C24	BIO09N	1B24	*	1A24	BIO01N
1C25	BIO10N	1B25	*	1A25	BIO02N
1C26	BIO11N	1B26	OV	1A26	BIO03N
1C27	BIO12N	1B27	*	1A27	BIO04N
1C28	BIO13N	1B28	*	1A28	BIO05N
1C29	BIO14N	1B29	*	1A29	BIO06N
1C30	BIO15N	1B30	*	1A30	BIO07N
1C31		1B31	+5VL	1A31	
1C32	+5VL	1B32	+5VL	1A32	+5VL

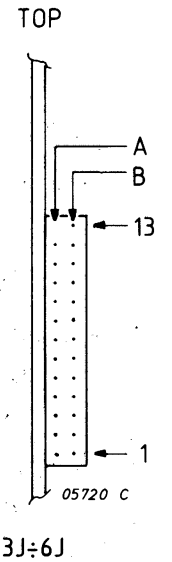


* These signals are not connected to the back panel bus.

Table 25.1 CONNECTOR 1J (UPL BUS)

PIN NUMBER	SIGNAL NAME		PIN NUMBER	SIGNAL NAME
A01	OUTAN		B01	
A02			B02	CT103
A03	OUTAP		B03	CT104
A04			B04	CT105
A05	CT141		B05	CT106
A06	INAN		B06	CT107
A07	CT108-1/2		B07	CT102
A08	CT140		B08	CT109
A09	CT125		B09	CT119
A10	CT111		B10	CT116
A11	INAP		B11	CT126
A12	CT142		B12	
A13	DUMMY		B13	

Table 25.2 CONNECTOR 3J (LINE 1)



3J÷6J

PIN NUMBER	SIGNAL NAME		PIN NUMBER	SIGNAL NAME
A01			B01	
A02			B02	CT103
A03			B03	CT104
A04			B04	CT105
A05	CT141		B05	CT106
A06			B06	CT107
A07	CT108-1/2		B07	CT102
A08	CT140		B08	CT109
A09	CT125		B09	CT119
A10	CT111		B10	CT116
A11	INAP		B11	CT126
A12	CT142		B12	
A13	DUMMY		B13	

Table 25.3 CONNECTOR 4J, 5J, 6J (LINE 2, 3, and 4)

PIN NUMBER	SIGNAL NAME
A02	0V
A02	IPLN

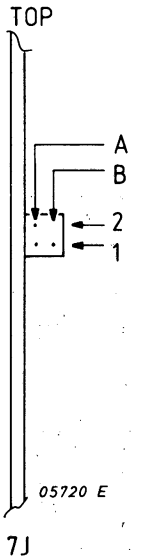


Table 25.4 CONNECTOR 7J (Remote IPL)

PIN NUMBER	SIGNAL NAME		PIN NUMBER	SIGNAL NAME
A01	IVB3N		B01	AD12
A02	IVB4N		B02	AD11
A03	IVB5N		B03	AD10
A04	IVB6N		B04	AD09
A05	IVB7N		B05	AD08
A06	0V		B06	AD07
A07	MCLKAN		B07	AD06
A08	0V		B08	AD05
A09	+5V		B09	AD04
A10	+5V		B10	AD03
A11	AD2		B11	IVBON
A12	AD1		B12	IVB1N
A13	RHTN		B13	IVB2N

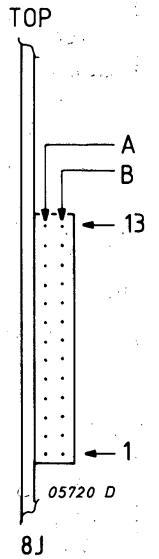


Table 25.5 CONNECTOR 8J (TEST)

PIN NUMBER	SIGNAL NAME
A01	0V
A02	EMADAN
B01	EMADAN
B02	0V

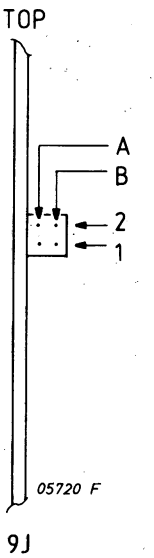


Table 25.6 CONNECTOR 9J (EMADAN)

25.4.4 CABLES

The MODEM cable used for the AMA4Z is of type "PUC".
A maximum of 4 cables can be connected to the AMA4Z

The metal box of the PUC cable is fixed on a rail.
(for pull relief and conducting the shielding)

The 12 NBC of the cable:

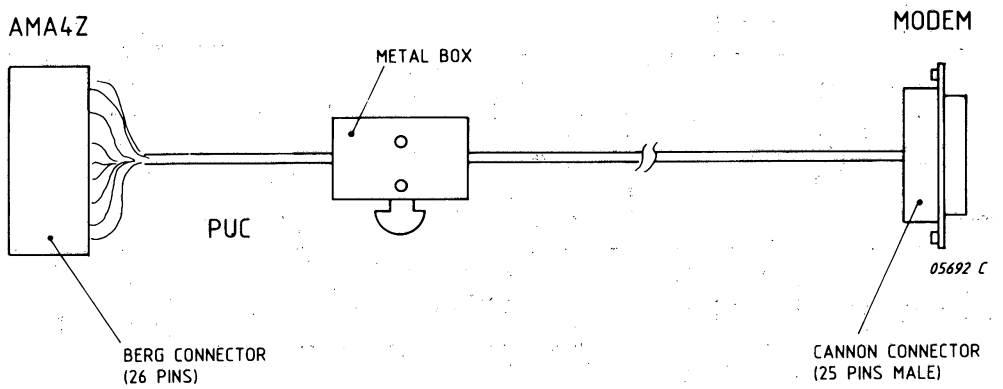


Figure 25.5 MODEM CABLE

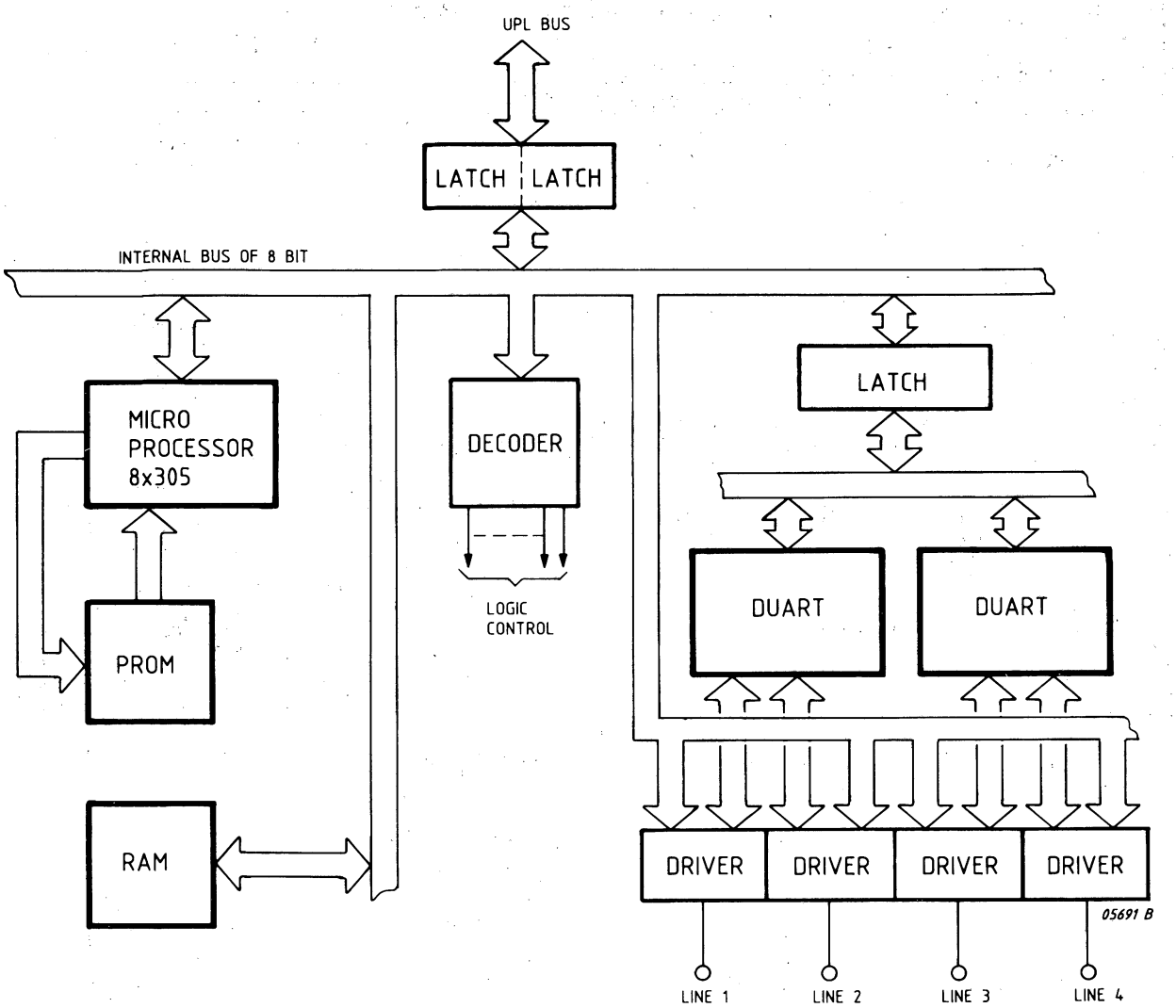


Figure 25.6 BLOCK DIAGRAM AMA4Z

25.6. HARDWARE SOFTWARE INTERFACE DETAILS

CIO start:

MAD lines	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	1	0	0	0	R3			1	1	CU ADDRESS					

The CU address mut be equal to the strap setting on the card, R3 is not relevant.

SST:

MAD lines	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	0	1	0	0	0	R3			1	1	CU ADDRESS					

The CU address mut be equal to the strap setting on the card, R3 is not relevant.

List of commands (in IOD):

command	command code
TEST CU	/80
CONNECT	/00
SEND	/01
RECEIVE	/02
CANCEL	/03
DISCONNECT	/04
SET PARAMETER	/05
READ STATUS	/06
TERMINATE	/81

Abbreviations in the IOD:

COM = Command
IOAA = I/O area address
IOAL = I/O area length
IOSC = special character table address
LOGSTA = logical status
LRC = LRC character
PHYSTA = pysical status
RDN OUT = relative device number
SUBCOM = sub command
TIMVAl = timer value

25.6.1 TEST CU

The layout of the IOD is:

	0 7	8 15
0	/00	/80
2	Not Used	LOGSTA
4	PHYSTA	
6	GLOBAL PARAMETER	
8	Parameter 1	Line 1
A	Parameter 2	Line 1
C	Parameter 1	Line 2
E	Parameter 2	Line 2
10	Parameter 1	Line 3
12	Parameter 2	Line 3
14	Parameter 1	Line 4
16	Parameter 2	Line 4

Global Parameter Description:

0 1 2 3 4 5 6 7 8 9 10 11 12 13	14	15
	B1	B0

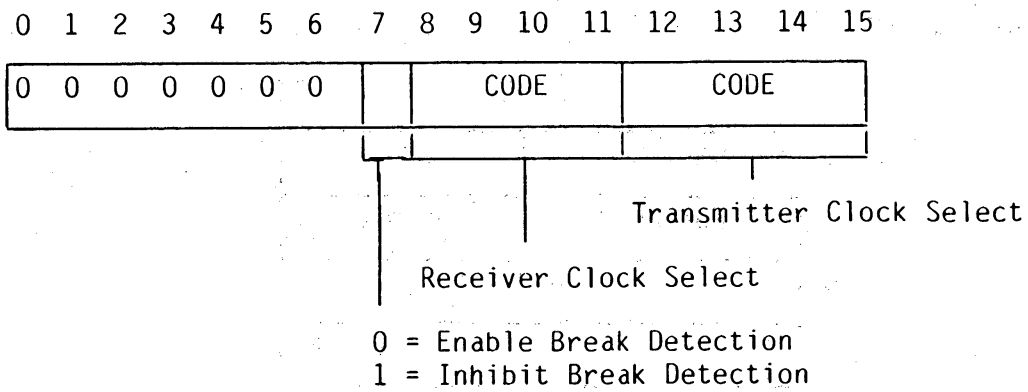
B0 = Baud rate generator set select for line 0 and 1

B0 = 0 set A selected on line 1 and 2
= 1 set B selected on line 1 and 2

B1 = Baud rate generator set select for line 2 and 3

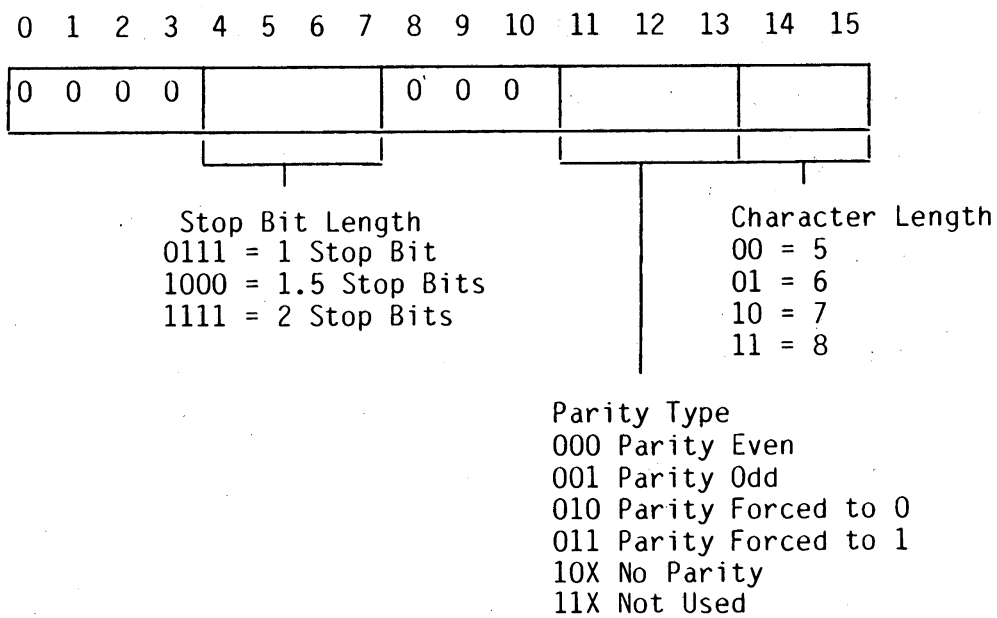
B1 = 0 set A selected on line 3 and 4
= 1 set B selected on line 3 and 4

Parameter 1 Description:



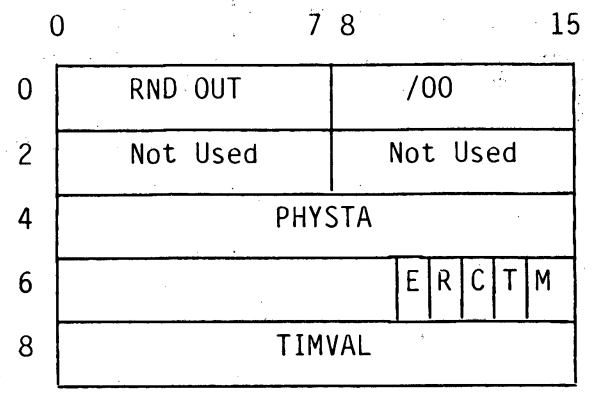
CODE	BAUD RATE SET B	BAUD RATE SET A
0000	75	50
0001	110	110
0010	134.5	134.5
0011	150	200
0100	300	300
0101	600	600
0110	1200	1200
0111	2000	1050
1000	2400	2400
1001	4800	4800
1010	1800	7200
1011	9600	9600
1100	19200	-

Parameter 2 Description:



25.6.2 CONNECT

The layout of the IOD:



E - Normal Reception = 0
Auto Echo Mode = 1

R - CT105 is always active after the execution of a CIO send = 0
CT105 is disactivated after the execution of an CIO send = 1

C - Connect Active = 0
Connect Passive = 1

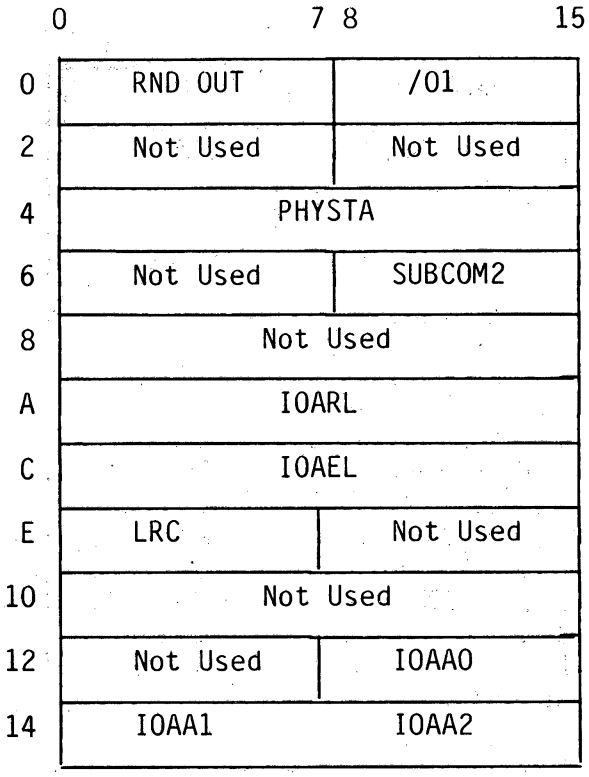
T - Timer OFF = 0
Timer ON = 1

M - Mode CT108/1 = 0
Mode CT108/2 = 1

TIMVAL : unit of 100ms

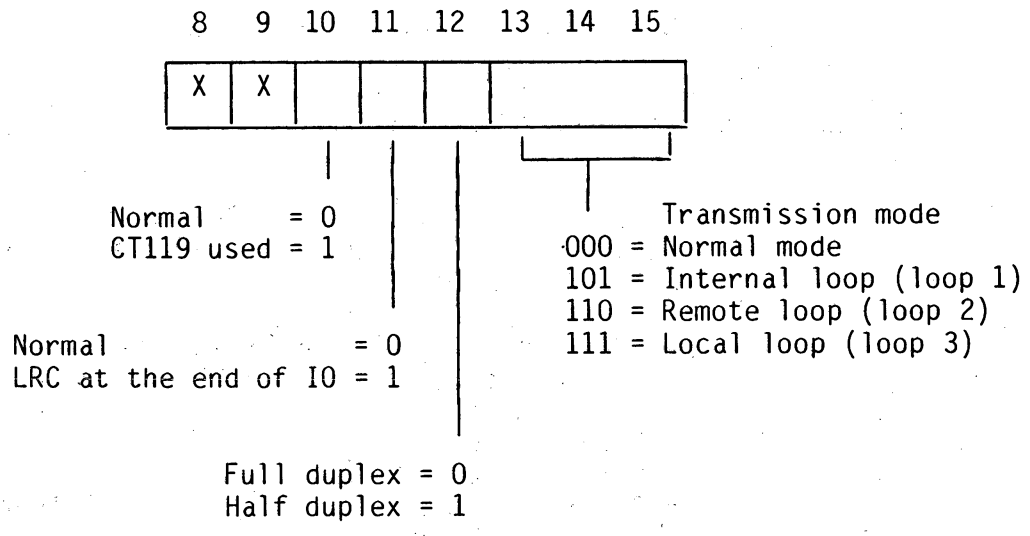
25.6.3 SEND

The layout of the IOD:



RDN OUT = Relative Device number (00 - 03 = line number 1 up to 4)

SUBCOM2 =



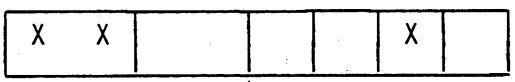
25.6.4 RECEIVE

The layout of the IOD:

	0 7	8 15
0	RND OUT	/O2
2	Not Used	LOGSTA
4	PHYSTA	
6	SUBCOM1	SUBCOM2
8	TIMVAL	
A	IOARL	
C	IOAEL	
E	LRC	IOSCO
10	IOSC1	IOSC2
12	Not Used	IOAAO
14	IOAA1	IOAA2

SUBCOM 1 = Masked Echoing Character.

SUBCOM 2 = 8 9 10 11 12 13 14 15



0 = Special Character Table inactive
1 = Special Character Table active
0 = Normal
1 = Masked Echoing
0 = Look Ahead Character in FIFO
1 = Reset Character in FIFO
00 = Normal Mode
01 = Timer Active
10 = PAI Each Character
11 = PAI Each Character with a minimum between two PAI's given by TIMVAL.

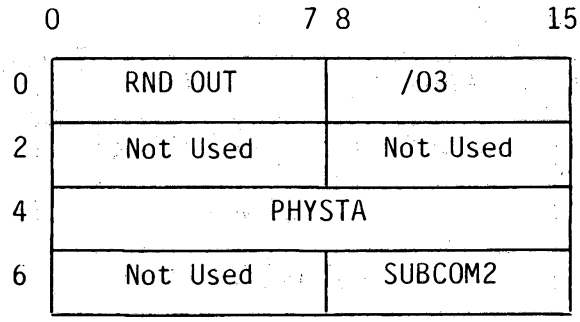
TIMVAL = Timer value in hexadecimal (100mS to 655500mS)

IOSCO-2 Special Character Table Address

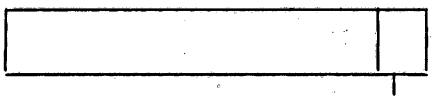
Note: RNOUT = 0 up to 3 (line 1 up to 4)

25.6.5 CANCEL

The layout of the IOD:



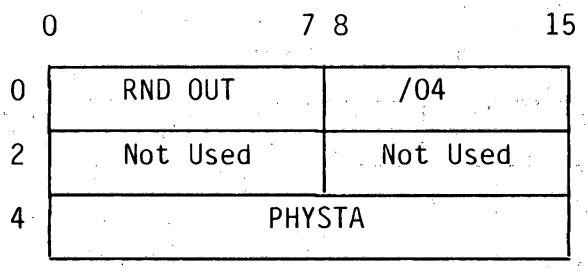
SUBCOM 2 = 8 9 10 11 12 13 15



0 = Receiver part
1 = Transmitter part

25.6.6 DISCONNECT

The layout of the IOD:



25.6.7 SET PARAMETER

The layout of the IOD is:

	0	7 8	15
0	RND OUT	/05	
2	Not Used	Not Used	
4	PHYSTA		
6	PARAMETER 1		
8	PARAMETER 2		
A	PARAMETER 3		
C	Mask Parameter 1		
E	Mask Parameter 2		
10	Mask Parameter 3		

PARAMETER 1 and PARAMETER 2 are the same as in the TEST CU command. (See section 2.5.4.1).

PARAMETER 3:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	140	141	142		105	106	107	108	109		111	125	116	119	126

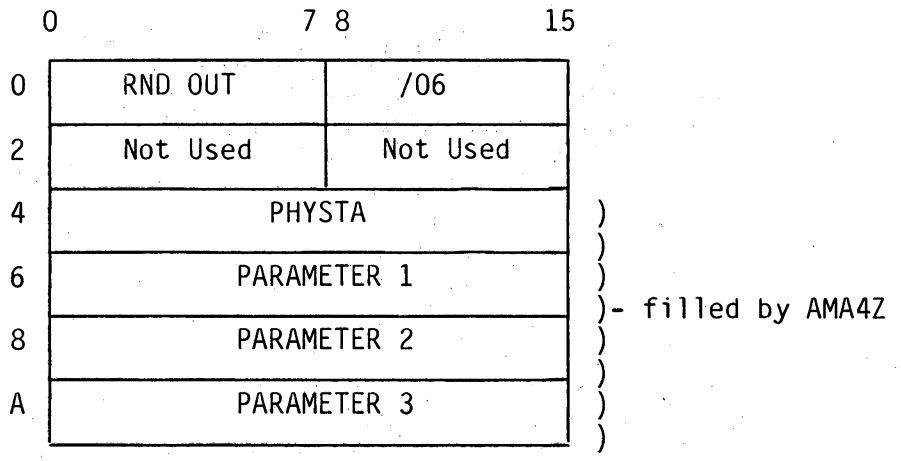
A bit set to 1 is a V24 signal active (+12V at the connector level).

MASK PARAMETER 1, 2 and 3: the mask bits can be filled within the same layout as PARAMETER 1, 2 and 3. (bit set to 0, parameter not changed).

Note: the parameters only can be masked per field.

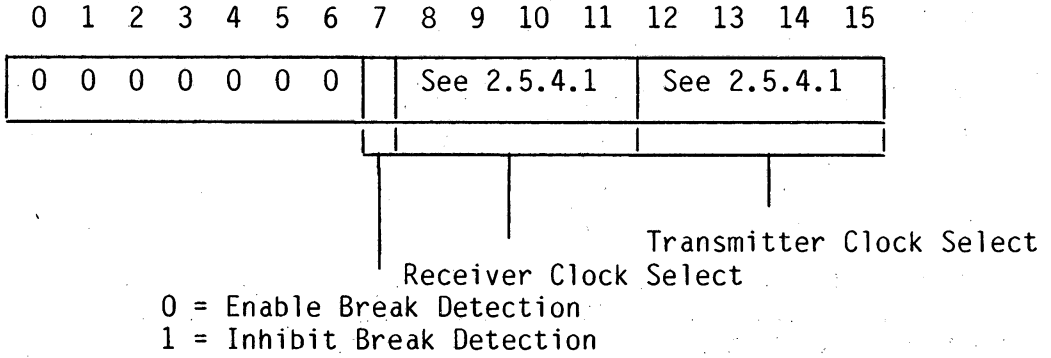
25.6.8 READ STATUS

The layout of the IOD:

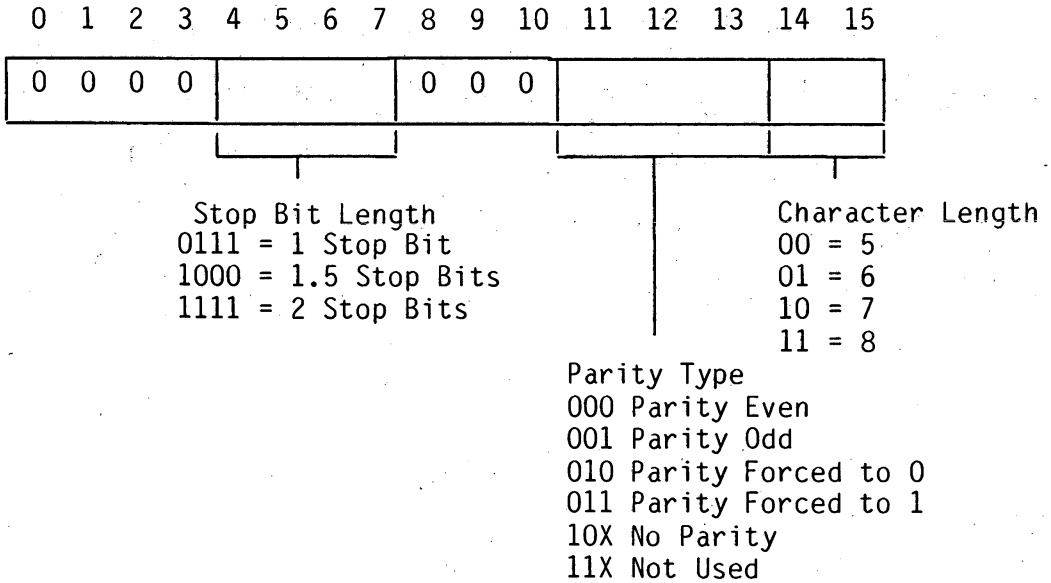


PHYSTA : see Status Description section 25.6.10

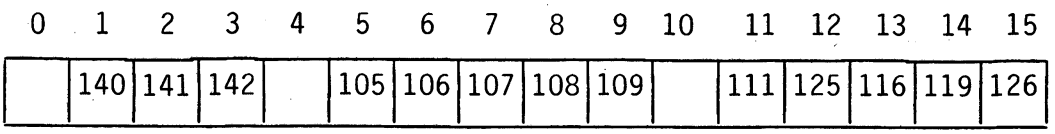
Parameter 1:



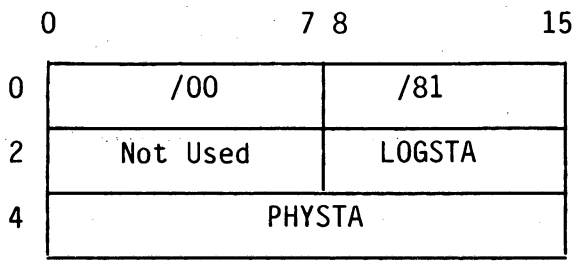
Parameter 2:



Parameter 3:

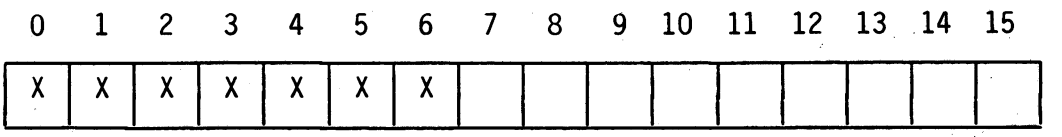


25.6.9 TERMINATE



2.5.6.10 PHYSICAL STATUS

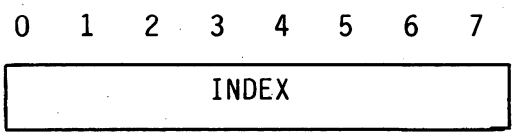
The layout of the Physical Status:



X not significant

- Bit 15: Not Operable
- Bit 14: Overrun Error
- Bit 13: Parity Error
- Bit 12: Framing Error
- Bit 11: Command Rejected
- Bit 10: End of Carrier Detection (CT109 drop)
- Bit 9: Index available in the Logical Status when a terminator is detected by the special character table.
- Bit 8: Break character detected (character zero without stop bit)
- Bit 7: Time out

The layout of the Logical Status:



- INDEX: Index of Special Character Table

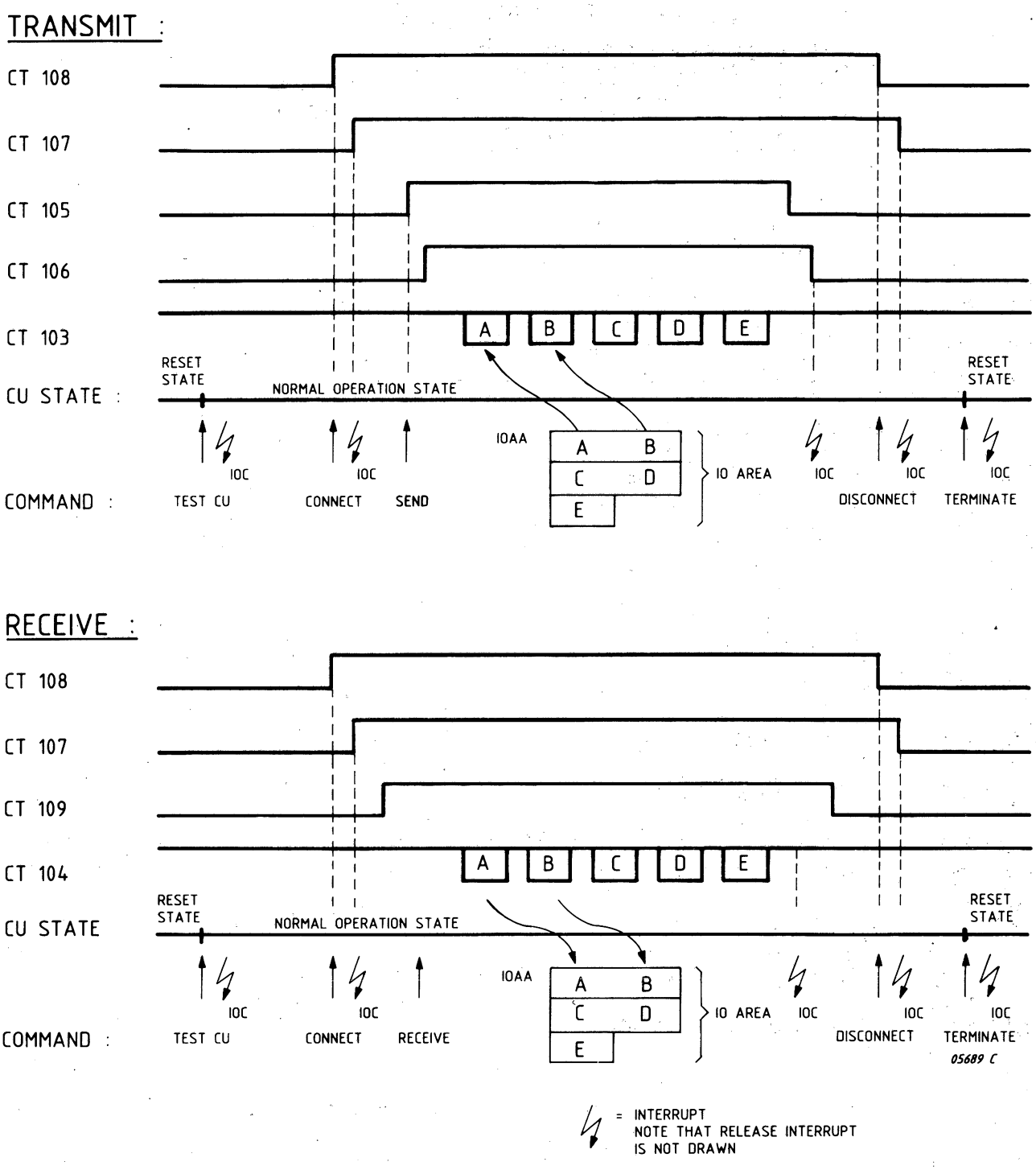


Figure 25.7 COMMAND TIMING

```
                        IDENT    AMA4
                      * THIS PROGRAM SENDS BLOCKS OF DATA ON THE LINE
                      *
                      * THE DATA WHICH IS SENT IS : 0 1 2 3 4 5 6 7 8 9
                      *
                      * AFTER IPL THE PROGRAM STOPS, AND BEFORE RUNNING
                      * REGISTER A1 MUST BE FILLED WITH THE LINE NUMBER:
                      * 00 = LINE 1 (SPEED = 4800; 2 STOPBITS; NO PARITY; 8 DATA BITS)
                      * 01 = LINE 2 (      ,,          ,,          ,,          ,,     )
                      * 10 = LINE 3 (      ,,          ,,          ,,          ,,     )
                      * 11 = LINE 4 (      ,,          ,,          ,,          ,,     )
                      *
                      *
                      *
      0010            INT       EQU       /10
      000A            ADA       EQU       /0A
0000                  RES       /40
0080  FFFF            DATA      /FFFF
0082  0000            DATA      0
0084  0100      START   LDK       A1,0
0086  207F            HLT
                      *
                      * FILL IN LINE NUMBER
0088  E141            SC        A1,IOD2
008A  00EC  R
008C  E141            SC        A1,IOD3
008E  00F6  R
                      *
                      * STORE INTERRUPT POINTERS
0090  87A0            LDKL      A15,/8000
0092  8000
0094  8120            LDKL      A1,RTCINT
0096  00AE  R
0098  8141            ST        A1,4
009A  0004
009C  8120            LDKL      A1,AMAINT
009E  00B2  R
00A0  8141            ST        A1,INT+INT
00A2  0020
00A4  8120            LDKL      A1,CSD
00A6  00C4  R
00A8  8141            ST        A1,/80
00AA  0080
00AC  5768            RF(7)     BEGIN
                      *
                      * REAL TIME CLOCK INTERRUPT
00AE  20F7      RTCINT  RIT       /1B
00B0  F03E            RTN       A15
                      *
                      * AMA4 INTERRUPT ROUTINE
00B2  8140      AMAINT  LD        A1,CID+6
00B4  00D0  R
00B6  E921            CCK       A1,/8080
00B8  8080
00BA  5402            RF(NE)    NORM
00BC  207F            HLT
00BE  49CA      NORM    SST       A1,ADA
00C0  1A01            SUK       A2,1
00C2  F03E            RTN       A15
                      *
                      * IO DESCRIPTORS
00C4  0000      CSD     DATA      0,0,/1000
00C6  0000
00C8  1000
00CA  0000      CID     DATA      0,0,0,0,0
00CC  0000
00CE  0000
00D0  0000
00D2  0000
00D4  0080      IOD1    DATA      /80,0,0,0,/99,/F13,/99,/F13,/99,/F13,/99,/F13
00D6  0000
00D8  0000
00DA  0000
00DC  0099
00DE  0F13
00E0  0099
00E2  0F13
00E4  0099
00E6  0F13
00E8  0099
00EA  0F13
```

```
00EC  0000        IOD2      DATA      0,0,0,0,0
00EE  0000
00F0  0000
00F2  0000
00F4  0000
00F6  0001        IOD3      DATA      1,0,0,0,0,/A,0,0,0,0,IOA
00F8  0000
00FA  0000
00FC  0000
00FE  0000
0100  000A
0102  0000
0104  0000
0106  0000
0108  0000
010A  010C  R
010C  3031        IOA       DATA      /3031,/3233,/3435,/3637,/3839
010E  3233
0110  3435
0112  3637
0114  3839
                  *
                  * MAIN PROGRAM
0116  8120        BEGIN     LDKL      A1,CID
0118  00CA  R
011A  E204                  ECR       A2,A1
011C  22FF                  ANK       A2,/FF
011E  8241                  ST        A2,CSD
0120  00C4  R
0122  21FF                  ANK       A1,/FF
0124  E104                  ECR       A1,A1
0126  8141                  ST        A1,CSD+2
0128  00C6  R
012A  8120        TESTCU    LDKL      A1,IOD1
012C  00D4  R
012E  F7A1                  CF        A15,PREP
0130  0144  R
0132  8120        CONN      LDKL      A1,IOD2
0134  00EC  R
0136  F7A1                  CF        A15,PREP
0138  0144  R
013A  8120        SEND      LDKL      A1,IOD3
013C  00F6  R
013E  F7A1                  CF        A15,PREP
0140  0144  R
0142  5F0A                  RB(7)     SEND
                  *
                  * PREPARE THE CID FOR THE NEW IOD ADDRESS
0144  E204        PREP      ECR       A2,A1
0146  22FF                  ANK       A2,/FF
0148  8241                  ST        A2,CID
014A  00CA  R
014C  21FF                  ANK       A1,/FF
014E  E104                  ECR       A1,A1
0150  8141                  ST        A1,CID+2
0152  00CC  R
0154  F7A1                  CF        A15,COM
0156  015A  R
0158  F03E                  RTN       A15
                  *
                  * START IO ROUTINE
015A  0202        COM       LDK       A2,2
015C  2840                  ENB
015E  41CA                  CIO       A1,1,ADA
0160  8208                  LDR       A2,A2
0162  5C04                  RB(NZ)    *-2                    WAIT FOR IOC INTERRUPT
0164  20BF                  INH
0166  F03E                  RTN       A15
                  *
                  *
                            END       START
```

30 WINCHESTER DISC CU FOR 5.25" DISK DRIVES P829-141 (WDE)

SECTION	30.1	WDE IDENTIFICATIONS	PAGE 30-2
	30.2	INSTALLATION	30-3
	30.3	INTERFACE	30-5
	30.4	DRIVE CHARACTERISTICS	30-7
	30.5	DISK LAYOUT	30-7
	30.6	HARDWARE SOFTWARE INTERFACE DETAILS	30-7
	30.7	SHORT DESCRIPTION OF TESTPROGRAMS	30-9
	30.8	SHORT ROUTINES	30-12

LIST OF ILLUSTRATIONS

FIGURE	30.1	INTERCONNECTION DIAGRAM WDE CONTROLLER	30-3
	30.2	U-LINK SETTING WDE1	30-4
	30.3	CONNECTORS WDE1	30-5

LIST OF TABLES

TABLE	30.1	PROMS WDE1	30-4
	30.2	INTERFACE SIGNALS WDE1	30-6

30.1 WDE IDENTIFICATIONS

Type number : P829-142 WDE CU 5.25" WINCHESTER DISC
5122 194 48350 CARD WDE1

Test program : BWDE1 : SEAGATE ST - 412, RODIME 201E, 202E, 203E, 204E

Channel : DMA - OKI pin 1B07, OKO pin 1B06

Interrupt-connection : BCI (pin 1C03), programmed level

Power Consumption : WDE - +5VL /3.5A

12NC code on the stickers on the board:

WDE1: 5122 194 4835X (5322 216 21586)

X = modification level

Devices: 3 X SEAGATE ST-412 DISKOS 3450-011 10MB (formatted), or

3 X RODIME	201E	10.5	MB, or
3 X RODIME	202E	21	MB, or
3 X RODIME	203E	31.5	MB, or
3 X RODIME	204E	42	MB,

Refer to Chapter 3, RACK RAWIST P829-005

Note : The WDE CU is the replacement CU for the WDD + XEBEC CU.
In P800 RODIME 202E and 204E are used:
- P829 - 025 : Rack Rawist + Rodime Drive 202E or 204E
- P829 - 035 : Extra Rodime Drive 202E or 204E

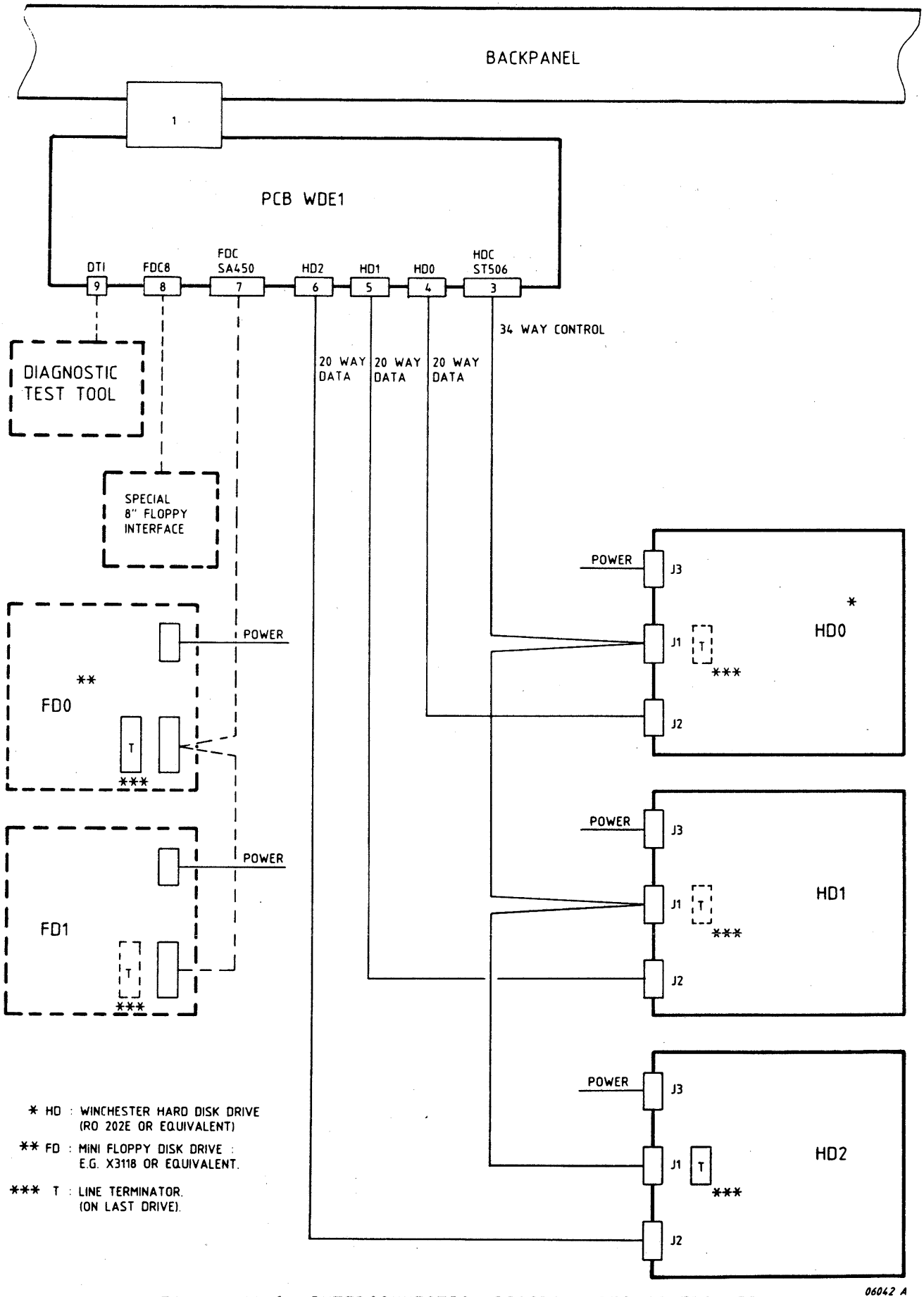


Figure 30.1 INTERCONNECTION DIAGRAM WDE1 CONTROLLER

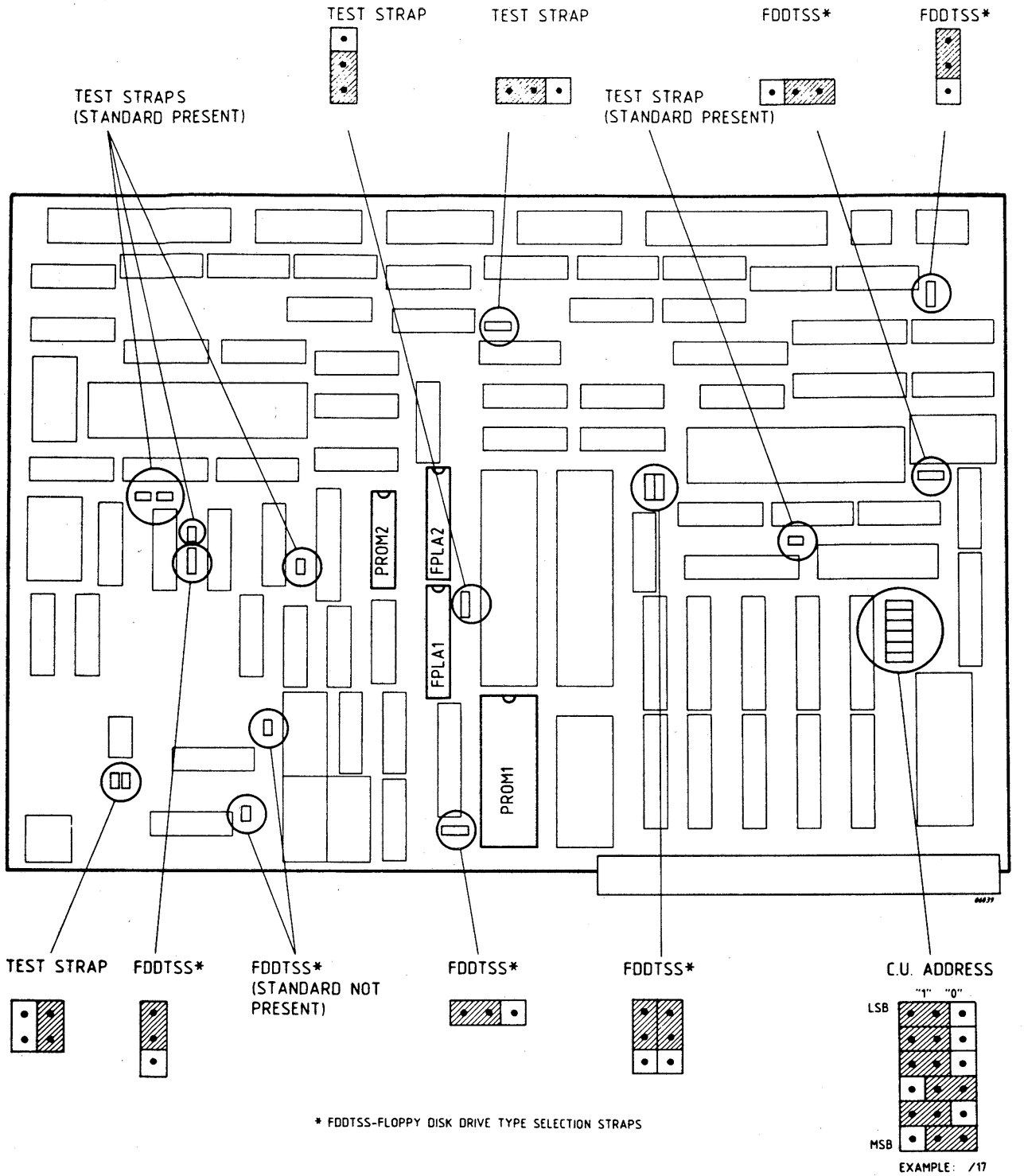


Figure 30.2 U-LINK SETTING WDE1

	LOCATION	IDENTIFICATION	12 NC	DESCRIPTION
PROM1		2764-3 - 012	39471	MPR 5 1/4 DCU
PROM2	D3C6	82S185 - 138	39501	PLL PROM
FPLA	D888	82S153 - 029	39511	
FPLA	D8C9	82S153 - 030	39521	

Table 30.1 PROMS WDE1

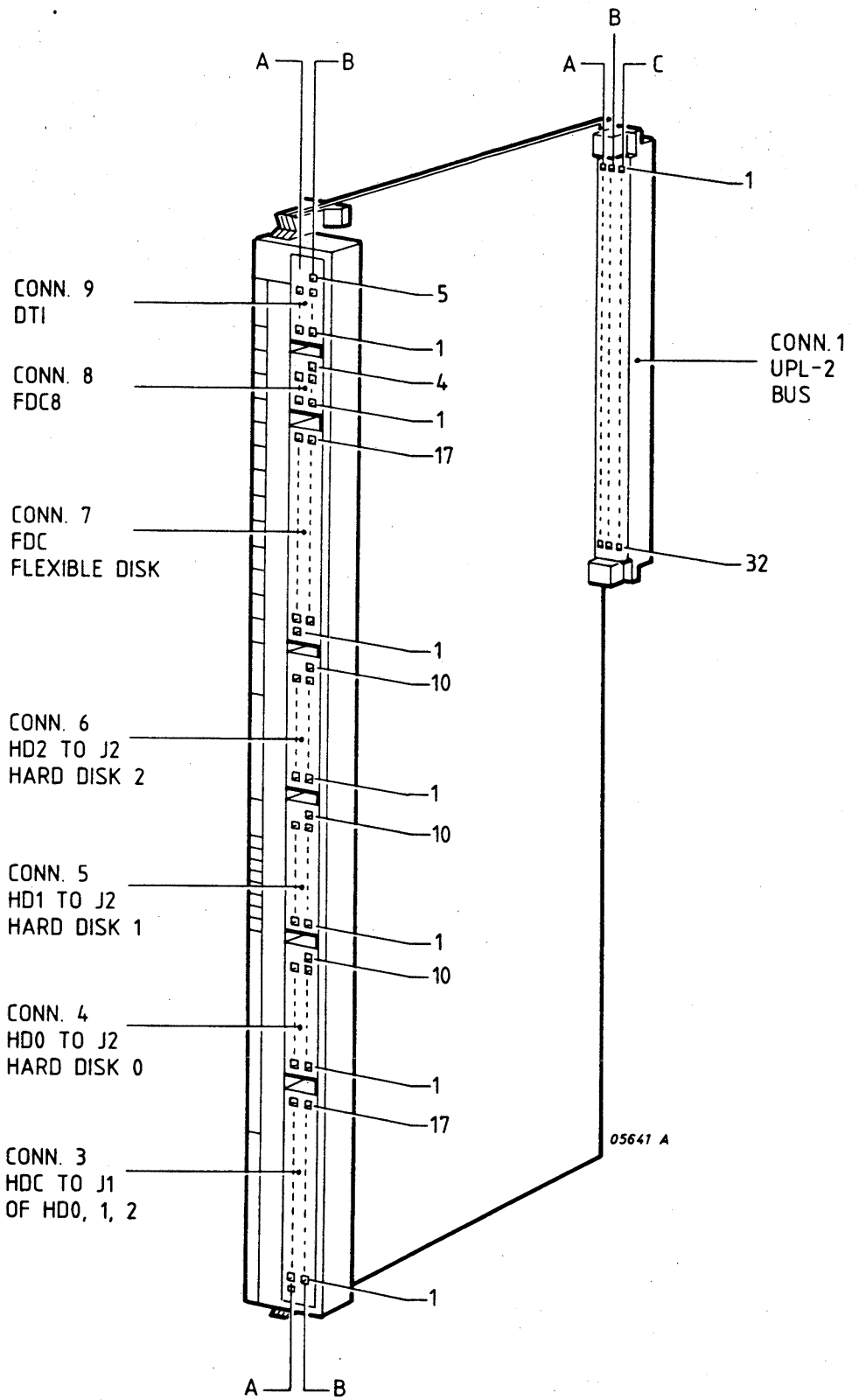


Figure 30.3 CONNECTORS WDE1

HDC Interface

J3	A	B
17	DIR1	L
16		L
15	DS3	L
14	DS2	L
13	DS1	L
12	STEP	L
11	READY	L
10	INDEX	L
9	HSI	L
8		L
7	HSO	L
6	WRTF	L
5	TRO	L
4	SEEKL	L
3	WRG	L
2	HS2	L
1	HS3	DUMMY

HDO Interface

J4	A	B
10	DUMMY	L
9	MRDO	PRDO
8	L	L
7	MWRDO	PWRDO
6	L	L
5	L	
4	L	
3	L	
2	L	
1	L	DRSO

Connector 8, FDC8 Interface

J5	A	B
4	DUMMY	FA8N
3	L	RDY8N
2	L	FARE8N
1	L	LOC8N

Connector 9, DTI Interface

J5	A	B
5	DUMMY	L
4	L	EMADAN
3	L	RESETN
2	L	SDTUN
1	CONNECTN	SDUTN

HD1 Interface

J5	A	B
10	DUMMY	L
9	MRD1	PRD1
8	L	L
7	MWRD1	PWRD1
6	L	L
5	L	
4	L	
3	L	
2	L	
1	L	DRS1

HD2 Interface

J6	A	B
10	DUMMY	L
9	MRD2	PRD2
8	L	L
7	MWRD2	PWRD2
6	L	L
5	L	
4	L	
3	L	
2	L	
1	L	DRS2

Connector 7, FDC Interface

J3	A	B
17	IUDCH	L
16	HSEL	L
15	RD	L
14	WRPROT	L
13	TRKO	L
12	WRGF	L
11	WRD	L
10	STP	L
9	DIRS	L
8	MOTON	L
7		L
6	SEL2	L
5	SEL1	L
4	INDX	L
3	SEL4R	L
2		L
1		DUMMY

Table 30.2 INTERFACE SIGNALS WDE1

30.4 DRIVE CHARACTERISTICS

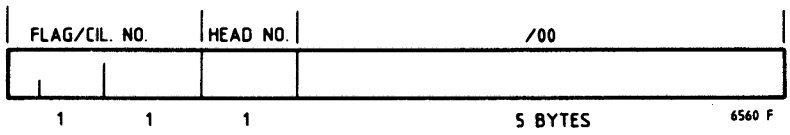
DISK MODELS	ST412	RO201E	RO202E	RO203E	RO204E
- CAPACITY OF DISK PACK (FIXED)	10 MB	10.5 MB	21MB	31.5MB	42MB *
- NUMBER OF CYLINDERS	306	640	640	640	640
- TRACKS PER CYLINDER (HEADS)	4	2	4	6 ~~4~~	8 ~~4~~
- SECTORS PER TRACK	32	32	32	32	32
- BYTES PER SECTOR	256	256	256	256	256

* (formatted)

Refer also to chapter 3, RACK RAWIST, for more information about the drives.

30.5 DISC LAYOUT

The IDENTIFIER FIELD (8 bytes) is as follows:



Flag (2 bits) = 00 if Primary track
01 if Detective track
10 if Alternate track

Cyl. (No. 14 bits)

30.6 HARDWARE SOFTWARE INTERFACE DETAILS

Refer to chapter 27.6 for the description of the BEZARDS interface and Status bytes.

The following commands are supported:

General commands

/80 Test control unit
/81 Terminate
/82 IPL
/83 Read identification

NORMAL DISK COMMANDS

/00 Read data
/01 Write data
/02 Search key equal
/03 Search key equal with data return
/04 Search key high
/05 Search key high with data return
/06 Format track
/07 Format defective track
/08 Format alternate track
/0A Toper
/0B Indicate access parameters
/0C Program load
/0F Search multiple index
/10 Format pack

ERROR RECOVERY

/17 Return to zero
/1A Disable retry
/1D Enable retry

SERVICE COMMANDS

/12 Read identifier (note that only one identifier will be transmitted)

The "/0B" command (INDICATE ACCESS PARAMETERS) is mandatory.

The IOD parameters are:

Name		Code	Address
RDN - out (drive number)		- - = /- -	IOD+/0
Command	COM	11 = /0B	IOD+/1
Number Of Cylinder	NOC	306 = /0132 *	IOD+/16
Number of Heads	NOH	4 = /4 *	IOD+/18
Start Reduced Write Curr.	SRWCC	128 = /0080 *	IOD+/19
Start Write Pre Comp. Curr.	SWPCC	0 = /0000 **	IOD+/1B
ECC Length	ECCM	11 = /0B **	IOD+/1D
INTERLEAVE Factor	INTERL	3 = /03 **	IOD+/1E
Step Rate Access Motor	STEP	14 = /0E *	IOD+/1F

* Default value; may be different for each drive.
** Default value, which cannot be changed (fixed).

Note: STEP = 14 advised for all drives.

30.7 SHORT DESCRIPTION OF TEST PROGRAMS

TEST PROGRAMS BWDE1

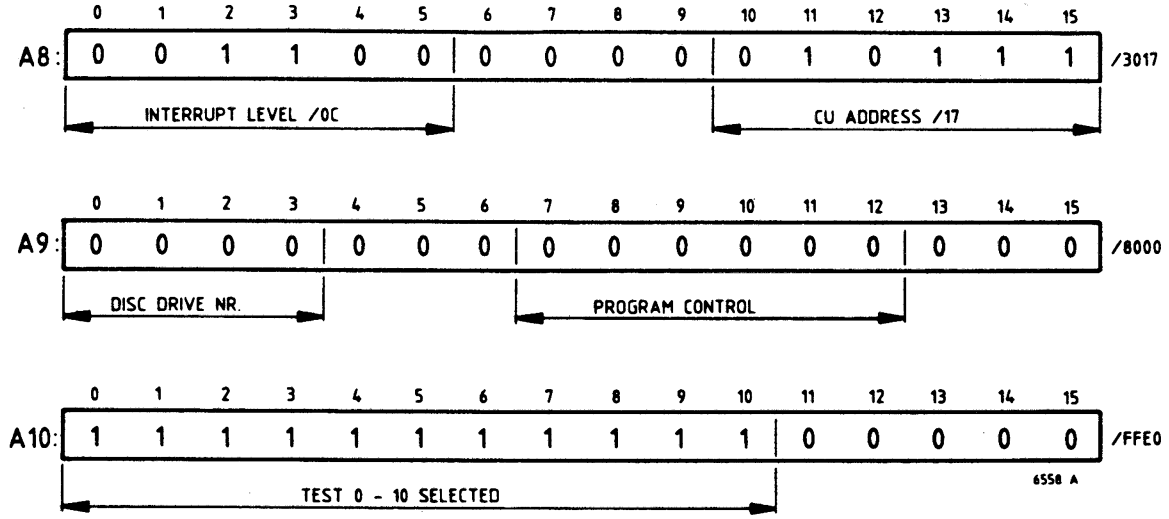
For P829-005/006 connected to P829 WDE

Procedure:

After IPL the program stops at /0700, which is also the restart address. Parastic interrupts cause the program to stop and return to address /0700. RTC on, PWF/AR possible.

CAUTION: THE USER's DATA WILL BE OVERWRITTEN

REGISTER MODIFICATION:



A13: PATTERN TO BY WRITTEN ON THE DISC.

Press MCL, RUN: Initialisation dialogue starts...

MESSAGE	REPLY
- TYPE OF DISK UNIT: (SEAGATE=0, RODIME 201E-204E=1-4) 0, 1, 2, 3, or 4 *	
- DO YOU INTEND TO TEST A CERTIFIED PACK?	Y or N

Then program starts the checks according to register A10.
After completion of the test the program stops at /0700 or if A9 Bit 10 is 1, the program is automatically restarted.
For further details refer to official testprogram description.

* Note:

DISK UNIT CHARACTERISTICS

- Model 0: CYL. 0-305, 1st.ALT=300, TRK/CYL=4 SEC/TRK=32, BYT/SEC=256
- Model 1: CYL. 0-639, 1st.ALT=634, TRK/CYL=2, SEC/TRK=32, BYT/SEC=256
- Model 2: CYL. 0-639, 1st.ALT=634, TRK/CYL=4, SEC/TRK=32, BYT/SEC=256
- Model 3: CYL. 0-639, 1st.ALT=634, TRK/CYL=6, SEC/TRK=32, BYT/SEC=256
- Model 4: CYL. 0-639, 1st.ALT=634, TRK/CYL=8 SEC/TRK=32, BYT/SEC=256

BWDE1 Checks

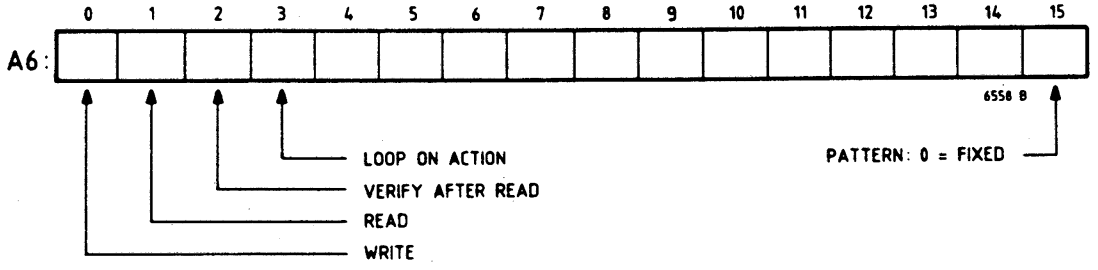
> Note: Some checks need either special DATA recorded on the disk pack or bad tracks formatted.
> Take care that the sequence of checks is correct for: IF0009 and IF0012

IF0000: Writing of the Format
IF0001: Command in Reset State
IF0002: Write and Read Test
IF0003: Fast Access Read Commnad
IF0009: Worst Case Pattern
IF0012: Write/Read Service Routine (Optional)
1F0014: Bad Parameter in Command (Optional)
1F0015: IPL (Optional)

Notes:

IF0012 Write/Read Service Routine needs the following parameters:

- A1 (Bits 8-15) and A2 (Bits 0-15) contain the first sector number (24 Bits).
- A3 and A4 contain (in the same format as A1 and A2) the last sector number.
- A5 contains the test pattern if in A6 fixed pattern is specified.



IF0015 IPL is only possible from a not certified pack.

DISC SECTOR NUMBERING:

- 10MB FROM /000000 THROUGH /0098FF

BWDE1: Procedure 12NC - 5111 991 13262
Listing 12NC - 5111 991 13272
Program 12NC - 5111 199 55752

APPLICATION PROGRAM WDEU

WDEU is a program to check the magnetic surface of the disks.

After IPL the program asks for the TIME (HH, MM, SS): Answer "TIME", CR or only CR.
After that the program asks for the CU-address and Interrupt Level (both in decimal format)
Then the program asks a command by printing:
S:

> WARNING
> All Commands (except CONT, HELP and LSDT) will
> DESTROY ANY DATA already recorded on the disk.
> In certain cases even the BAD TRACK LIST is destroyed.
> Make sure that you have saved the DATA and have a
> BAD TRACK LIST produced by the previous certification

LIST OF COMMANDS:

COMMAND	FUNCTION
CERT	Certify Disk Pack: Defective track handling and automatic alternate track handling
CONT	CONTROL UNIT test
DUMP	Dump of (selected) Sector(s) on the operator's Console.
HELP	Edition of the command set.
LSDT	List Defective Tracks of the disk pack
REPL	Replace a defective track
SPOT	Tracking Bad Spots on the magnetic surface
STOR	Store Program on the disk (including IPL)

CONTROL PANEL INTERRUPT:

Pressing the Control Panel Interrupt button aborts the current function and the program types S: waiting for a new command.
Doing so makes RESULTS UNPREDICTABLE, especially in case of WRITE functions.

PARASTIC INTERRUPTS:

Any Interrupt other than Control Panel, Power Failure, Real Time Clock, or the Disk Control Unit will stop the program.
The level of the parastic interrupt will be in the PSW (RST button).
The program has to be loaded again with IPL.

POWER FAILURE INTERRUPT:

The system must be switched to LOCK mode and no other peripherals than the disk units must be READY.

WDEU: Procedure 12NC 5111 991 13472
Listing 12NC 5111 991 13462
Program 12NC 5111 199 55342

30.8 SHORT ROUTINES

For the WDE the same Short Routine as for the WDD can be used (routine SEAWDD).

The registers A10, A11 and A12 can be changed if Rodime drive has to be tested:

A10, A11 (END SECTOR)	A12 (INCREMENT VALUE)	DRIVE
/0098, /FF00	/0020 or /0080	SEAGATE ST412
/009F, /FF00	/0020 or /0040	RODIME 201E
/013F, /FF00	/0020 or /0080	RODIME 202E
/01DF, /FF00	/0020 or /00C0	RODIME 203E
/027F, /FF00	/0020 or /0100	RODIME 204E